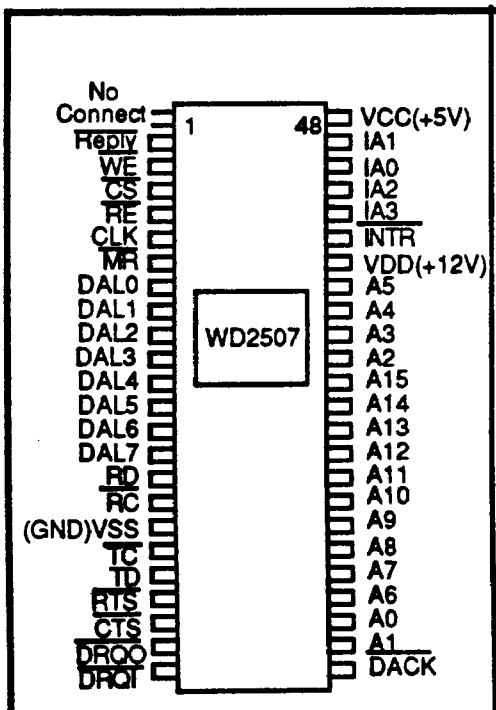
WESTERN DIGITAL
CORPORATION

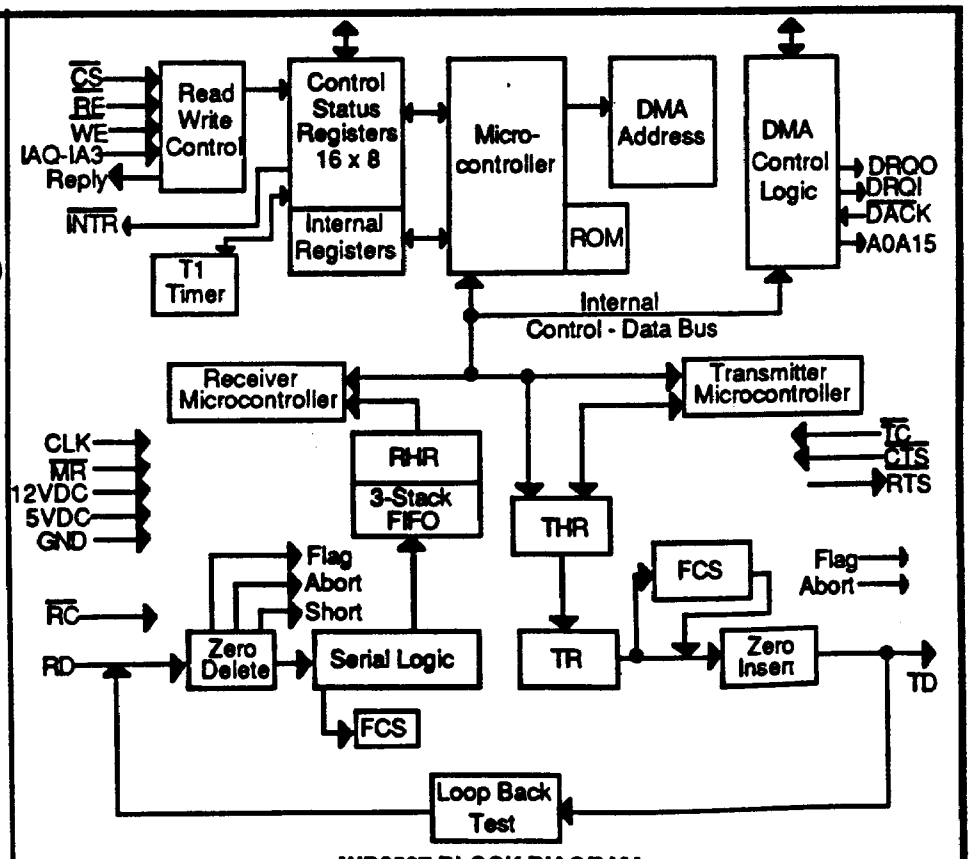
PRELIMINARY
WD2507 Signalling Link Controller

FEATURES

- Performs major portions of the Signalling Link Control for Signalling System No. 7. Q.703.
- Transmits and receives full-duplex serial data at rates up to 64Kbps.
- Dual channel DMA for full-duplex operation.
- Unique memory access method for buffer management.
- All formatting of bit-oriented control including zero bit insertion and deletion, automatic appending, and testing of flags and FCS fields.
- Automatic control of sequence numbers FSN and BSN and control bits FIB and BIB, modulo 128.
- Selectable "Basic" error correction method or the Preventive Cyclic Retransmission error correction method.
- 48-pin dual in-line package. Pin compatible with the WD2511A X.25 LAPB controller and the WD2840A LAN Token Access Controller.
- TTL compatible.



PIN DESIGNATION



WD2507 BLOCK DIAGRAM

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APPLICATIONS

DIGITAL TELEPHONE SIGNALLING
ISDN TRUNK SIGNALLING
SATELLITE LINKS
PBX SWITCHING/ROUTING
DATA BASE SERVICE CONTROL

GENERAL DESCRIPTION

Signalling System Number 7 is an international standard for common channel signalling systems and is used within digital telecommunications networks for call control, remote control, management and maintenance signalling.

The flexible nature of the device allows more general application in systems that have long roundtrip delays, notably satellite systems. As with other members of the Western Digital family of Protocol Controllers, all real-time protocol functions are fully handled by the WD2507. Thus, high speed, high efficiency communications are easily integrated into new and existing designs.

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REFERENCE:

CCITT Red Book, Volume VI - Fascicle VI.7, Q.703, VIIIth Plenary Assembly, Geneva, 1984

Bell Communications Research Specification of Signalling System Number 7, TR-NPL-000246 Issue 1, 1985

TABLE 1: INTERFACE SIGNALS DESCRIPTION (All signals are TTL compatible)

PIN NO.	SYMBOL	PIN NAME	FUNCTION
1		No Connection	Leave pin open
2	$\overline{\text{REPLY}}$	Reply	An active low output to indicate the WD2507 has either a $\overline{CS} \bullet \overline{RE}$ or a $\overline{CS} \bullet \overline{WE}$ input.
3	$\overline{\text{WE}}$	Write Enable	The data on the DAL are written into the selected register when $\overline{CS}$ and $\overline{WE}$ are low.
4	$\overline{\text{CS}}$	Chip Select	Active low chip select for CPU control of I/O registers.
5	$\overline{\text{RE}}$	Read Enable	The contents of the selected register are placed on DAL when $\overline{CS}$ and $\overline{RE}$ are low.
6	CLK	Clock	Clock input used for internal timing. Must be square wave, 2MHz +5%.
7	$\overline{\text{MR}}$	Master Reset	Initialize on active low. All registers reset to zero, except control bits MDISC and $\overline{\text{LINK}}$ are set to 1. $\overline{\text{DACK}}$ must be stable high before $\overline{MR}$ goes high.
8-15	DAL0-DAL7	Data Access Lines	An 8-bit bi-directional three-state bus for CPU and DMA controlled transfers.
16	RD	Receive Data	Receive serial data input.
17	$\overline{\text{RC}}$	Receive Clock	This is a 1x clock input, and RD is sampled on the rising edge of $\overline{RC}$. RD changes occur on the falling edge of $\overline{RC}$.
18	V_{SS}	Ground	Ground.
19	$\overline{\text{TC}}$	Transmit Clock	A 1x clock input. TD changes on the falling edge of TC.
20	TD	Transmit Data	Transmitted serial data output.
21	$\overline{\text{RTS}}$	Request-To-Send	An open collector (drain) output which goes low when the WD2507 is ready to transmit either flags or data.
22	$\overline{\text{CTS}}$	Clear-To-Send	An active low input which signals the WD2507 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.
23	$\overline{\text{DRQO}}$	DMA Request Out	An Active low output signal to initiate CPU bus request so the WD2507 can output onto the bus.
24	$\overline{\text{DRQI}}$	DMA Request In	An active low output signal to initiate CPU bus request so that data may be input to the WD2507. $\overline{\text{DRQO}}$ and $\overline{\text{DRQI}}$ will not be low at the same time.
25	$\overline{\text{DACK}}$	DMA Acknowledge	An active low input from the CPU in response to the $\overline{\text{DRQI}}$ or $\overline{\text{DRQO}}$. $\overline{\text{DACK}}$ must not be low if CS and $\overline{RE}$ are low or if $\overline{CS}$ and $\overline{WE}$ are low.

INTERFACE SIGNALS DESCRIPTION CONTINUED

PIN NO.	SYMBOL	PIN NAME	FUNCTION
26-41	A0-A15	Address Lines Out (See front page for Pin Assignments)	Sixteen address outputs from the WD2507 for DMA operation. If the control bit ADRV is 1, the outputs are TTL drives at all times. If ADRV is 0, the outputs are three-state, and are Hi-Z whenever $\overline{DACK}$ is high. (ADRV is in Control Register #1.)
42	V_{DD}	Power Supply	+ 12VDC power supply input.
43	$\overline{INTR}$	Interrupt Request	An active low interrupt service request output, and returns high when Status Register #1 is read.
44-47	IA0-IA3	Address Lines In (See front page for Pin Assignments)	Four address inputs to the WD2507 for CPU controlled read/write operation with registers in the WD2507. If ADRV = 0, these may be tied to A0-A3. (ADRV is in Control Register #1.)
48	V_{CC}	Power Supply	+5VDC power supply input.

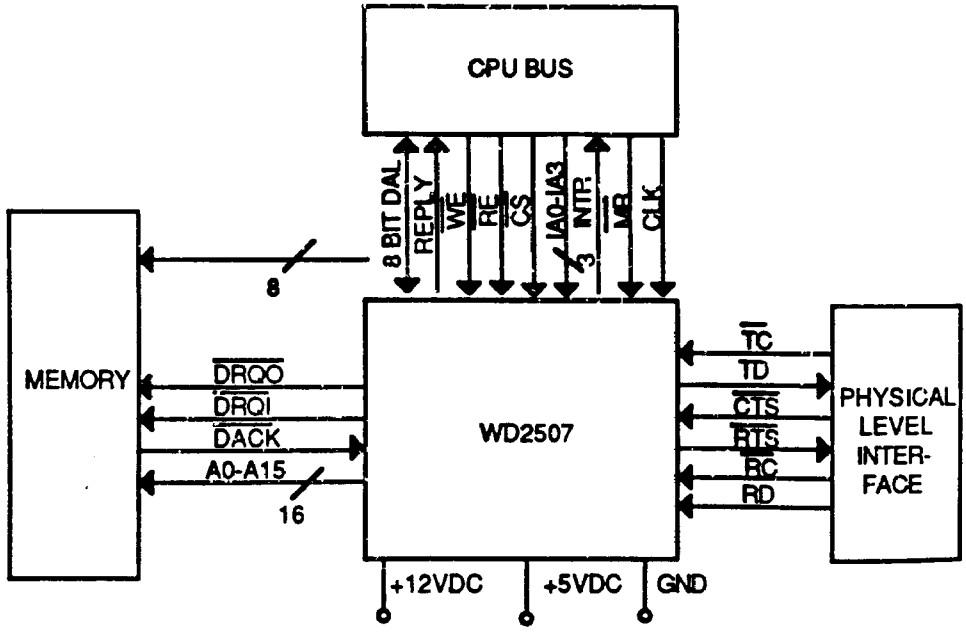


Figure 1: SYSTEM CONNECTION

1.0 INTRODUCTION

This document describes the operation and programming of the WD2507 protocol controller chip. This chip supports the CCITT Signalling System No. 7 Link Layer protocol. As shown in Figures 7 and 8, about two-thirds of the functionality of Q.703 (the link layer) is carried out by this chip. The following functional blocks are supported.

1) DAEDT Delimination, Alignment and Error Detection (Transmitting)
2) DAEDR Delimination, Alignment and Error Detection (Receiving)
3) SUERM Signal Unit Error Rate Monitor
4) AERM Alignment Error Rate Monitor
5) TXC Transmission Control
6) RC Reception Control
7) CC Congestion Control

Key features which are supported include:

1) Both "Basic" and "Preventitive Cyclic Retransmission" (PCR) methods.
2) Congestion Control -- T5 maintained and SIB's sent automatically.
3) Both Signal Unit and Alignment Error Rate Monitors.
4) Automatic repetitive transmission of LSSU's and FISU's.

The WD2507 is controlled and monitored through a combination of host accessable registers within the WD2507 and external RAM-based data structures. The WD2507 has two internal DMA channels which it uses to read transmit data and write received data concurrently. These DMA channels are also used to access control structures, error counters, and a work area containing internally used values. Programmable registers are used to set the starting address for these memory structures.

1.1 ORGANIZATION

A detailed block diagram of the WD2507 is shown on the front page.

Mode control and monitor of status by the user's CPU is performed thru the 16 I/O registers.

Internal control of the WD2507 is by means of 3 microcontrollers: one for receive, one for transmit, and one for the internal protocol control.

Parallel transmit data is entered into the Transmitter Holding Register (THR), and then presented to the Transmitting Register (TR) which converts the data into a serial bit stream. A five bit serial buffer facilitates zero bit insert under control of the Transmitter Microcontroller. The 16 bit FCS is calculated and transmitted from the FCS register.

Parallel receive data entering the Receiver Holding Register (RHR) from a 3-stack FIFO input is from a 24 bit serial Receiver Register (RR). This 24 bit register prevents received FCS data from entering the RHR. The receiver FCS register is used to test the correctness of the received FCS.

Serial data is defined in blocks called Signal Units (SU). An SU may be a Fill-in Signal Unit (FISU), a Link Status Signal Unit (LSSU), or a Message Signal Unit (MSU). (See Figure 2). Each SU starts and ends with a unique Flag (01111110). In between flags, data transparency is maintained by the insertion of a 0 bit after each sequence of 5 contiguous 1's. Inserted 0 bits are stripped-off by the receiver. The last 16 bits before the closing flag is the FCS.

Signalling System No. 7 requires that no more than 6 flags be transmitted without sending a frame. If there is no user or status information to be sent, the chip will send fill-in signal units.

The transmitter will only send one flag in between frames.* The receiver will, of course accept multiple flags between frames.

* Note: In future revisions of the WD2507, the user will be able to increase number of flags that are sent by transmitter.

The FCS calculation includes all data between opening flag and the first bit of the FCS, except for 0's inserted for transparency. The 16 bit FCS has the following characteristics:

Polynomial: $X^{16} + X^{12} + X^{5} + 1$
Transmitted Polarity: Inverted
Transmitted Order: High order bit first
Preset Value: All 1's
FCS Register Value: 0001110100001111
If Received Correct (high order bit shown in LSB)

The WD2507 generates and tests Flags, FCS, inserted zeroes, FSN, BSN, FIB, BIB, and LI. SIO and SIF data are accessed thru DMA control. Serial data is generated and received by the bit-oriented transmitter and receiver. (See Figure 2).

The WD2507 performs most of the signalling link control. All FISU's are automatically generated and tested by WD2507. The user need only be concerned with the SF field of LSSU's and the SI and SIF fields of MSU's. If the WD2507 has no outstanding MSU's or LSSU's, it will transmit continuous FISU's.

The WD2507 will discard all received SU's which do not meet all the minimum conditions:

1. FCS Correct.
2. A multiple of 8 bits.
3. At least 5 bytes between flags.
4. A correct Length Indicator. (See Section 3.9)

When this document refers to an SU as "received" that SU is understood to meet all the above minimum conditions. In some cases an error counter may be incremented, but the SU is not considered as received unless all minimum conditions are met.

Refer to section 8.0 for a glossary of terms.

Fill In Signal Unit (FISU) LI = 0

← FISU's completely controlled by WD2507 →								
FLAG	BSN	BIB	FSN	FIB	LI	00	FCS	FLAG
8	7	1	7	1	6	2	16	8

Link Status Signal Unit (LSSU) LI = 1 or 2

← appended by WD2507 →							Selected by User	← appended → by WD2507	
FLAG	BSN	BIB	FSN	FIB	LI	00	SF	FCS	FLAG
8	7	1	7	1	6	2	8 or 16	16	8

Message Signal Unit (MSU) LI > 2

← appended by WD2507 →							← DMA →		← appended → by WD2507	
FLAG	BSN	BIB	FSN	FIB	LI	00**	SIO	SIF	FCS	FLAG
8	7	1	7	1	6	2	8	8n, n>2	16	8

* Numbers under SU show number of bits
** Supplied by users; normally 00

Figure 2: THE THREE SIGNAL UNIT (SU)TYPES

2.0 PROGRAMMING THRU REGISTERS

The WD2507 is programmed by 7 write/read registers, and is monitored by 2 status, read-only registers.

Figure 3: WD2507 REGISTERS

REGISTER NO.	IA3	IA2	IA1	IA0	REGISTER NAME
0	0	0	0	0	CR0-Control Register 0
1	0	0	0	1	CR1-Control Register 1
2	0	0	1	0	BSNR (Internal Use)
3	0	0	1	1	IR0-Interrupt Register 0
4	0	1	0	0	SR0-Status Register
5	0	1	0	1	(Internal Only)
6	0	1	1	0	(Internal Only)
7	0	1	1	1	FSNT (Internal Only)
8	1	0	0	0	TR0-Timer (Low Byte)
9	1	0	0	1	TR0-Timer (High 2 Bits)
A	1	0	1	0	CBPH-Control Block Pointer
B	1	0	1	1	CBPL-Hi and Low
C	1	1	0	0	(Internal Only)
D	1	1	0	1	(Internal Only)
E	1	1	1	0	SLSSU-Send LSSU
F	1	1	1	1	CR2 - Control Register 2

CONTROL/STATUS REGISTER ENCODING

REG	BITS 7	6	5	4	3	2	1	0
0. CR0	PCR/ Basic	0	Restart	DMA Test	Loop Test	RAM Test	RECV On	Inactive
1. CR1	Accept	Send MSSU	Send LSSU	ADRV	0	0	0	Send
2.								
3. IR0	MSUR	XMA	ATTN	X	Link Fail	RX LSSU	RX NRDY	X
4. SR0	T1	$\overline{\text{IRTS}}$	REC IDLE	X	X	RLSSU/Failure		
5.								
6.								
7.								
8. TIMER	$T1_7$	$T1_6$	$T1_5$	$T1_4$	$T1_3$	$T1_2$	$T1_1$	$T1_0$
9. TIMER	$T5_5$	$T5_4$	$T5_3$	$T5_2$	$T5_1$	$T5_0$	$T1_9$	$T1_8$
10. CBPH	B_{15}	B_{14}	B_{13}	B_{12}	B_{11}	B_{10}	B_9	B_8
11. CBPL	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0
12.								
13.								
14. SLSSU	0	0	0	0	0	LSSU Type		
15. CR2	0	0	0	0	FISU INT	BUSY NAK	ALIGN	TRM OFF

Notes:
- Whenever any of the three bits MSUR, XMA, or ATTN is a 1, $\overline{\text{INTR}}$ will go low. After IR0 is read, all three bits will return to 0, and $\overline{\text{INTR}}$ will return high.
- "X" represents a bit used by the WD2507's internal microcontroller. At any time these bits may be "1" or "0", and are to be disregarded by the user's CPU.
- Unused control bits must be left a "0"

CONTROL REGISTER 0

Register	CR07	CR06	CR05	CR04	CR03	CR02	CR01	CR00
CR0	PCR/$\overline{\text{BASIC}}$	0	RESTART	DMA TEST	LOOP TEST	RAM TEST	RECV ON	INACTIVE

BIT	NAME	DESCRIPTION
CR00	INACTIVE	This bit, when set, commands the WD2507 to reset. The WD2507 will not transmit or accept serial data until INACTIVE = 0. INACTIVE will go to 1 when $\overline{\text{MR}}$ is enabled.
CR01	RECV ON	Defines the CPU's receiver memory as initially ready (RECV ON = 1) or initially not ready ((RECV ON = 0).
CR02	RAM TEST	Enables a self test for registers internal to the WD2507. (See section 7.0 on SELF-TESTS.)
CR03	LOOP TEST	Internally ties TD back to RD, and $\overline{\text{TC}}$ to $\overline{\text{RC}}$. The normal inputs of RD and $\overline{\text{RC}}$ are logically disconnected. There will still be an output at TD, and $\overline{\text{TC}}$ needs the transmitter clock. (See 7.0)
CR04	DMA TEST	Selects DMA Test
CR05	RESTART	Resets Sequence numbers, etc.
CR06	0	Unused control bits, like CR06 must be left at 0.
CR07	PCR/$\overline{\text{BASIC}}$	This bit selects one of two error correction procedures. If CR07 = 0, the "basic" error correction method is employed which uses retransmission, positive acknowledge, and negative acknowledge. (See section 4.0) If CR07 = 1, the Preventive Cyclic Retransmission (PCR) error control method is used. PCR is essentially a noncompelled forward error correction method. (See section 5.0)

CONTROL REGISTER 1

Register	CR17	CR16	CR15	CR14	CR13	CR12	CR11	CR10
CR1	ACCEPT	SEND MSU	SEND LSSU	ADRV	0	0	0	SEND

BIT	NAME	DESCRIPTION
CR10	SEND	Used to command the WD2507 to transmit the next MSU. If SEND = 1, the WD2507 will read from the next TLOOK segment the value of RDY (See Figure 5). If RDY = 0, the WD2507 will clear SEND, and no transmission occurs. If RDY = 1, the WD2507 will then read TSADR and LIT from the TLOOK segment, and the buffer is transmitted. After transmission, the WD2507 will clear RDY of the segment just transmitted. If an MSU has been transmitted, the RDY of the next TLOOK segment is now read, and the procedure above is repeated. (See section 3.0) As a matter of good practice, the user's CPU should set SEND each time a new MSU is ready to transmit.
CR14	ADRV	The ADRV bit is the control for the 16 bit output addresses (A0-A15). If ADRV = 0, the outputs are three-state, and are in HI-Z, except when $\overline{DACK}$ goes low. If ADRV = 1, the outputs are always low impedance (TTL), and are high level $\overline{DACK}$ is high.
CR15	SEND LSSU	Start sending the LSSU in register SLSSU
CR16	SEND MSU	Start sending any available MSUs.
CR17	ACCEPT	Enable reception of MSUs and BSNR/FSNR checking for MSUs and FISUs.

INTERRUPT REGISTER

Register	IR07	IR06	IR05	IR04	IR03	IR02	IR01	IR00
IRO	MSUR	XMA	ATTN	X	LINK FAIL	X	X	X

Bf.	NAME	DESCRIPTION
IR00	X	Used internally; may be zero or one.
IR01	X	Used internally; may be zero or one.
IR02	X	Used internally; may be zero or one.
IR03	LINK FAIL	Link Failure: Reason encoded in SR02-SR00.
IR04	X	Used internally, may be zero or one.
IR05	ATTN	Attention Interrupt: reason encoded in IR01-IR03.
IR06	XMA	Transmitted MSU Acknowledged Interrupt
IR07	MSUR	MSU Received Interrupt: MSU was valid, FCS was good, FSN was equal to BSN + 1, and receive buffer was available. An Ack will be transmitted at the next respond opportunity.

STATUS REGISTER

Register	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
SR0	T1 OUT	$\overline{\text{IRTS}}$	REC IDLE	X	X	RLSSU/FAILURE		

BIT	NAME	DESCRIPTION
SR00-SR02	RLSSU/ FAILURE	Encoding depends on IR02 or IR03. If IR02 is set, the value is the LSSU type received: 000 O Out of Alignment 001 N Normal Alignment 010 E Emergency Alignment 011 OS Out of Service 100 PO Processor Outage 101 B Busy 110 – – 111 – – If IR03 is set, the link has failed for the following reason: 000 Reserved 001 BSNR Error 010 FIBR Error 011 SUERM Exceeded 100-111 (reserved)
SR03-SR04	X	Used internally, may be zero or one.
SR05	REC IDLE	At least 15 contiguous ones received. When one zero is received, REC IDLE is cleared and remains clear until 15 contiguous ones are received.
SR06	$\overline{\text{IRTS}}$	Internal Request To Send. When clear, chip is sending flags or SUs.
SR07	T1 OUT	Timer; used internally, may be zero or one.

SEND LSSU

Register	7	6	5	4	3	2	1	0
SLSSU	0	0	0	0	0	LSSU TYPE		

BIT	NAME	DESCRIPTION
0 - 2	SLSSU	Used in conjunction with SEND_LSSU (CR15 = 1) where: 000 O Out of Alignment 001 N Normal Alignment 010 E Emergency Alignment 011 OS Out of Service 100 PO Processor Outage 101 B Busy 110 – – 111 – –

TIMER REGISTERS

	7	6	5	4	3	2	1	0
TIMER	$T1_7$	$T1_6$	$T1_5$	$T1_4$	$T1_3$	$T1_2$	$T1_1$	$T1_0$
TIMER	$T5_5$	$T5_4$	$T5_3$	$T5_2$	$T5_1$	$T5_0$	$T1_9$	$T1_8$

BIT	DESCRIPTION
T9-T0	Registers 8 and 9 define a 10 bit value used for octet timing. The LSB is Register 8 bit 0. The MSB is Register 9, bit 1, where: $T1 = \frac{256\ N}{CLK}$ where: N = binary value in T9-T0 CLK = 2 MHz ± 5% These bits should be set by the user to the maximum period of silence allowed.
$T5_5$ - $T5_0$	The least significant bits of timer T5. The most significant bits are maintained in the user memory work area. The user must also set up T5_limit. The T5 counter (all 14 bits) counts once every time T1 expires. The timers are programmed by the user at initialization and maintained by the WD2507.

Note that the functional blocks covered by the WD2507 require three timers, T5, T6, and T7. T5 is a timer which is implemented inside the WD2507 to regulate how often SIB LSSUs are sent. The T6 and T7 timers must be implemented by the host. T6 should be started whenever a SIB is received and stopped whenever the XMA interrupt is seen. T7 should be started when a SIB is seen, when XMA interrupt is seen, when enqueuing a new transmit MSU or when changing SEND_MSU from cleared to set. T7 should be stopped when SEND_MSU is cleared or all transmit MSUs have been acknowledged. If either T6 or T7 expires it should be considered a link failure condition.

CONTROL BLOCK POINTER REGISTERS

CBPH	B_{15}	B_{14}	B_{13}	B_{12}	B_{11}	B_{10}	B_9	B_8
CBPL	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

BIT	DESCRIPTION
B15-B0	Registers A and B represent the 16 bit starting address of the 1056 byte control block which includes TLOOK, RLOOK, Error Counters, Timers and a work area. RLOOK and TLOOK each have 128 4 byte segments.

This control block must start on an even page boundary (100 hex)

CONTROL REGISTER 2

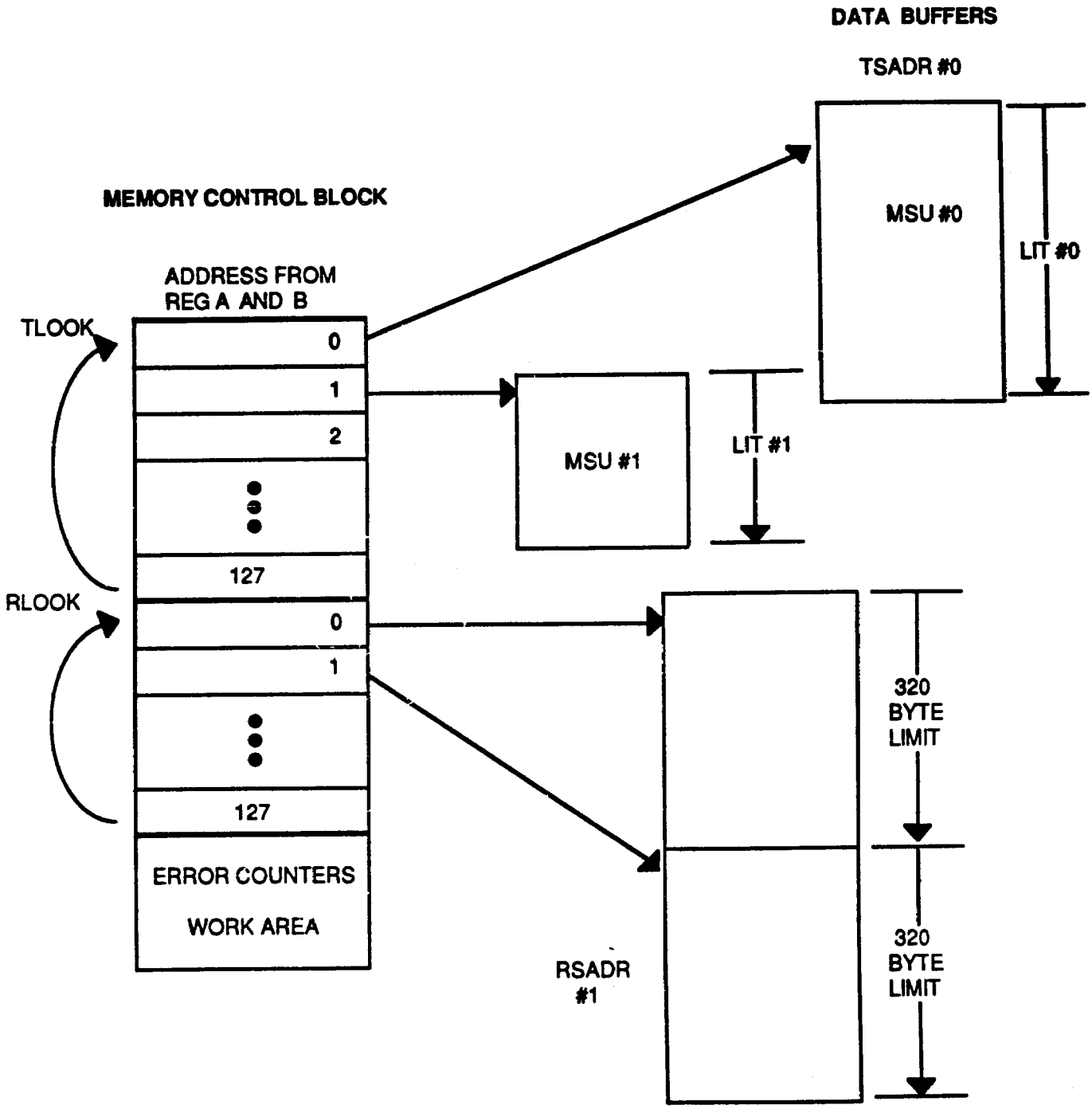
Register	CR27	CR26	CR25	CR24	CR23	CR22	CR21	CR20
CR2	0	0	0	0	FISU INT	BUSY NAK	ALIGN	TMROFF

BIT	NAME	DESCRIPTION
CR20	TMROFF	Disables all internal timers (for test)
CR21	ALIGN	Controls behavior of error rate monitors
CR22	BUSY NAK	Enables sending of NACKs when busy
CR23	FISU INT	Generate MSUR interrupt upon receipt of FISU

An option to allow NACKs to be sent when in the busy (no receive buffers available) state has been implemented. While the standard does not indicate that NACKs should be sent while MSUs are being dropped due to lack of receive buffers, some implementations require an option to be able to send these NACKs. Setting BUSYNAK in CR2 enables this option.

There is one Error Rate Monitor located at offset 11 (0bH) of the work area of the control block. This monitor serves as either the AERM or the SUERM depending on the state of the ALIGNMENT bit of CR2. Setting this bit causes the monitor to be the AERM. The limit for when the monitor is acting as the SUERM is now located at offset 12 (0cH) of the work RAM.

During Initial Alignment the WD2507 will optionally report whenever a good FISU or MSU is received. There is an option to get an MSUR interrupt whenever any good FISU or MSU is received based on FISU INT. The host system must check the RLOOK table to determine if this interrupt indicated an expected new MSU as opposed to other MSUs or FISUs. If the next RLOOK entry is not posted complete, then it must be one of the later. This extended use of MSUR may be disabled by clearing bit 3 in register CR2. Disabling this feature will prevent excessive interrupts when the host is no longer in the Initial Alignment phase.



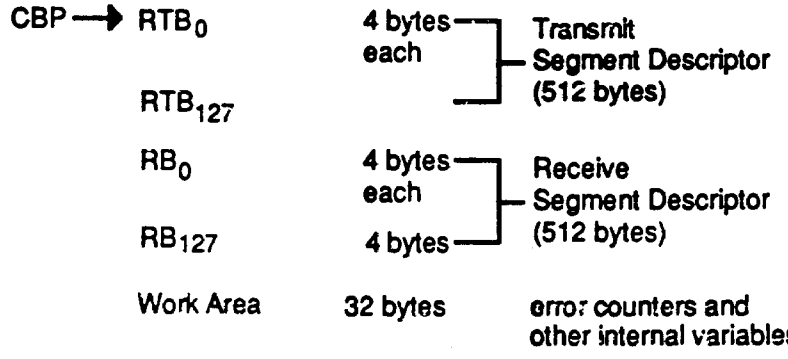
NOTES: All RAM in the figure is external to the WD2507

Figure 4: MEMORY ACCESS METHOD

3.0 TRANSMITTING AND RECEIVING PROCEDURES

Figure 3 notes that the SIO and SIF fields of MSUs are DMA accessed. The DMA is part of the WD2507's memory access method as seen in Figure 4.

CBPH and CBPL (registers A and B) are used to tell the WD2507 the address in external RAM of a data structure used to access transmit and receive buffers as well as other miscellaneous locations. This structure, as a whole, is called the "Control Block". The Control Block is 1056 bytes long and may be located anywhere in the 64K byte WD2507 address space. The following is the overall structure of the control block.



Each Retransmission Buffer (RTB) and Receive Buffer (RB) Descriptor has the format shown in Figure 5.

3.1 TRANSMITTING MSU's

Figure 5 shows the segment descriptors used by the WD2507.

RDY is set in an RTB discriptor by the host when the buffer pointed to by ADDR_HI:ADDR_LO points to an MSU which is ready to be sent. The length of the data buffer to be sent is specified by the nine bits LEN_HI:LEN_LO. When the MSU has been sent and then acknowledged, the WD2507 will clear RDY and set ACKED. The length of an MSU data buffer may not exceed 320 bytes. Even though nine bits are used to specify the buffer length, the WD2507 follows the CCITT specification and will send a length indicator (LI) field of 3F hex if the actual length is 3F hex or greater.

Bits 6 and 7 of the LI byte may be assigned by the host by programming bits in the appropriate TLOOK Control word.

There is no arbitrary length queue of new MSU's like the Transmit Buffer (TB) described in the CCITT #7 specification. Instead the host is responsible for putting new MSU's directly in the ReTransmission Buffer (RTB). The host must keep an index into the RTB in the Control Block for the next MSU to be acknowledged (FSNF) and one for the most recently enqueued MSU (FSNL). The host should also keep a count of the total number of MSU's and the corresponding total byte count of all MSU's which have been enqueued but not yet acknowledged. CCITT #7 specifies two limits N1 and N2 for the total number of outstanding MSU's and their total byte counts respectively. The host should not enqueue new MSU's when the outstanding MSU's exceed these limits. The following steps should be followed to add new MSU's.

1) Increment the outstanding MSU count and the outstanding byte count.
2) If the outstanding counts exceed the limits N1 or N2, then wait for sufficient acknowledgements to reduce the outstanding counts to within the limits. The host must continue to monitor received MSU's, LSSU's, and acknowledgements.
3) Once able to proceed, the host should increment FSNL (index to most recently enqueued MSU).
4) The host should write the address of the buffer to send to the ADDR_HI:ADDR_LO bytes in the RTB(FSNL) segment of the Control Block, described above.

5) The LEN_HI bit and the LEN_LO byte should be set to the length of the buffer to be sent.

6) The ACKED bit of byte 0 of RTB(FSNL:) should be cleared and the RDY bit should be set.

7) Finally, the SEND bit in register CR1 should be set.

It should be noted that no MSU's will be sent unless the SEND_MSU bit in CR1 is set and the SEND_LSSU bit in CR1 is cleared. Once the MSU is put in the RTB, the WD2507 will send the MSU automatically. The host should be alert for an XMA interrupt from the WD2507. This interrupt may indicate that one or more MSU's starting with the one at FSNF, have been acknowledged. Acknowledgement is indicated by the ACKED bit in the MSU's RTB segment being set.

The XMA interrupt may also be set without any ACKED bit being set. This case corresponds to a NACK being received. This latter case is for use by the host to stop its T6 timer which may have been started by a received SIB LSSU. The T6 timer should be stopped whenever XMA is set.

3.2 RECEIVING MSU'S

RDY is set in the RB discriptor by the host when the buffer pointed to by ADDR_HI:ADDR_LO points to a buffer ready to receive data. The length of the data buffer received will be placed in the nine bits LEN_HI:LEN_LO by the WD2507. New MSUs will be indicated to the host by simultaneously clearing RDY and setting MRCVD. The LEN_HI:LEN_LO fields will reflect the true length of the MSU even if this number exceeds 3F hex.

Once the bits RECVON in CR0 and ACCEPT in CR0 are set and Receive Buffers (RB) are available, the WD2507 will write to memory any MSUs received with the proper Forward Sequence Number. The host should keep an index (FSNX) into the RB table in the Control Block at the position where a new MSU will next be placed. When an MSU is received, the WD2507 will fill the buffer pointed to by the RB(FNSX) and write the length into the length field. The MRCVD bit of byte zero of the RB(FSNX) segment will be set to indicate a new MSU is available to the host. The MSUR interrupt bit in IRO will be set to let the host know at least one RB segment has a new MSU. Once the host is done using the RB segment and its buffer, the MSUR bit should be cleared and the RDY bit set to make the segment available for future MSU's. If the WD2507 receives an MSU and no free RB segments exist, then an SIB (busy) LSSU will automatically be sent at a user defined interval based on T5. This busy signal will keep the other side of the link from closing down due to a lack of acknowledgements from this side of the link.

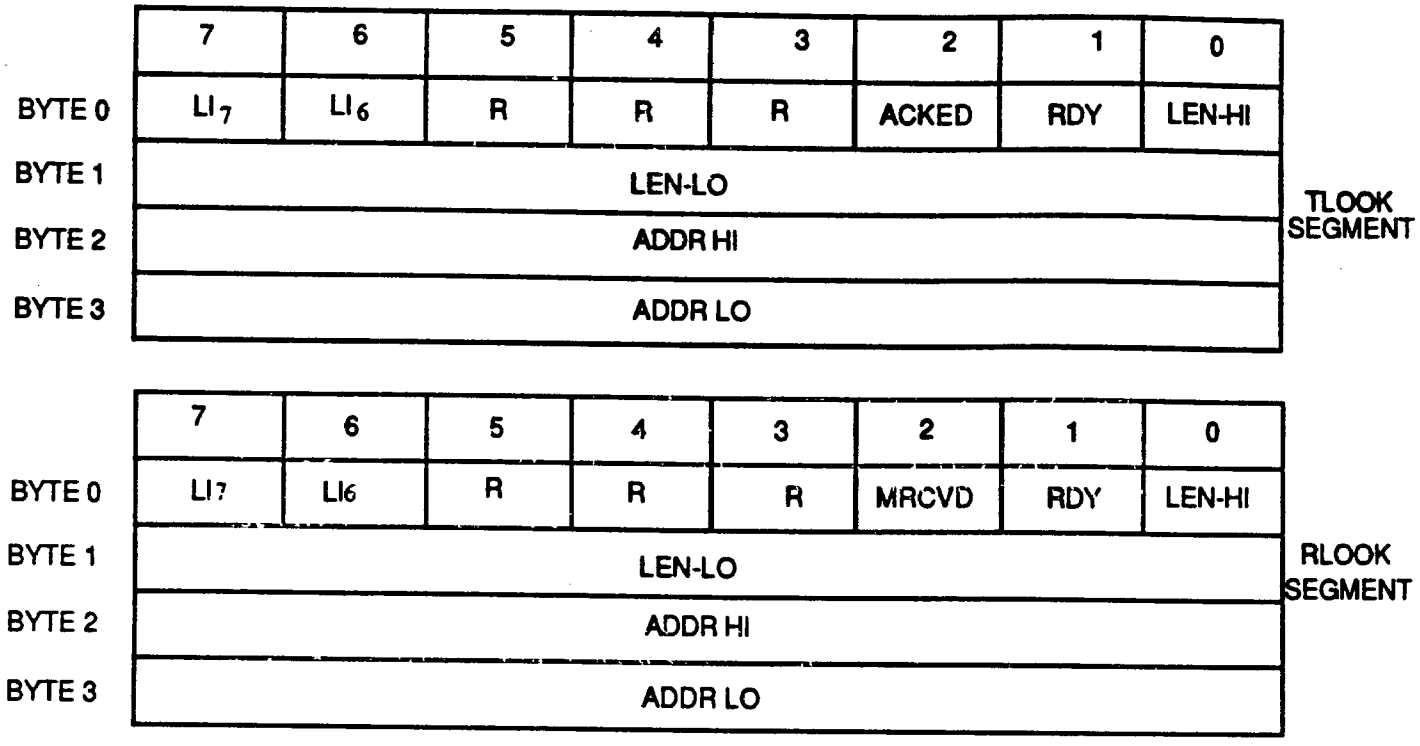
3.3 DEADLY EMBRACE PREVENTION

A "deadly embrace" is defined here as a state where the host and the WD2507 are both waiting for an action from the other. This situation could exist unless control bits shared by the WD2507 and the host are handled properly. A shared control bit is defined as one which is either set by the host and cleared by the WD2507, or is set by WD2507 and cleared by the host. They must not both be allowed to set or clear the same bit. The shared control bits are:

BIT NAME	WHERE FOUND	SET BY	CLEARED BY
SEND	CRI0	Host	WD2507
RDY	each TLOOK segment	Host	WD2507
ACKED	each TLOOK segment	WD2507	Host
RDY	each RLOOK segment	Host	WD2507
MRCVD	each RLOOK segment	WD2507	Host

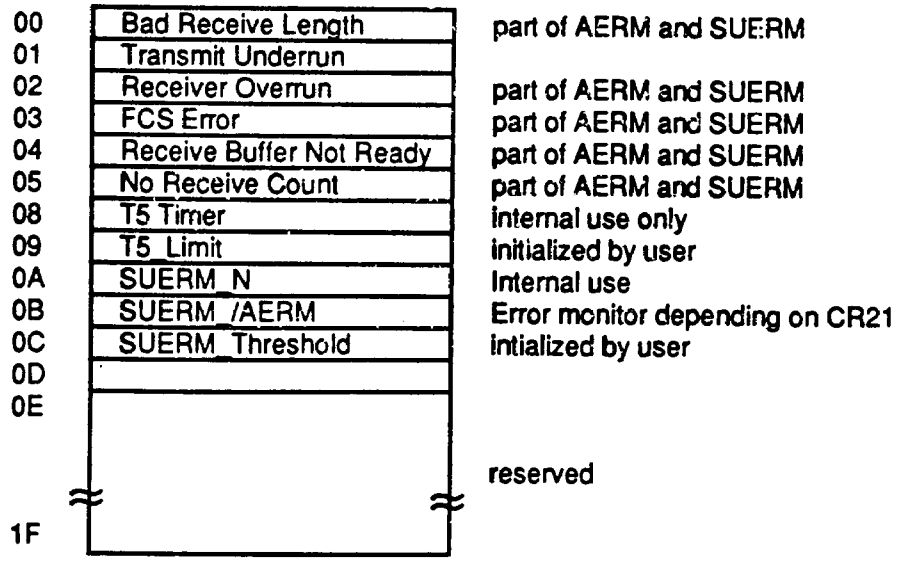
Any of these bits may be set to any value by the host at initialization. After initialization, the deadly embrace rule takes effect.

Figure 5: SEGMENT DESCRIPTORS



NOTE: R = Reserved for furture use. Program to 0

Figure 6: ERROR COUNTERS & WORK AREA OFFSET FROM CBP



3.4 SENDING LSSU's

The WD2507 may be setup to automatically send an LSSU repetitively until instructed to do other wise. The type of the LSSU is passed to the WD2507 in the lower three bits of SLSSU (register number E). The SEND_LSSU bit in CR1 is then set by the host. The WD2507 will honor this bit over the SEND_MSU bit. The user should clear the SEND_MSU bit when setting SEND-LSSU. To change the value of new LSSU's, the host changes the value in the SLSSU register. To stop sending LSSU's the host clears the SEND_LSSU bit in CR1. SEND_MSU should be set again if there are more MSU's are to be sent. It should be noted that the WD2507 will automatically send SIB (busy) LSSU's periodically based on the value in T5 if receiver congestion is noted (no free receive buffers available).

All LSSU's are sent with the LI field set to one by the WD2507.

3.5 RECEIVING LSSU's

When an LSSU is received, its type is placed in the lower three bits of register SR0. The ATTN bit and RXLSSU bits in IR0 will be set when an LSSU is received. Setting ATTN causes an interrupt to be generated to the host. Reading the IR0 register will clear the ATTN bit. In this way detection of additional LSSU's is possible. While the WD2507 will send SIB LSSU's automatically, the host must still monitor the reception of these LSSU's; SIB reception indicates the host should start its T6 timer. The LI is not compared to the actual received byte count by the WD2507.

3.6 ERRORS

Errors of interest to the host are reported in two ways. Non-critical errors (where automatically retries may help) are reported by incrementing counters in the Control Block. A critical error results in a link failure interrupt to the host.

The WD2507 maintains a set of error counters in user memory, following TLOOK and RLOOK. The errors that are monitored are as follows:

Bad receive length
Transmit Underrun (TUR)
Receiver Overrun (ROR)
FCS error or Abort Received
Receive Buffer Not Ready
No Receive Count
Alignment Error Rate Monitor
Signal Unit Error Rate Monitor

Regarding the TUR and ROR errors: an ROR means that the receiver Register (RR) had a byte to load into the receiver FIFO, but the FIFO was full. TUR means that the Transmitting Register (TR) needed a byte from the Transmitter Holding Register (THR), but the THR was empty. Either TUR or ROR may be caused by one of two conditions, or both.

1) The bit rate clock, TC or RC, is too fast for the WD2507.
2) The DACK response is too slow for the bit rate.

The Signal Unit Error Rate Monitor (SUERM) counter will count up when a number of receive errors have occured; it will also count down when a sufficient number of good signal units have been received with no errors between them. When the SUERM reaches a user defined limit a link failure will result. (SEURM_N for down; SEURM_T for limit.) The WD2507 increments the appropriate counter upon detection of an error. The user should periodically scan these error counters and take appropriate action.

Link failures are errors indicating the link is too poor to use. Link failures can come from the following events.

1) Two bad BSNR values within three consecutive receive frames.
2) Two bad FIBR values within three consecutive receive frames.
3) The SUERM exceeding a user defined limit.

The cause of a link failure can be found in the lower three bits of register SR0 when LINK-FAIL is set (IR03=1). When a link failure occurs the receiver will be disabled. The transmitter will continue to send FISU's until the host takes some action. When a Link down occurs, the host has two choices: RESTART or INACTIVATE the chip. The host should set the appropriate bit (CR05 or CR00), wait for LINK FAIL (IR03) to clear, then clear CR05/CR00.

3.7 WD2507 WORK AREA

Following TLOOK, RLOOK, and the Error Counters is an additional block of memory used by the WD2507 for additional host programmed parameters and temporary work storage.

For example, the most significant bits of the T5 timer can be found here (the least significant bits are in the Timer Registers). The SUREM limit and SIB time interval are also maintained in this area.

3.8 INITIALIZATION PROCEDURE

After power up the WD2507 will be in an inactive state -- nothing (including FISU's) will be sent and everything received will be ignored. From this state self diagnostics such as an internal register test may be selected or the WD2507 may be commanded into "active" state.

Initialization begins after either the INACTIVE (CR00) bit is cleared after having been set, or after the RESTART (CR04) bit is cleared after having been set. The latter causes initialization only if the WD2507 was already active.

At initialization, transmitted FSN's and BSN's are all 1's. Transmitted FIB's and BIB's are 1. The first transmitted MSU will have FSN=0 and the expected value of the FSN of the first received MSU will be 0.

As long as the chip is active, it will always be transmitting either FISU's, LSSU's, or MSU's. There is never more than 1 flag separating two signal units in the current WD2507. Future revisions will allow the user to select the number of flags, up to a maximum of 15.

3.9 DEFINITION OF CORRECT LI

The LI field is found in each SU as the lower 6 bits in the third byte following the leading flag. LI is the byte count for the length of the SU. The length of the SU is the number of bytes following the LI field, but preceding the FCS.

For an FISU, LI=0, and a correct LI means that the FCS field will immediately follow the LI field. For an LSSU, LI=1 or 2, and a correct LI means that there are 1 or 2 bytes in the SF field (corresponding to LI).

A correct LI for an MSU will meet either one of two conditions:

1) For MSU's with lengths from 3 to 63, the LI must equal the number of bytes in the length of the MSU.

2) For MSU's which are 63 bytes, or longer, the LI will be maintained at a value of 63 (six 1's).

4.0 "BASIC" ERROR CORRECTION METHOD

In the basic method, previously transmitted, but unacknowledged, MSU's are not retransmitted unless a NACK (Negative ACKnowledge) is received. The WD2507 will employ this procedure when PCR is cleared (CR07-0).

A NACK is defined as an SU with the BIB inverted from the previously transmitted SU. When the WD2507 receives a NACK, the WD2507 will begin retransmission of MSU's with the transmitted FSN equal to the received BSN plus one, and the transmitted FIB equal to the received BIB. However, if the received NACK refers to an FSN not in the retransmission buffer, the NACK is discarded but the next transmitted FIB will still be made equal to the received BIB. If 2 out of 3 consecutively received BSN's reference FSN's of MSU's not in the retransmission buffer, LINK_FAIL is set and an ATTN interrupt is generated.

When a valid NACK is received, the WD2507 will begin sequential retransmission starting with the oldest MSU even if there are new MSU's ready.

A received NACK may also acknowledge one, or more, previously transmitted MSU's.

All previously transmitted MSU's may be acknowledged by a received NACK. In this case, a received NACK will have cleared the retransmission buffer. This is an acceptable condition and the acknowledgements are accepted. The FIBT is inverted. However, there will be no retransmission of MSU's.

The retransmission buffer is defined as those MSU's awaiting acknowledgement from FSNF to FSNL.

In BASIC mode, retransmission will not begin unless a NACK is received.

If the WD2507 receives an MSU with an FSN not equal to the BSNT +1, or if an FISU or LSSU is received with an FSN not equal to BSNT, the WD2507 will transmit a NACK.

5.0 ERROR CORRECTION BY PREVENTIVE CYCLIC RETRANSMISSION (PCR)

In the PCR procedure, previously transmitted, but unacknowledged, MSU's are sequentially retransmitted whenever there are no new MSU's or LSSU's to transmit. This procedure is employed if PCR is set (CR07=1).

The absence of new MSU's or LSSU's is determined if the RDY bit of the next TLOOK segment is 0; if there are no new MSU's or LSSU's to transmit, and if the retransmission buffer is not empty, the WD2507 will begin retransmission with the oldest MSU. If there are no new MSU's or LSSU's, and if the retransmission buffer is empty, the WD2507 will transmit continuous FISU's.

PCR does not require a NACK to be received before beginning retransmission. In PCR mode, only BSN values are checked to ACK SUs; BIBRs are ignored.

The host must determine when the maximum number of bytes available for retransmission (N2) has been reached. N2, measured in bytes, is the total of the lengths of the MSU's in the retransmission buffer. When N2 is reached, the host must not allow new MSU's to be transmitted by insuring that the RDY bit of those new MSU's is zero. However, new LSSU's may be transmitted. When the host has determined that new MSU's may be transmitted (because some of the retransmission buffer has been removed by received acknowledgements), then the host may add new MSU's.

6.0 SUMMARY OF CONDITIONS FOR TRANSMISSION

No SUs will be transmitted until INACTIVE (CR00) is 0 and CTS (pin 22) is low. Given these conditions, the WD2507 will always be transmitting SU's. If there are no MSUs nor LSSUs to send, the WD2507 will send FISUs.

The following conditions require that INACTIVE = 0 and that CTS is low. In the following paragraphs, the following conventions are used: X means "don't care." (N) refers to the applicable TLOOK segment.

CONDITIONS FOR SENDING AN LSSU

SEND = 1 (CR10)
CR07 = X
SEND_LSSU = 1 (CR15)
SLSSU - LSSU TYPE

CONDITIONS FOR SENDING AN FISU

Either condition A or B below will cause an FISU to be transmitted.

A. "Basic" procedure selected, no new MSU's nor LSSU's ready for transmission, and no retransmission in progress.
B. PCR procedure selected, no new MSUs nor LSSUs ready for transmission, and the reransmission buffe r is empty.

SEND = 0
CR07 = 1
FSNT + 1 = FSNO

CONDITIONS FOR SENDING AN MSU FOR THE FIRST TIME

In either Basic or PCR, the conditions below will cause an MSU to be transmitted for the first time. After the transmission is complete, RDY (N) is cleared to 0. FSN is incremented prior to the transmission of that MSU.

SEND = 1
CR07 = 0
RDY(N) = 1
LIR(N)>2
There are less than 127 outstanding MSU's

CONDITIONS FOR RETRANSMITTING AN MSU

Retransmission of one or more MSUs will occur whenever conditions A, B or C below are met. MSUs are sequentially retransmitted beginning with FSNO.

A. NACK received with received BSN greater than equal to FSNO, but less than FSNT. Notice that this conditions requires that the retransmission buffer is not empty. (The retransmission buffer is empty when FSNT + 1 = FSNO).
B. PCR procedure, no new MSUs nor LSSUs ready, and etransmission buffer not empty.
C. PCR procedure, and there are 127 outstanding MSU's.

7.0 SELF TESTS

There are three self tests: 1) An internal RAM test, 2) A loop-back test, and, 3) a DMA test. These tests are suitable for manufacturing testing, user incoming inspection testing, diagnostics, and trouble-shooting.

7.1 INTERNAL RAM TEST

There are eleven 8-bit registers in the WD2507 which are not directly accessible by the user's CPU. Four of these cannot be completely tested by using loop-back. Therefore, this test was created as a means to test those four internal registers. The contents of Register A are placed in two even internal registers, and the contents of Register B are placed in two odd internal registers. The four registers are then added together, without carry, and the results are placed in Registers 2, 5, 6, and 7. This test is initiated when RAMT (CR02) is set to 1 provided INACTIVE (CR00) is also set to 1. Use the following procedure:

1. Insure INACTIVE=1
2. Set RAMT
3. Set-Up Registers A and B
4. Wait at least 150 times the CLK period
5. Check the results in Registers 2, 5, 6, and 7

To repeat the test for new values in Registers A and B:

6. Clear RAMT
7. Wait at least 120 times the CLK period
8. Go back to step 1

7.2 LOOP-BACK TEST

The internal loop-back condition exists whenever CR03=1. TD is tied back to RD and TC is tied to RC. The imputs, RD and RC are gated-out, but the TD output is still present.

When running this test, it is recommended that MSU's be transmitted and received and the SIO and SIF fields be checked. The transmitted and received SIO and SIF fields should be identical. When this is done, the entire DMA and buffer management is tested as well as the transmitter and receiver.

LSSU's may also be transmitted and received in loop-back.

7.3 DMA TEST

This test verifies proper operation of the DMA sub-system by reading the value from a register and writing it into the user memory. The test continues by reading the value from the same location in memory and writing it into another register.

The value is read from register C. Using the transmitter DMA sub-system, it is written into memory location addressed by register A and B (location N; register A is the MSB). The receiver DMA sub-system is used and contents of the same address is read and it is stored into register 7. Next the receiver DMA is used and the contents from register D is written into location N + 1. The transmitter DMA reads the value from location N + 1 and stores it into register 6.

It is the host's responsibility to check if the contents of registers C and register 7 and memory location N match. The same is true for registers D and 6 and memory location N + 1.

8.0 GLOSSARY OF TERMS

ACK	Positive ACKnowledgementAERM Alignment error rate monitor
BASIC	The "basic" error correction method
BIB	Backward Indicator Bit (1 bit)
BIBR	BIB received
BIBT	BIB to be transmitted
BIBX	BIB expected
BSN	Backward Sequence Number (7 bits)
BSNT	BSN to be transmitted
CC	Congestion control
DAEDR	Delimitation, alignment and error detection (receiving)
DAEDT	Delimitation, alignment and error detection (transmitting)
F	Flag
FCS	Frame Check Sequence
FIB	Forward Indicator Bit (1 bit)
FIBR	FIB received
FIBT	FIB to be transmitted
FIBX	FIB expected
FISU	Fill In Signal Unit (L=0)
FSN	Forward Sequence Number (7 bits)
FSNC	Forward sequence number of last message signal unit accepted by remote level 2
FSNF	FSN of the oldest MSU in the RTB
FSNL	FSN of the last MSU in the RTB
FSNO	FSN of next transmitted MSU to acknowledged (Also called FSN of oldest MSU in retransmission buffer)
FSNR	FSN received
FSNT	FSN of the last MSU transmitted
FSNX	FSN expected
IAC	Initial Alignment Control
L2	Level 2
L3	Level 3
LI	Length Indicator (1 byte field)
LSC	Link State Control
LSSU	Link Status Signal Unit (L=1 or 2)
MGMT	Management system - Unspecified implementation dependent management function
MSU	Message Signal Unit (L>2)
N	Corect SU count
N1	Maximum number of time slots which are available for retransmission (fixed by the numbering capacity of the FSN)
N2	Maximum number of MSU octets which are available for retransmission (fixed by the common channel loop delay time).
NACK	Negative ACKnowledgement
NMAX	The number of bytes available for retransmission
PCR	Preventive Cyclic Retransmission (one of two error correction methods)
POC	Processor Outage Control
RC	Reception Control
RTB	Retransmission buffer
RTR	If = 1 means retransmission expected
SF	Status Field (1 or 2 byte field in an LSSU)
SIB	Status Indication "B" ("Busy")
SIE	Status indication "E" ("emergency alignment")
SIF	Signalling Information Field (2 or more byte field in an MSU)
SIN	Status indication "N" ("normal alignment")
SIO	Service Indicator Octet (1 byte field in an MSU)
SIOS	Status indication "OS" ("out of service")
SIPO	Status indication "PO" ("processor outage")
SU	Signal Unit (may be FISU, LSSU, or MSU)
SU length	The number of bytes in an SU after the LI field, but before the FCS.

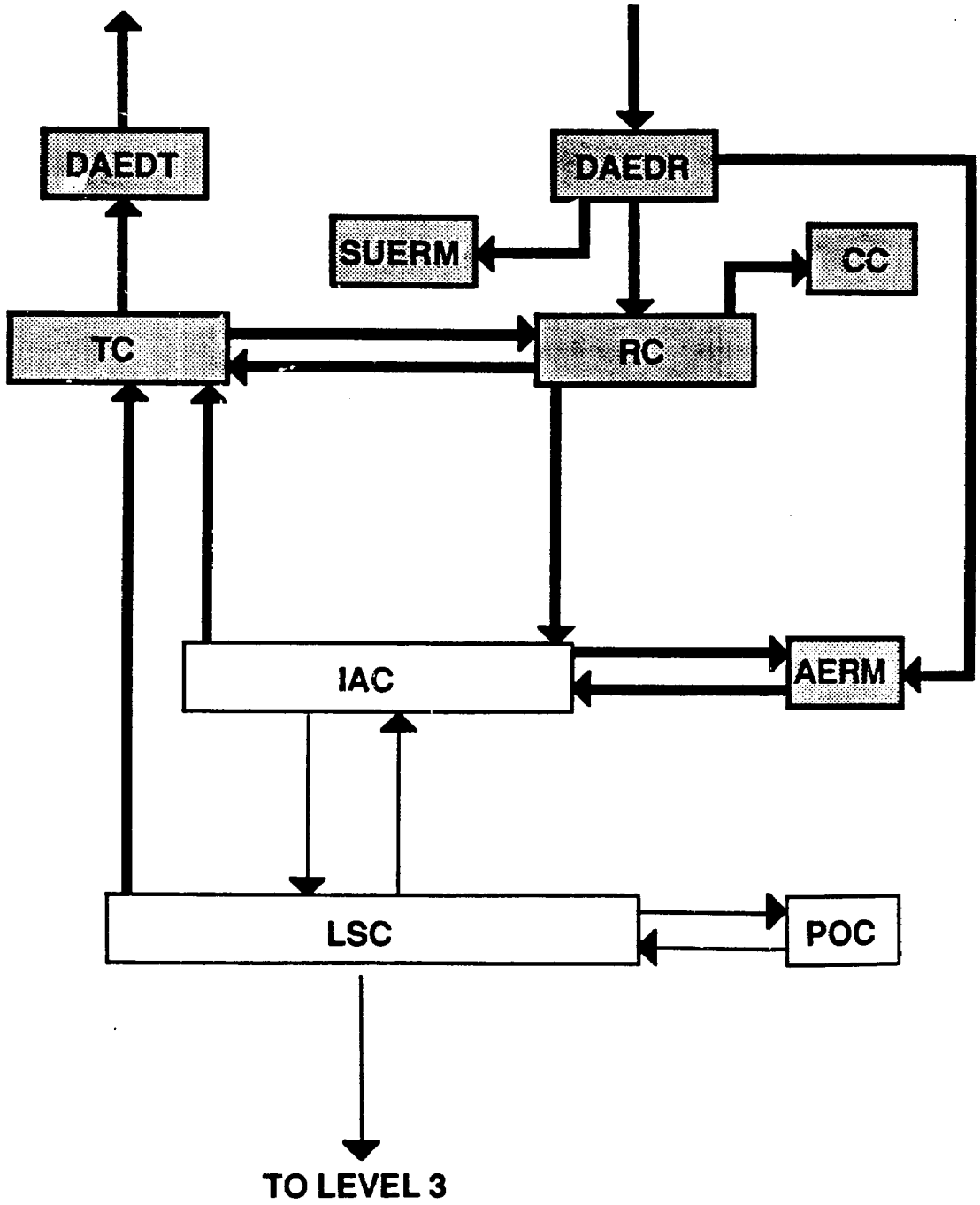
SUERM	Signal Unit Error Rate Monitor
T	SUERM threshold
TB	Transmission Buffer
TXC	Transmission control
UNB	Counter of unreasonable BSN
UNF	Counter of unreasonable FIB
Ti	AERM threshold
Tie	Emergency AERM threshold
Tin	Normal AERM threshold
Z	Pointer to sequence number of next MSU to be retransmitted in transmission code

Timers used in Q.703

T1	Timer "alignment ready"
T2	Timer "not aligned"
T3	Timer "aligned"
T4	Proving period timer = 2^{16} or 2^{12} octet transmission time
T5	Time between sending SIBs.
T6	Timer "remote congestion"
T7	Timer "excesive delay of acknowledgement
PE	Emergency proving period
PN	Normal proving period

Figure 7:

Q.703 SIGNALLING LINK FUNCTIONAL BLOCK DIAGRAM



* Shaded areas handled by WD2507

Figure 8:

SIGNALLING SYSTEM #7 LAYERED ARCHITECTURE

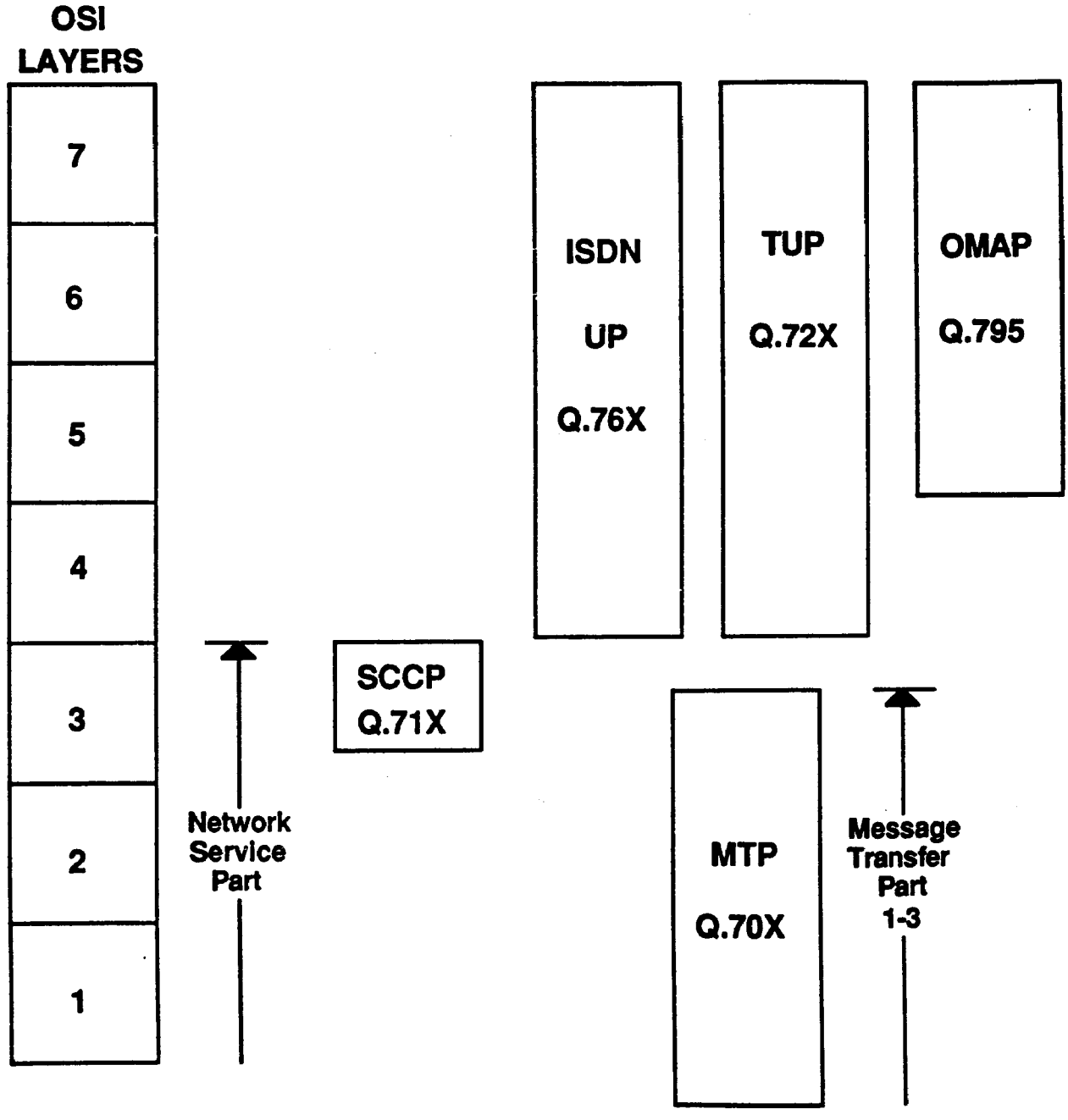


Table 2:

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	CONDITIONS
CLK	Clock Frequency	1.9	2.0	2.1	MHz	Clock must have 50% duty cycle
RC	Receive Clock Range	0		64	KHz	
TC	Transmit Clock Range	0		64	KHz	
MR	Master Reset Pulse Width	1.0			mS	
T_{AR}	Input Address Valid to RE	0			nS	
T_{RD}	Read Strobe (or DACK Read) to Data Valid	2		375	nS	C(load) = 100pf
T_{HD}	Data Hold Time From Read to Strobe	20		100	nS	
T_{HA}	Address Hold Time From Read Strobe	80			nS	
T_{AW}	Input Address Valid to Trailing Edge of WE	100			nS	
T_{WW}	Minimum WE Pulse Width	200			nS	
T_{DW}	Data Valid to trailing Edge of WE or Trailing Edge of DACK for DMA Write	100			nS	
T_{AHW}	Address Hold Time After WE	80			nS	
T_{DHW}	Data Hold Time After WE or After DACK for DMA Write	100			nS	
T_{DA1}	Time from DRQO (or DRQI) to Output Address Valid if ADRV = 1			80	nS	
T_{DA0}	Time From DACK to Output Address Valid if ADRV = 1			375	nS	C(load) = 100pf
T_{DD}	Time From Leading Edge of DACK to Trailing Edge of DRQO (or DRQI)			375	nS	C(load) = 100pf
T_{DAH}	Output Address Hold Time From DACK	20		125	nS	
T_{DMW}	Data Hold Time From DACK for DMA Read	20		125	nS	
T_{RP1}	REPLY Response Time (leading edge)			240	nS	C(load) = 100pf
T_{RP2}	REPLY Response Time (trailing edge)			260	nS	C(load) = 100pf

9.0 WD2507 ELECTRICAL SPECIFICATIONS:

ABSOLUTE MAXIMUM RATINGS:

Voltages referenced to V_{SS}

High Supply Voltage (V_{DD}) ..... - 0.3 to 15V
Voltage at any Pin..... ..... - .03 to 15 V
Operating Temperature Range..... .....0° C to + 70° C
Storage Temperature Range..... -15° C to + 125° C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions spe cified in the DC Electrical characteristics.

Figure 7: Operating Characteristics:

V_{SS} = 0V, V_{CC} = 5.0V ±.25, V_{SS} =12.0V ±.6VT A = 0° to 70°

SYMBOL	PARAMETER	MIN.	TYP	MAX	UNIT	CONDITIONS
I_{DD}	V_{DD} Supply Current		20	70	mA	
I_{CC}	V_{CC} Supply Current		200	280	mA	
V_{DD}	High Voltage Supply	11.4	12	12.6	V	
V_{CC}	Low Voltage Supply	4.75	5	5.25	V	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	I_O = -0.1mA
V_{OH}	Output High voltage	2.8			V	I_O = 1.6mA
V_{OL}	Output Low Voltage			0.4	V	↓
I_{LH}	Input Leagage Source or Sink			10	uA	
I_{OZH}	Input Leakage High Impedance			10	uA	Vin = V_{CC}
I_{OZL}	Output Leakage High Impedance			10	uA	Vin = V_{SS}