HARRIS

HI-5660/5660A

High Speed Monolithic Digital-to-Analog Converter

T-51-09-12

Features

- MONOLITHIC CONSTRUCTION
- FAST SETTLING (TO ±1/2 LSB) 500ns
- ±1/2 LSB MAX. NONLINEARITY GUARANTEED OVER TEMPERATURE
- INTERNAL CANCELLATION OF GROUND CURRENT
- EXCELLENT POWER SUPPLY REJECTION 1ppm/%PS
- LOW COST

Applications

- HIGH SPEED A/D CONVERTERS
- CRT DISPLAYS
- WAVEFORM SYNTHESIS

Description

The HI-5660 is a current output, 12 bit monolithic digital-to-analog converter. It offers high speed plus enhanced accuracy, through internal cancellation of ground currents.

Fabrication of the HI-5660 features the Harris bipolar dielectric isolation process, which eliminates latchup and minimizes parasitic capacitance and leakage currents. The chip includes nichrome thin-film resistors, laser trimmed at the wafer level to a maximum linearity error of ±1/4 LSB at +25°C.

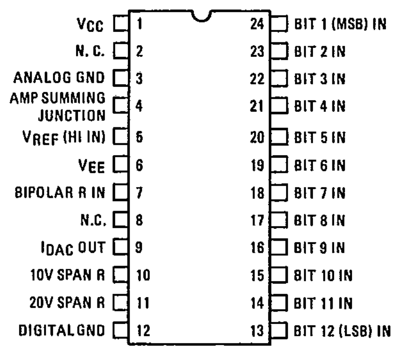
Near zero current in the Analog Ground terminal simplifies use of the HI-5660 by minimizing noise and offsets between the package and the system analog ground. This is accomplished by adding a complement current to the internal ground from an auxiliary R-2R ladder, and then supplying the resultant DC current from the positive power supply.

Electrical performance is similar to that of the AD566A. Pinouts are identical except for pin 1, which requires a +5V supply (versus no connection on the AD566A).

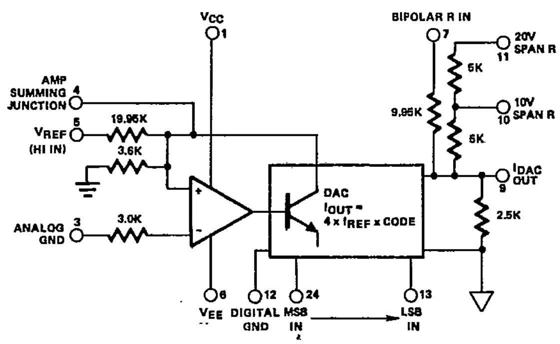
The HI-5660 is offered in two accuracy grades each for the commercial and military temperature ranges. Package is a 24 pin ceramic DIP, and power requirements are ± 12V to +15V.

Pinout

TOP VIEW
24 LEAD DIP



Functional Diagram



Absolute Maximum Ratings †

V_{CC} to Power Ground	0V to +18V	10V Span R to Reference Ground	±12V
V_{EE} to Power Ground	0V to -18V	20V Span R to Reference Ground	±24V
Voltage on DAC Output (Pin 9)	-3V to +12V	Junction Temperature	175°C
Digital Inputs (Pins 13-24) to Power Ground	-1V to +7.0V	Operating Temperature Ranges	
Ref In to Reference Ground	±12V	HI-5660/A-2,-8	-55°C to +125°C
		HI-5660/A-5	0°C to +75°C
Bipolar Offset to Reference Ground	±12V	Storage Temperature Range	-65°C to +150°C

†Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, V_{REF} = 10V, unless otherwise specified)

MODEL	HI-5660-5			HI-5660A-5			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX}) Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	µA
Bit OFF Logic "0"		-10	-50		-10	-50	µA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	0.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of FS
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With 50Ω External Load		500			500		ns

MODEL	HI-5660-5			HI-5660A-5			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE							
Operating	0		+75	0		+75	°C
Storage	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +4.5 to +16.5V_{DC} ; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC} ; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Zero Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Zero Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW
MULTIPLYING MODE PERFORMANCE (All Models)							
Quadrants	Two (2): Bipolar Operation at Digital Input Only.						
Reference Voltage	Unipolar: +10V Max, +2V Min.						
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.						
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical						
Output Slew Rate 10%-90%	1.3mA/µs						
Output Slew Rate 90%-10%	1.3mA/µs						
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5µs to 0.01% F.S.						
CONTROL AMPLIFIER							
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:
1. The Digital Input Levels are Guaranteed but not Over the Temperature Range.
2. See Settling Time Section.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified.)

MODEL	HI-5660-2, HI-5660-8			HI-5660A-2, HI-5660A-8			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	2.0		5.5	2.0		5.5	V
Bit OFF Logic "0"	0.0		0.8	0.0		0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		2	10		2	10	μA
Bit OFF Logic "0"		-10	-50		-10	-50	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	2.0K	2.5K	3.0K	2.0K	2.5K	3.0K	Ω
Offset Unipolar		.01	.05		.01	.05	% of FS
Bipolar (Figure 2, R_3 = 50Ω Fixed)		.05	.15		.05	.10	% of FS
Capacitance		25			25		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-3		+12	-3		+12	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of FS
T_{MIN} to T_{MAX}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of FS
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED (±1 LSB MAX)						
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		7	10	ppm/°C
Differential Nonlinearity		2	6		2	2	ppm/°C
SETTLING TIME TO 1/2 LSB							
With 50Ω External Load		500			500		ns

MODEL	HI-5660-2, HI-5660-8 MIN	TYP	MAX	HI-5660A-2, HI-5660A-8 MIN	TYP	MAX	UNITS
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +4.5V to +16.5V_{DC}		7	12		7	12	mA
V_{EE}, -11.4 to -16.5V_{DC}		-13	-17		-13	-17	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC} = +4.5 to +16.5V_{DC}; V_{EE} = -15V		1	10		1	10	ppm of FS/%
V_{EE} = -11.4 to -16.5V_{DC}; V_{CC} = +15V		1	10		1	10	ppm of FS/%
PROGRAMMABLE OUTPUT RANGES (See Table 1)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R_2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of FS
Bipolar Offset Error with Fixed 50Ω Resistor for R_3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of FS
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of FS
Bipolar Offset Adjustment Range (Fig. 2)	±0.15			±0.15			% of FS
REFERENCE INPUT							
Input Impedance	16K	20K	24K	16K	20K	24K	Ω
POWER DISSIPATION		230	330		230	330	mW

MULTIPLYING MODE PERFORMANCE
(All Models)

Quadrants	Two (2): Bipolar Operation at Digital Input Only.
Reference Voltage	Unipolar: +10V Max, +2V Min.
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 2V_{DC} Reference Voltage.
Reference Feedthrough (Unipolar Mode, All Bits OFF, and +2V to +10V (p-p), Sinewave Frequency for 1/2 LSB (p-p) Feedthrough)	22kHz Typical
Output Slew Rate 10%-90%	1.3mA/μs
90%-10%	1.3mA/μs
Output Settling Time (All Bits ON and a +2V to +10V Step Change in Reference Voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Full Power Bandwidth (+10V to +3V)		200			200		kHz
Small Signal Closed-Loop Bandwidth		2.4			2.4		MHz

NOTES:
1. The Digital Input Levels are Guaranteed but not Tested Over the Temperature Range.
2. See Settling Time Section.

DIGITAL INPUTS

The HI-5660 accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement*, or Offset Binary (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i. e. the line is drawn between the end-points of the actual transfer characteristic (codes 00. . .0 and 11. . .1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HI-5660

OP AMP SELECTION

The HI-5660's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

Applying the HI-5660 (Continued)

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TABLE 1. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS: OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)*	CALIBRATION: APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

*Many op amps do not require this resistor, since a bias current of 60nA produces a worst case output error of only 100μV. For a low bias current amplifier, connect its non-inverting input directly to ground.

NO-TRIM OPERATION

The HI-5660 will perform as specified without calibration adjustments. To operate without calibration, substitute 50 Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω ; also remove the network on pin 7 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

When using wide bandwidth op amps, the feedback capacitor C may be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-5660, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

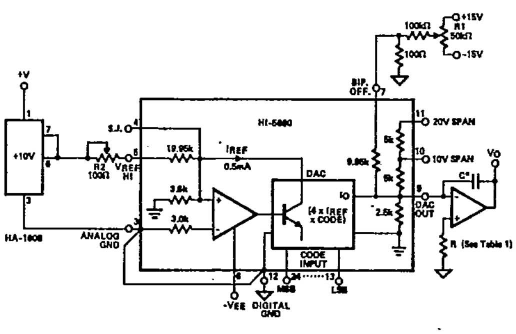


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

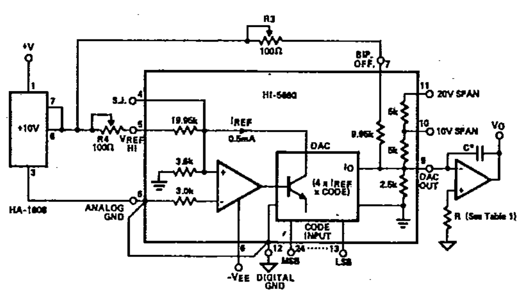


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-5660), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X +15ns.

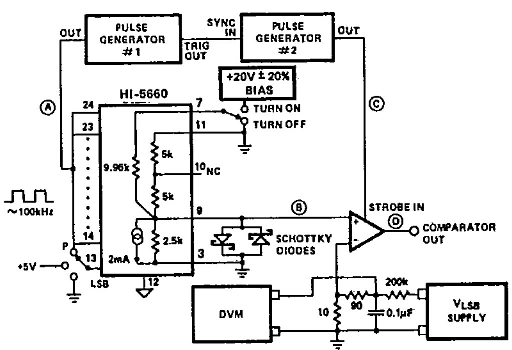


FIGURE 3A.

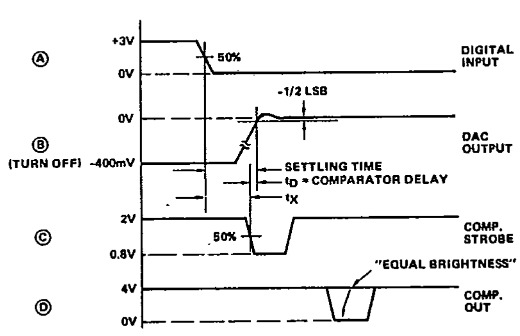


FIGURE 3B.

Other Considerations

GROUNDS

The HI-5660 has two ground terminals, pin 3 (ANALOG GND) and pin 12 (DIGITAL GND). The current through pin 3 is near-zero DC, but pin 12 carries up to 1.75mA of code-dependent current from bits 1, 2 and 3. The general rule is to connect pin 3 to the system analog ground and pin 12 to the power or digital ground. If the system has a single ground point, provide separate paths to pins 3 and 12.

Current cancellation in pin 3 is accomplished as follows: An auxiliary 9 bit R-2R ladder is driven by the complement of the HI-5660 input code. Together, the main and auxiliary ladders draw a constant 2.25mA from the internal analog ground, regardless of input code. This current is then sourced from the positive supply via a current mirror, yielding near-zero current through pin 3.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-5660 are very critical for high speed performance. Output capacitance of the DAC is only 25pF, so a small change or additional capacitance may alter the output op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C).

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-5660 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient.

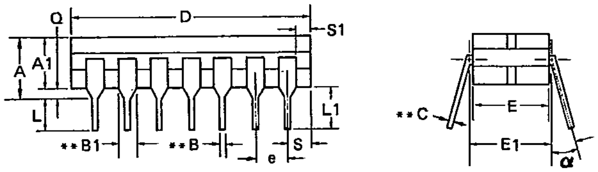
Die Characteristics

Transistor Count		158
Die Size:		104 x 172 mils
Thermal Constants;	θ_{ja}	52°C/W
	θ_{jc}	17°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

Package Configuration

T-90-20

A B C D E .300 CERAMIC DUAL-IN-LINE



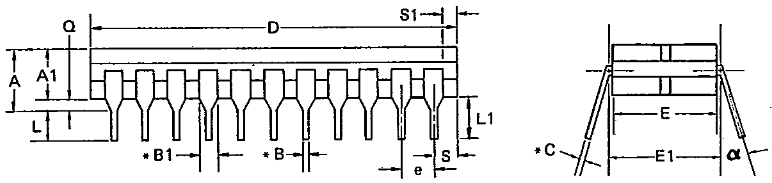
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 / SSI	— / .200	.140 / .160	.016 / .023	.050 / .065	.008 / .015	.375 / .395	.245 / .265	.290 / .310	.100 / BSC	.125 / .150	.150 / —	— / .055	.005 / —	.015 / .060	0° / 15°
B1	14 / MSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
B2	14 / LSI	— / .200	.140 / .170	.016 / .023	.050 / .065	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
C1	16* / MSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.265 / .285	.290 / .310	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
C2	16* / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.753 / .785	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
D	18 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.882 / .915	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
E	20 / LSI	— / .200	.140 / .170	.016 / .023	.050* / .065*	.008 / .015	.940 / .970	.285 / .305	.300 / .320	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add +0.003 inches

F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.055 / 1.085	.375 / .395	.395 / .415	.100 / BSC	.125 / .180	.150 / —	— / .080	.005 / —	.015 / .060	0° / 15°
G .600	24 / LSI	— / .225	.150 / .180	.016 / .023	.050 / .065	.008 / .015	1.24 / 1.27	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°
H .600	28 / LSI	— / .225	.160 / .190	.016 / .023	.050 / .065	.008 / .015	1.44 / 1.47	.515 / .535	.595 / .615	.100 / BSC	.125 / .180	.150 / —	— / .098	.005 / —	.015 / .060	0° / 15°

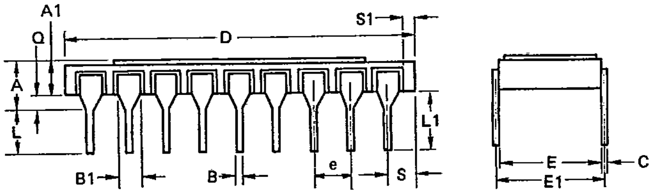
* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

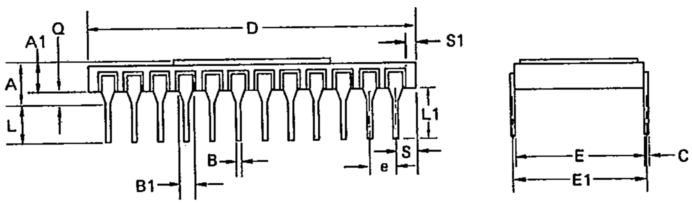
Package Configuration

I .300 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	—/.200	.080/.110	.016/.023	.045/.060	.008/.015	.890/.910	.280/.300	.290/.310	.100/BSC	.125/.180	.150/—	—/.098	.005/—	.025/.045

J K L .600 SIDEBRAZE DUAL-IN-LINE



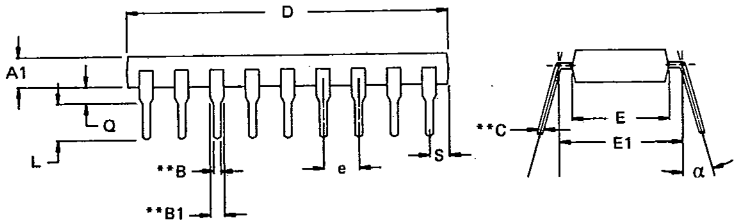
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	—/.225	.080/.110	.016/.023	.040/.054	.008/.015	1.185/1.215	.587/.603	.598/.612	.100/BSC	.125/.180	.150/—	—/.080	.005/—	.040/.060
K	28	—/.225	.080/.110	.016/.023	.040/.054	.008/.015	1.385/1.415	.587/.603	.598/.612	.100/BSC	.125/.180	.150/—	—/.080	.005/—	.030/.060
L	40	—/.225	.080/.110	.016/.023	.040/.054	.008/.015	1.980/2.020	.587/.603	.598/.612	.100/BSC	.125/.180	.150/—	—/.080	.005/—	.040/.060

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

M N O P Q .300 PLASTIC DUAL-IN-LINE

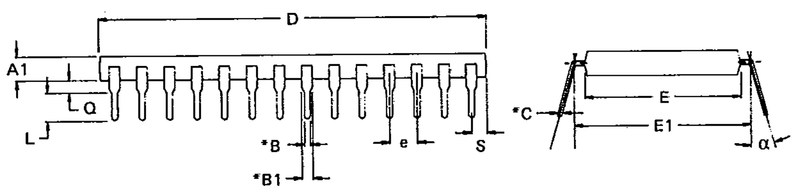


PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125/.140	.016/.023	.050/.070	.008/.015	.370/.390	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
N	14	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
O	16*	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.025/.035	.020/.040	0°/15°
P	18	.125/.140	.016/.023	.050/.070	.008/.015	.900/.920	.245/.265	.290/.310	.090/.110	.110/.150	.040/.060	.020/.040	0°/15°
Q	20	.130/.145	.016/.023	.050/.070	.008/.015	1.030/1.050	.250/.270	.290/.310	.090/.110	.110/.150	.060/.080	.020/.040	0°/15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add 0.003 inches.

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24	.145/.155	.016/.023	.050/.070	.008/.015	1.24/1.26	.540/.560	.590/.610	.090/.110	.110/.150	.045/.095	.020/.040	0°/15°
S	28	.145/.155	.016/.023	.050/.070	.008/.015	1.54/1.57	.540/.560	.590/.610	.090/.110	.110/.150	.110/.160	.020/.040	0°/15°

* Solder dip finish add 0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

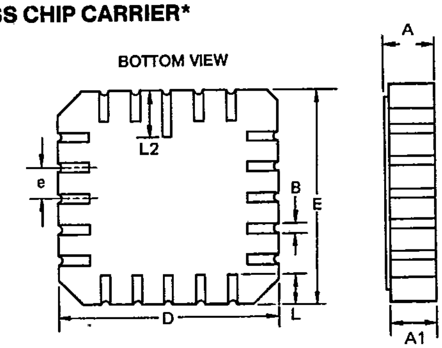
BSC means basic spacing between centerlines.

Package Configuration

T .350 CERAMIC LEADLESS CHIP CARRIER*

U .450 CERAMIC LEADLESS CHIP CARRIER*

V .650 CERAMIC LEADLESS CHIP CARRIER*

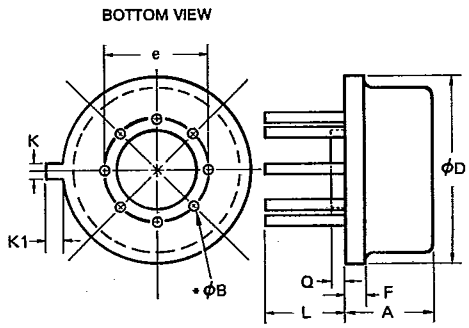


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 / .350 SQ	.073 / .089	.063 / .077	.022 / .028	.342 / .358	.342 / .358	.050 / BSC	.045 / .055	.075 / .095
U	28 / .450 SQ	.074 / .088	.064 / .076	.022 / .028	.442 / .458	.442 / .458	.050 / BSC	.045 / .055	.075 / .095
V	44 / .650 SQ	.073 / .089	.063 / .077	.022 / .028	.643 / .662	.643 / .662	.050 / BSC	.045 / .055	.075 / .095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN

X TO-100 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	.165 / .185	.016 / .018	.345 / .365	.190 / .210	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040
X	10 TO-100	.165 / .185	.016 / .018	.345 / .365	.220 / .240	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040

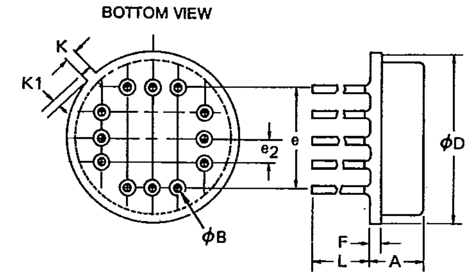
* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

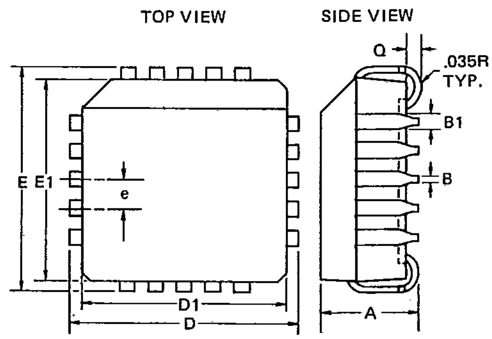
Package Configuration

Y TO-8 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130 / .150	.016 / .021	.585 / .615	.400 / BSC	.100 / BSC	.020 / .040	.027 / .034	.027 / .045	.500 / .550

AA AB AC PLASTIC LEADED CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165 / .180	.013 / .021	.026 / .032	.385 / .395	.350 / .356	.050 / BSC	.020 / —
AB	28	.165 / .180	.013 / .021	.026 / .032	.485 / .495	.450 / .456	.050 / BSC	.020 / —
AC	44	.165 / .180	.013 / .021	.026 / .032	.685 / .695	.650 / .656	.050 / BSC	.020 / —

NOTE: Dimensions are Min/Max. Dimensions are in inches.

BSC means basic spacing between centerlines.