AN8280, AN8281S

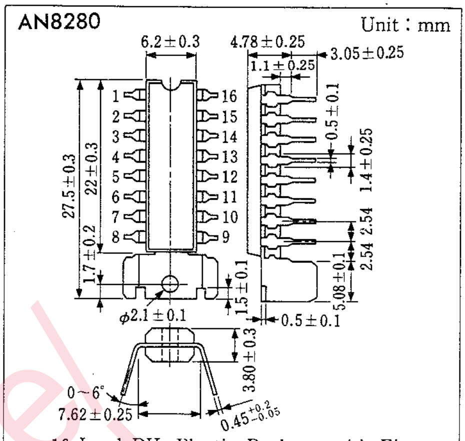
ICs for Spindle Motor Direct Drive

■ Outline

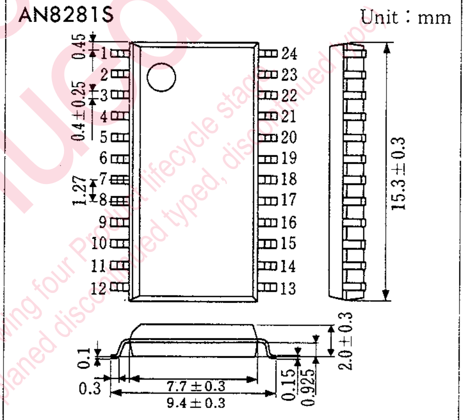
The AN8280 and the AN8281S are integrated circuits designed for spindle motor drive of CD player, incorporating a reverse detection logic circuit, an FG pulse output circuit, a filter amp. and an output-step transistor. The AN8281S can drive the spindle motor at voltage lower than that of the AN8280 by externally mounting the PNP transistor corresponding to the output-step one.

■ Features

- ●Equipped with spindle motor drive, reverse detection logic and output current control functions.
- ●Compact design realized by PANAFLAT package. (AN8281S)

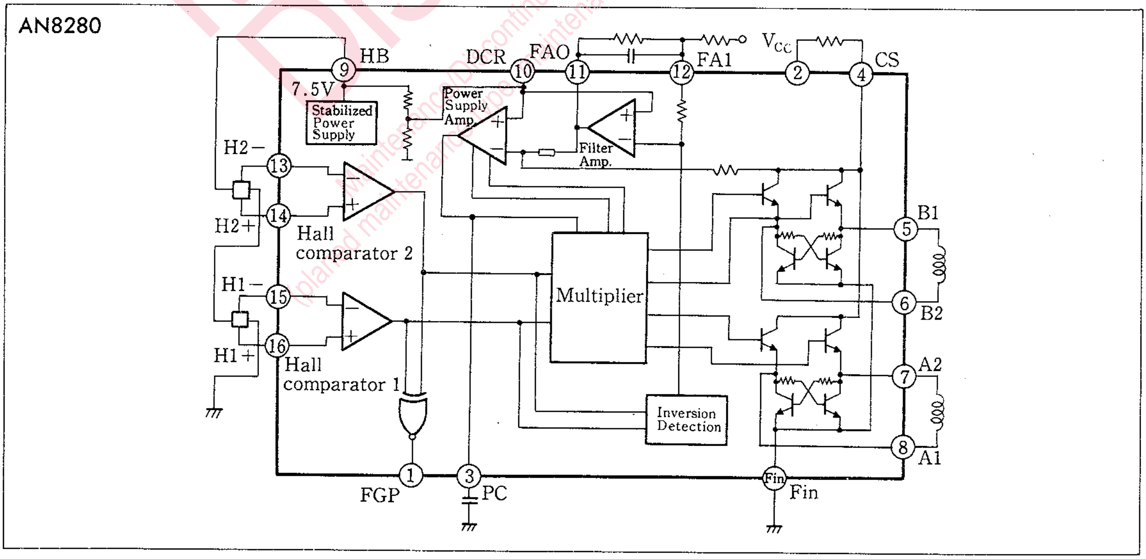


16-Lead DIL Plastic Package with Fin

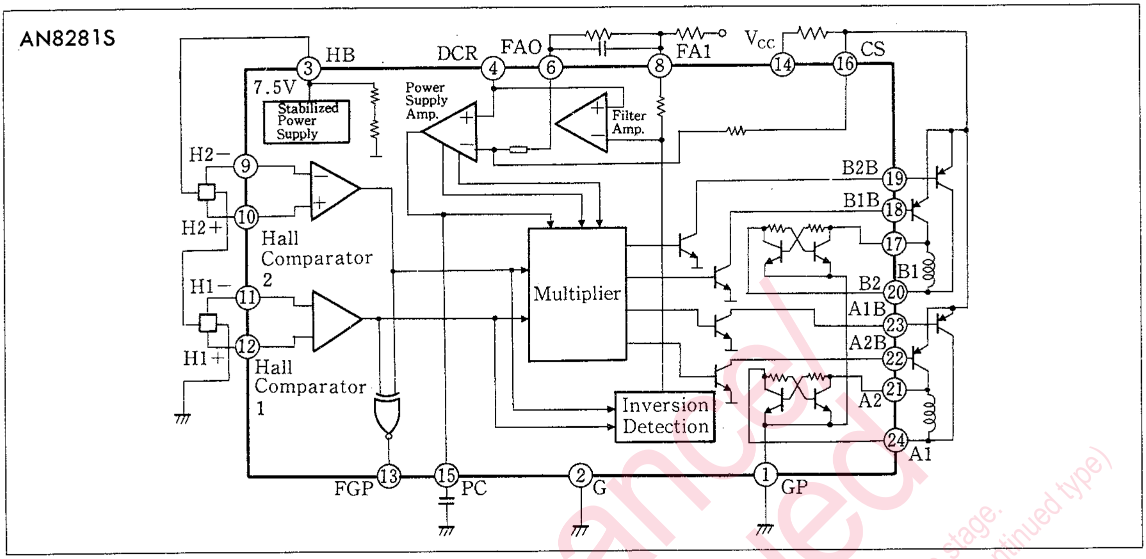


24-Lead PANAFLAT Package(SO-24D)

■ Block Diagram and Peripheral Circuit



Block Diagram and Peripheral Circuit



Pin

● AN8280

Pin No.	Pin Name	Pin No.	Pin Name
1	FG Pulse	10	Drive Ref. Input
2	V_{CC}	11	Filter Amp. Output
3	Drive Amp. PC	12	Fillter Amp. Input
4	Current Det.	13	Hall Amp. ($H2^-$)
5	Drive Output (B1)	14	Hall Amp. ($H2^+$)
6	Drive Output (B2)	15	Hall Amp. ($H1^-$)
7	Drive Output (A2)	16	Hall Amp. ($H1^+$)
8	Drive Output (A1)	Fin	GND
9	Hall Bias	—	—

● AN8281S

Pin No.	Pin Name	Pin No.	Pin Name
1	GND (Power)	13	FG Pulse Output
2	GND (Signal)	14	V_{CC}
3	Hall Bias	15	Drive Amp. PC
4	Drive Ref. Voltage	16	Current Det.
5	NC	17	Drive Output (B1)
6	Fillter Amp. Output	18	Base Drive Output (B1B)
7	NC	19	Base Drive Output (B2B)
8	Filter Amp. Input	20	Drive Output (B2)
9	Hall Amp. 2 ($H2^-$)	21	Drive Output (A2)
10	Hall Amp. 2 ($H2^+$)	22	Base Drive Output (A2B)
11	Hall Amp. 1 ($H1^-$)	23	Base Drive Output (A1B)
12	Hall Amp. 1 ($H1^+$)	24	Drive Output (A1)

■ Absolute Maximum Ratings (Ta=25℃)

Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}	20	V
Pin Voltage	AN8280	$V_1, V_{4\sim8}, V_{10\sim16}$	$-0.3\sim V_{CC}$	V
	AN8281S	$V_{3\sim13}, V_{15\sim24}$		
Pin Voltage		V_3	$-0.3\sim+1$	V
Pin Current	AN8280	I_1, I_{11}	$-0.1\sim+10$	mA
	AN8281S	I_6, I_{13}		
Pin Current	AN8280	I_1, I_{11}	$-10\sim+10$	mA
		$I_{5\sim8}$	$-500\sim+500$	mA
		I_9	$-30\sim+0.5$	mA
	AN8281S	$I_{17,20,21,24}, I_{16}$	$-10\sim+500$	mA
		$I_{18,19,22,23}$	$-1\sim+30$	mA
		I_3	$-50\sim+5$	mA
Power Dissipation	AN8280	P_D	1600	mW
	AN8281S		520	mW
Operating Ambient Temperature		T_{opr}	$-20\sim+75$	℃
Storage Temperature	AN8280	T_{stg}	$-55\sim+150$	℃
	AN8281S		$-55\sim+125$	℃

■ Electrical Characteristics (Ta=25℃)

● AN8280

Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
No-load Total Current	I_{CC}	1	$V_{CC}=12V$	3	8	20	mA
Output Amplitude 1	ν_{O1}	2	$V_{CC}=12V$, $R_L=40\Omega$	8.5			V
Output Amplitude 2	ν_{O2}	3	$V_{CC}=12V$, $R_L=40\Omega$	−0.1		0.1	V
Switching Offset	V_{OFS}	4	$V_{CC}=12V$, $R_L=40\Omega$	−20		20	mV
Limit Voltage	V_L	5	$V_{CC}=15V$, $R_L=40\Omega$	0.25	0.35	0.35	V
Idle Voltage	V_I	5	$V_{CC}=12V$, $R_L=40\Omega$			10	mV
Drive Offset	V_O	5	$V_{CC}=12V$, $R_L=40\Omega$	−100		100	mV
Drive Gain	G_D	5	$V_{CC}=12V$, $R_L=40\Omega$	0.455	0.505	0.555	Times
Direction Decision Output	V_{RDH}	6	$V_{CC}=12V$, $R_L=40\Omega$	7		8	V
	V_{RDL}	6	$V_{CC}=12V$, $R_L=40\Omega$	2		3	V
FG Pulse Output	V_{FGH}	6	$V_{CC}=12V$, $R_L=40\Omega$	11			V
	V_{FGL}	6	$V_{CC}=12V$, $R_L=40\Omega$			0.5	V
Hall Bias Voltage	V_{HB}	6	$V_{CC}=12V$, $R_L=40\Omega$	7.2		7.9	V

Note) Operating Supply Voltage Range : $V_{CC(opr)}=9\sim18V$

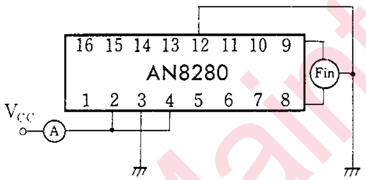
■ Electrical Characteristics ($Ta=25^\circ C$)

● AN8281S

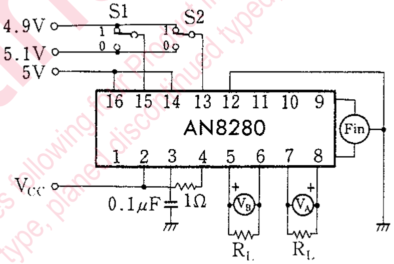
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
No-load Total Current	I_{CC}	7	$V_{CC}=12V$	4	8	20	mA
Output Amplitude 1	v_{O1}	8	$V_{CC}=12V, R_L=40\Omega$		0.6	0.8	V
Output Amplitude 2	v_{O2}	9	$V_{CC}=12V, R_L=40\Omega$	−0.1		0.1	V
Output Current	I_O	10	$V_{CC}=12V, R_L=40\Omega$	5	10	20	mA
Switching Offset	V_{OFS}	11	$V_{CC}=12V, R_L=40\Omega$	−20		20	mV
Limit Voltage	V_L	12	$V_{CC}=15V, R_L=40\Omega$	0.25	0.30	0.35	V
Idle Voltage	V_I	12	$V_{CC}=12V, R_L=40\Omega$			10	mV
Drive Offset	V_O	12	$V_{CC}=12V, R_L=40\Omega$	−100		100	mV
Drive Gain	G_D	12	$V_{CC}=12V, R_L=40\Omega$	0.48	0.54	0.58	Times
Direction Decision Output	V_{RDH}	13	$V_{CC}=12V, R_L=40\Omega$	8		9	V
	V_{RDL}	13	$V_{CC}=12V, R_L=40\Omega$	2		3	V
FG Pulse Output	V_{FGH}	13	$V_{CC}=12V, R_L=40\Omega$	11			V
	V_{FGL}	13	$V_{CC}=12V, R_L=40\Omega$			0.5	V
Hall Bias Voltage	V_{HB}	13	$V_{CC}=12V, R_L=40\Omega$	7.2	7.6	7.6	V

Note) Operating Supply Voltage Range : $V_{CC(opr)}=9\sim18V$

Test Circuit 1 (I_{CC})

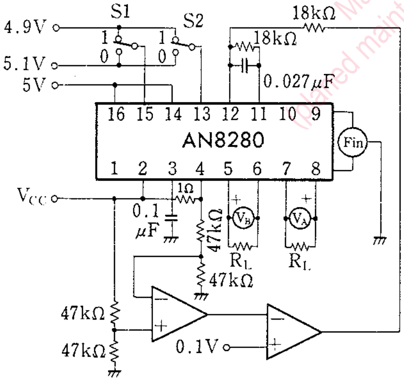


Test Circuit 2 (v_{O1})



S1	S2	V_A	V_B
1	1	> 8.5V	—
0	0	<−8.5V	—
0	1	—	> 8.5V
1	0	—	<−8.5V

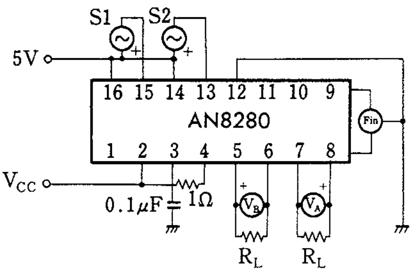
Test Circuit 3 (v_{O2})

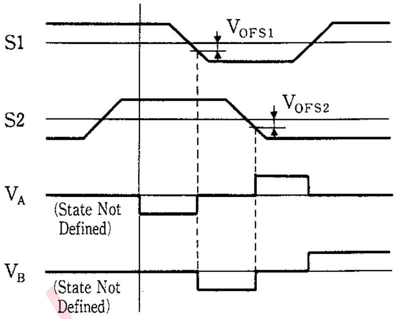


S1	S2	$\|V_A\|$	$\|V_B\|$	Remarks
1	0	—	—	
1	1	—	—	Forward
0	1	<0.1V	—	
0	0	—	<0.1V	
1	0	<0.1V	—	
1	1	—	<0.1V	

- ●Measure the phase output amplitude at the output-step OFF side according to the state of hall amp. input (Pin13~16) for output amplitude 2 (v_{O2}).
- ●To release the reverse detection logic, change over the switches S1 and S2 and perform the forward set as shown in the table left.
- ●After performing the forward set, measure the specified voltage corresponding to the state 4 of switches S1 and S2 as shown in the table left.

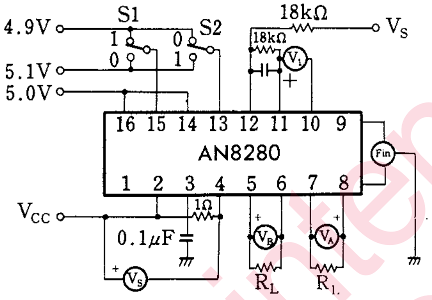
Test Circuit 4 (V_{OFS})

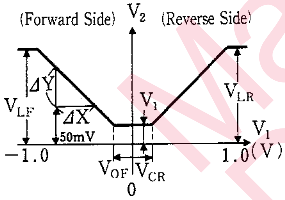




When $|V_A| = |V_B|$, make the change-over decision and measure the offset of signal level S1 and S2.

Test Circuit 5 (V_L, V_I, V_O, G_D)





Drive Input/Output Characteristics Figure

Forward Set Table

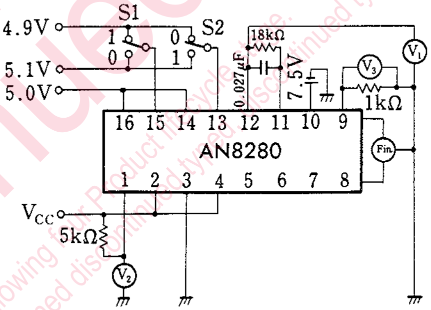
S1	S2	Remarks
1	0	Forward Set
1	1	

Measuring Item Table

Item	Symbol	Measuring Point
Limit Voltage	V_L	V_{LF} V_{LR}
Idle Voltage	V_I	V_I
Drive Offset	V_O	V_{OF} V_{OR}
Drive Gain	G_D	ΔY/ΔX

- The drive input/output characteristics are the characteristics of drive output (V_2) for drive input (V_1). They are represented typically as shown in the figure above. Measuring item is as shown in the table above and the measuring point is indicated with symbol in the figure.
  However, prior to measurement, be sure to perform the forward set as shown in the table above in order to release the reverse detection logic.

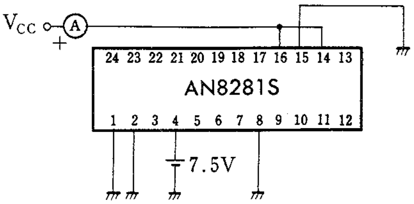
Test Circuit 6 (V_{RDH}, V_{RDL}, V_{FGH}, V_{FGL}, V_{HB})



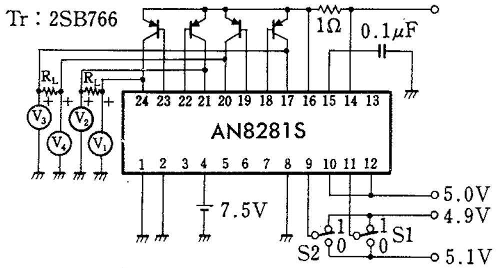
S1	S2	V_1	V_2	Remarks
0	0	—	—	Reverse Decision
0	1	V_{RDL}	—	
1	0	—	—	Forward Decision
1	1	V_{RDH}	—	
1	1	—	V_{FGH}	FG Pulse Output
0	1	—	V_{FGL}	
0	0	—	V_{FGH}	
1	0	—	V_{FGL}	

- Direction decision
  Sequential set is made from the top as shown in the table above and measure V_1 as V_{RDL} for reverse decision and V_1 as V_{RDH} for forward decision.
- FG pulse output
  Measure the voltage V_2 corresponding to the state of switches S1 and S2 as shown in the table above and confirm H and L levels.
- Hall bias voltage
  Connect the 1kΩ load irrespective of the state of switches S1 and S2 and measure the voltage V_3.

Test Circuit 7 (I_{CC})



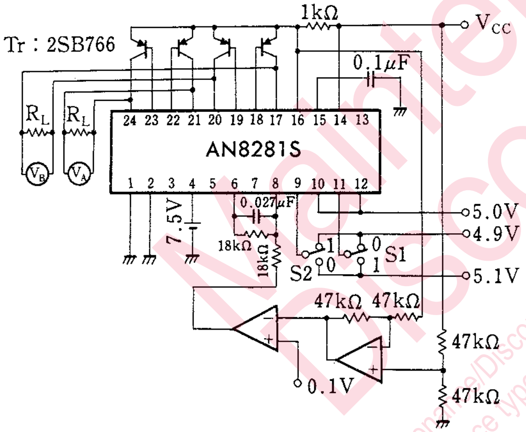
Test Circuit 8 (v_{08})



S1	S2	V_1	V_2	V_3	V_4
1	1	<0.8V	—	—	—
0	0	—	<0.8V	—	—
0	1	—	—	<0.8V	—
1	0	—	—	—	<0.8V

- According to the state of the output amplitude 1 (v_{02}) hall amp. input (Pins ⑨ to ⑫), measure the output-step saturation voltages V_1 to V_4 as shown in the table above.

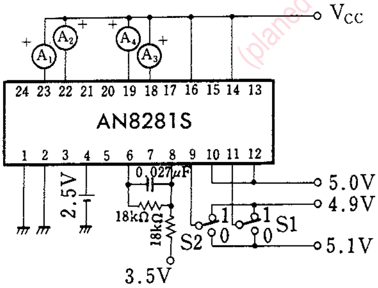
Test Circuit 9 (v_{09})



S1	S2	$\lvert V_A \rvert$	$\lvert V_B \rvert$	Remarks
1	0	—	—	
1	1	—	—	Forward set
0	1	<0.1V	—	
0	0	—	<0.1V	
1	0	<0.1V	—	
1	1	—	<0.1V	

- According to the state of the output amplitude 2 (v_{02}) hall amp. input (Pin ⑨ to ⑫), measure the output amplitude of phase at the output-step OFF side.
- To release the reverse detection logic, change over the switches S1 and S2 and perform the forward set.
- After performing the forward set, measure the specified voltage corresponding to the state 4 of switches S1 and S2 as shown in the table above.

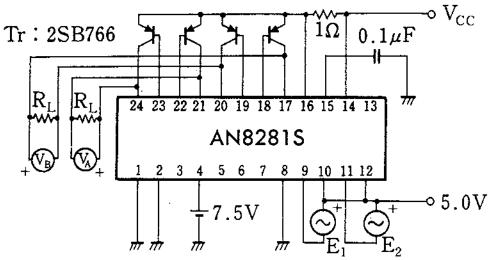
Test Circuit 10 (I_O)

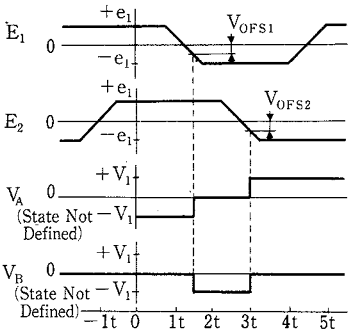


S1	S2	Measuring Current
1	0	—
1	1	—
1	1	A_1
0	1	A_3
0	0	A_2
1	0	A_4

- In the output drive current, measure the current of A_1 to A_4 as shown in the table left according to the state of hall amp. input (Pin ⑨ to ⑫). For the second item in the table above, perform the forward set to release the reverse detection logic. After that, measure the specified current as shown in the table left.

Test Circuit 11 (V_{OFS})

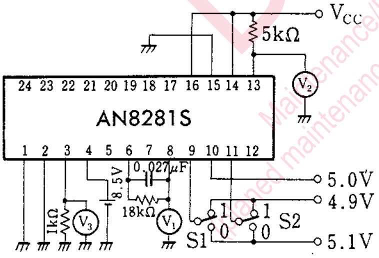




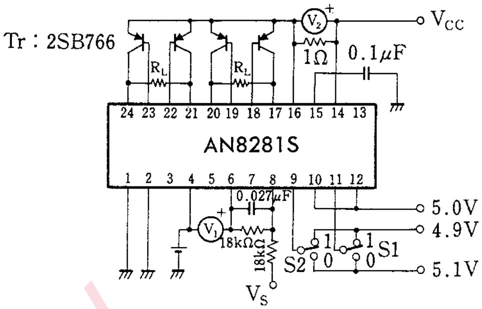
- In the switching offset (V_{OFS}), measure the offset voltage of output-step phase switching input by the hall amp. input.
- A timing chart for switching offset measurement is shown in the figure above.
  Measure the V_A, V_B output and change over the phase at $|V_A| = |V_B|$.
  Then, measure V_{OFS1} and V_{OFS2}.
  The following values are appropriate for X and Y-axis of each signal.

e_1 : 50~200mV
V_1 : 8~11V
t : >1ms

Test Circuit 13 (V_{RDH}, V_{RDL}, V_{FGH}, V_{FGL}, V_{HB})

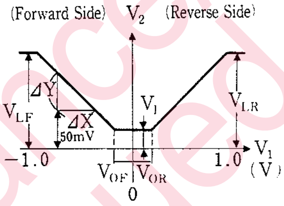


Test Circuit 12 (V_L, V_I, V_O, G_D)



Forward Set Table

S1	S2	Remarks
1	0	Forward Set
1	1	



Drive Input/Output Characteristics Figure

Measuring Item Table

Item	Symbol	Measuring Point
Limit voltage	V_L	V_{LF} V_{LR}
Idle voltage	V_I	V_I
Drive offset	V_O	V_{OF} V_{OR}
Drive gain	G_D	ΔY/ΔX

- The drive input/output characteristics are those of drive output (V_2) for drive input (V_1). They are represented typically as shown in the figure above. Measuring item is shown in the table above and the measuring point is indicated with symbol in the figure.
  However, prior to measurement, be sure to perform the forward set as shown in the table above in order to release the reverse detection logic.

S1	S2	V_1	V_2	Remarks
0	0	—	—	Reverse Decision
0	1	V_{RDL}	—	
1	0	—	—	Forward Decision
1	1	V_{RDH}	—	
1	1	—	V_{FGH}	FG Pulse Output
0	1	—	V_{FGL}	
0	0	—	V_{FGH}	
1	0	—	V_{FGL}	

- Direction decision
  Sequential set is made from the top as shown in the table above and measure V_1 as V_{RDL} for reverse decision and V_1 as V_{RDH} for forward decision.
- FG pulse output
  Measure the voltage V_2 corresponding to the state of switches S1 and S2 as shown in the table above and confirm H and L levels.
- Hall bias voltage
  Connect the 1kΩ load irrespective of the state of switches S1 and S2 and measure the voltage V_3.

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