

MX-COM, INC. MiXed Signal ICs

DATA BULLETIN

CMX602A

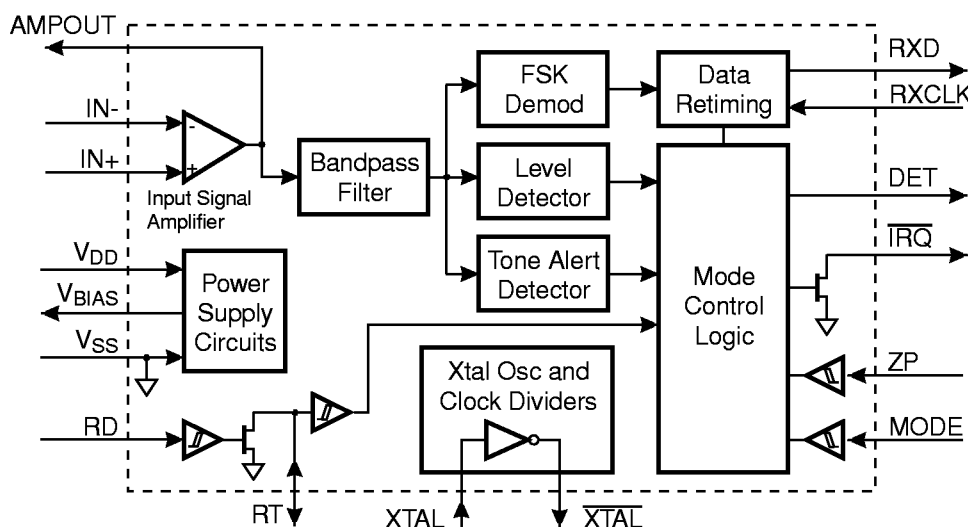
PRELIMINARY INFORMATION

Features

- Automatic CAS Dual Tone Detector
High Sensitivity, Low Falsing
Automatic CAS Duration Checking
- 1 μ A max. 'Zero-Power' Ring or Line
Polarity Reversal Detector
- V23/Bell202 FSK Demodulator
with Data Retiming facility
- μ C Interrupt / Wake-up output to
minimize system operating power
- Low Power Operation 0.5mA at 2.7V_{DD}

Applications

- Caller ID/Caller ID on Call Waiting
Telephones
Adjunct Boxes
- Bellcore, ETSI, British Telecom, and
Mercury Systems
- Computer Telephone Integration
- Call Logging Systems
- Voice Mail Equipment



The CMX602A is a low power CMOS device used for the reception of physical layer signals in Bellcore's Calling Identity Delivery (CID) and Calling Identity on Call Waiting (CIDCW) systems, British Telecom Calling Line Identification Service (CLIP), the Cable Communications Association's Caller Display Services (CDS), and similar evolving services. The CMX602A also meets the requirements of emerging Caller Identity with Call Waiting Services (CIDCW).

This device includes a 'zero-power' ring or line polarity reversal detector, a dual-tone (2130Hz plus 2750Hz) internally timed CPE Alerting Signal (CAS) detector, and a 1200-baud FSK Bell202/V23 compatible asynchronous data demodulator with data retiming circuitry which removes the need for a UART in the associated μ C.

The CMX602A is suitable for use in systems using Bellcore specifications GR-30-CORE and SR-TSV-002476, British Telecom specifications SIN227 and SIN242, CCA TW/P&E/312, ETSI: ETS 300 659 parts 1 and 2 and ETS 300 778 parts 1 and 2, and Mercury Communications MNR 19.

This device may be used with a 2.7V to 5.5V supply and is available in the following packages: 16-pin SOIC (CMX602AD4) and a 16-pin PDIP (CMX602AP3).

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1. Block Diagram

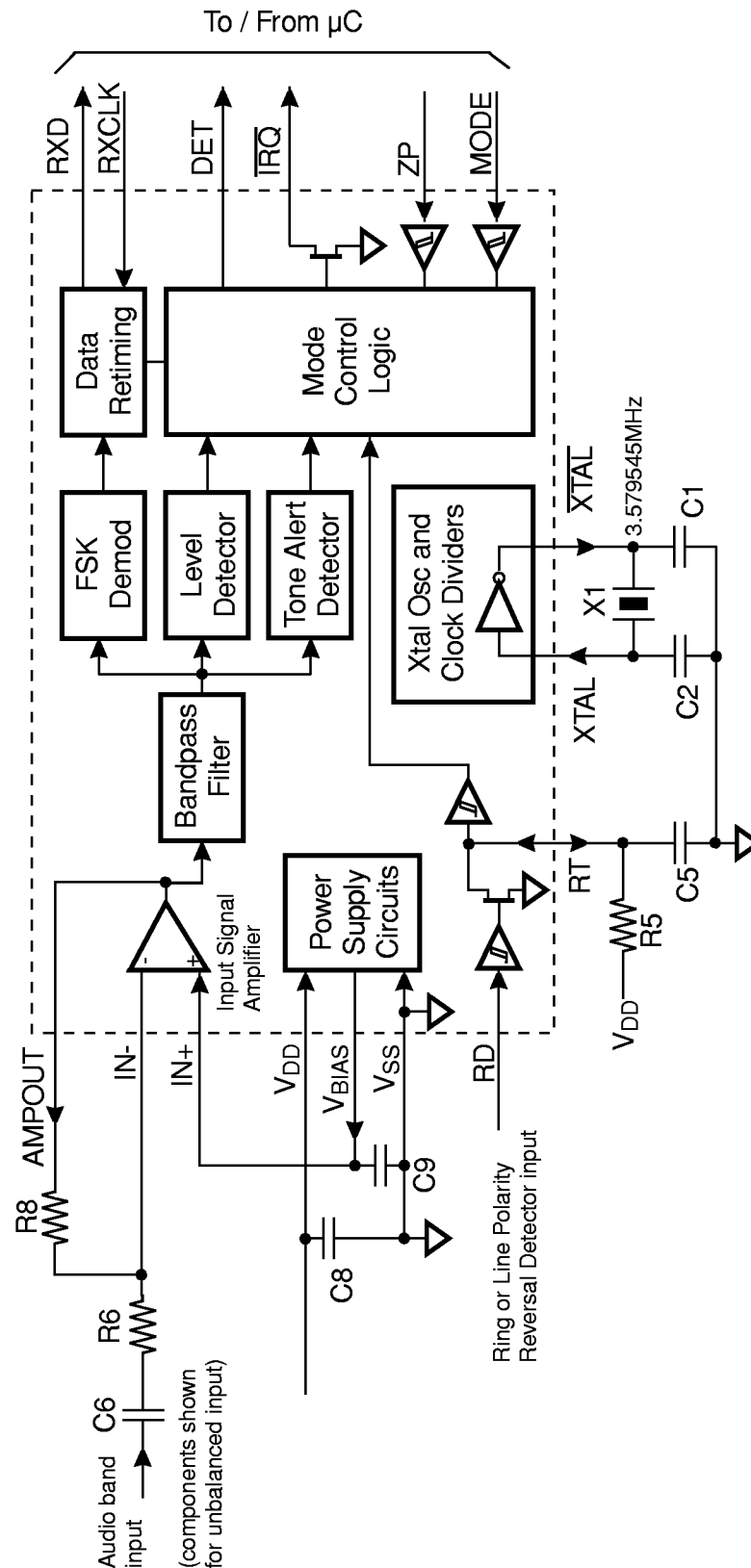


Figure 1: Block Diagram

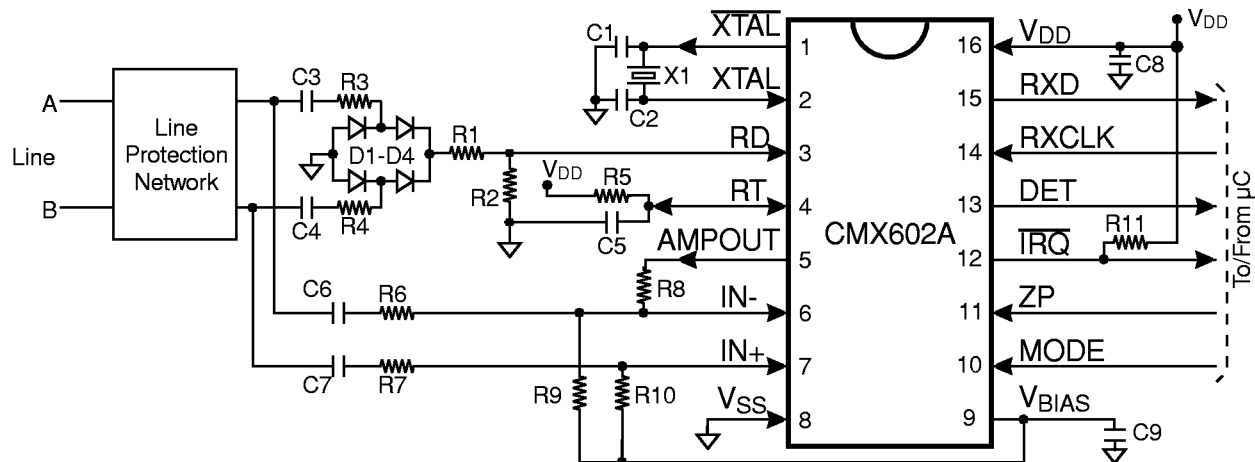
2. Signal List

Pin No.	Signal	Type	Description
1	$\overline{\text{XTAL}}$	output	Output of the on-chip Xtal oscillator inverter
2	XTAL	input	Input to the on-chip Xtal oscillator inverter
3	RD	input (S)	Input to the Ring or Line Polarity Reversal Detector
4	RT	input / output	Open-drain output and Schmitt trigger input forming part of the Ring or Line Polarity Reversal detector. An external resistor to V_{DD} and a capacitor to V_{SS} should be connected to RT to filter and extend the RD input signal
5	AMPOUT	output	Output of the on-chip Input Signal Amplifier
6	IN -	input	Inverting input to the on-chip Input Signal Amplifier
7	IN +	input	Non-inverting input to the on-chip Input Signal Amplifier
8	V_{SS}	power	Negative supply
9	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	MODE	input (S)	Input used to select the Tone Alert or FSK Level Detection operating mode. See Section 4.1
11	ZP	input (S)	High level on this input selects 'Zero-Power' mode, a low level input enables the V_{BIAS} supply, the Input signal amplifier, the Bandpass Filter, and either the FSK or the Tone alert circuits depending on the MODE input
12	$\overline{\text{IRQ}}$	output	Open-drain output (active low) that may be used as an Interrupt Request / Wake-up input to the associated μC . Indicates CAS Dual Tone event of correct duration when device is in Tone Alert Detect Mode. An external pull-up resistor should be connected between this output and V_{DD} .
13	DET	output	Logic level output driven by the Ring or Line Polarity Reversal Detector, the Tone Alert Detector or the FSK Level detect circuits, depending on the operating mode. When device is in Tone Alert Mode, it may be used as a near end voice mute control signal. See Section 4.1
14	RXCLK	input	Logic level input, which may be used to clock, received data bits out of the FSK Data Retiming block. When held high disables FSK Data Retiming block.
15	RXD	output	Logic level output carrying either the raw output of the FSK Demodulator or re-timed 8-bit characters depending on the state of the RXCLK input. See Section 4.6
16	V_{DD}	power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.

Notes: input (S) = Schmitt trigger input

Table 1 : Signal List

3. External Components



Note: It is recommended that the printed circuit board provide a ground plane in the CMX602A area to provide a low impedance ground connection to the V_{SS} pin and to the bypass capacitors C8 and C9.

Figure 2 : Recommended External Components for Bellcore and/or British Telecom Application

R1		470k Ω	$\pm 1\%$
R2	Note 1		$\pm 1\%$
R3, R4			
R5, R6		470k Ω	$\pm 1\%$
R7			
R8	Note 2, 3	470k Ω @ 3.3V 680k Ω @ 5.0V	$\pm 1\%$
R9	Note 2	240k Ω @ 3.3V 200k Ω @ 5.0V	$\pm 1\%$
R10		160k Ω	$\pm 1\%$

R11		100k Ω	$\pm 20\%$
C1, C2		18pF	$\pm 20\%$
C3, C4		0.1 μ F	$\pm 20\%$
C5		0.33 μ F	$\pm 20\%$
C6, C7		680pF	$\pm 20\%$
C8, C9		0.1 μ F	$\pm 20\%$
X1	Note 4	3.579545MHz	$\pm 0.1\%$
D1 - D4		1N4004	

Table 2: Recommended External Components

Recommended External Component Notes:

1. See Section 4.8
2. See Section 4.2
3. The recommended values of R8 were selected for applications in both Bellcore and British Telecom Systems. Optimum Bellcore-only operation may be achieved by reducing the value of R8 e.g. to 656k Ω @ 5.0V.
4. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD} , peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Mode Control Logic

The CMX602A's operating mode and the source of the DET and $\overline{\text{IRQ}}$ outputs are determined by the logic levels applied to the MODE and ZP input pins.

ZP	MODE	Mode	DET output from	$\overline{\text{IRQ}}$ output from
0	0	Tone Alert Detect	Tone Alert Signal Detection	Valid 'off-hook' CAS Duration. Ring or Line Polarity Reversal Detector
0	1	FSK Receive	FSK Level Detector	FSK Data Retiming (if enabled). Ring or Line Polarity Reversal Detector.
1	0	Zero-Power	Ring or Line Polarity Reversal Detector	Ring or Line Polarity Reversal Detector.
1	1	Zero-Power	Ring or Line Polarity Reversal Detector	None

In the 'Zero-Power' modes, power is removed from all of the internal circuitry except for the Ring or Line Polarity Reversal Detector and the DET and $\overline{\text{IRQ}}$ outputs.

4.2 Input Signal Amplifier

The Input Signal Amplifier is used to convert the balanced FSK and Tone Alert signals received over the telephone line to an unbalanced signal of the correct amplitude for the FSK receiver and Tone Alert Detector circuits.

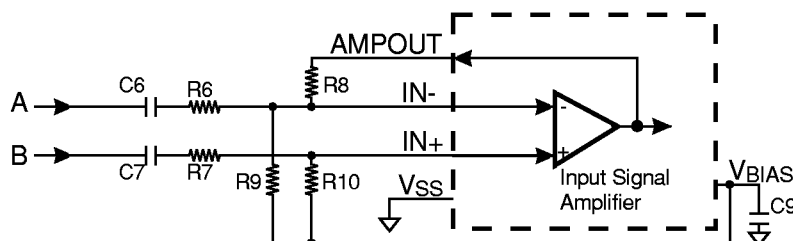


Figure 3: Input Signal Amplifier, balanced input configuration

The design equations for this circuit are:

$$\text{Differential Voltage Gain } \frac{V_{\text{AMPOUT}}}{V_{(B-A)}} = \frac{R_8}{R_6} \quad R_9 = \frac{R_8 \times R_{10}}{(R_8 - R_{10})}$$

$$R_6 = R_7 = 470\text{k}\Omega \quad R_{10} = 160\text{k}\Omega$$

The target differential voltage gain depends on the expected A and B input signal levels and the CMX602A's internal overload and threshold levels, which are proportional to the supply voltage.

The CMX602A has been designed to meet the applicable specifications when $R_8 = 430\text{k}\Omega$ at $V_{\text{DD}} = 3.0\text{V}$ nominal, rising to $680\text{k}\Omega$ at $V_{\text{DD}} = 5.0\text{V}$ (see note) and $R_9 = 240\text{k}\Omega$ at $V_{\text{DD}} = 3.0\text{V}$ dropping to $200\text{k}\Omega$ at $V_{\text{DD}} = 5.0\text{V}$ as indicated in Section 3 and as shown in Figure 5. Reference Notes found in Section 3.

The Input Signal Amplifier may also be used to allow the CMX602A to operate from an unbalanced signal source as shown in Figure 4. In this unbalanced signal configuration, the values of R6 and R8 are the same as used for the balanced input configuration.

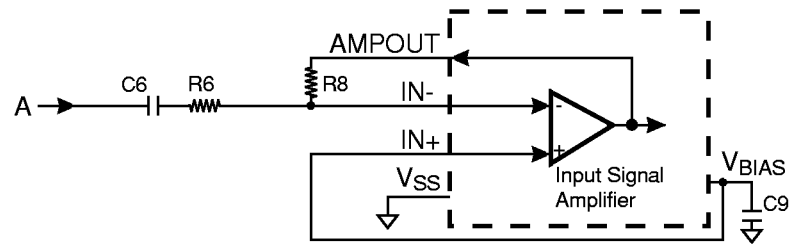


Figure 4: Input Signal Amplifier, unbalanced input configuration

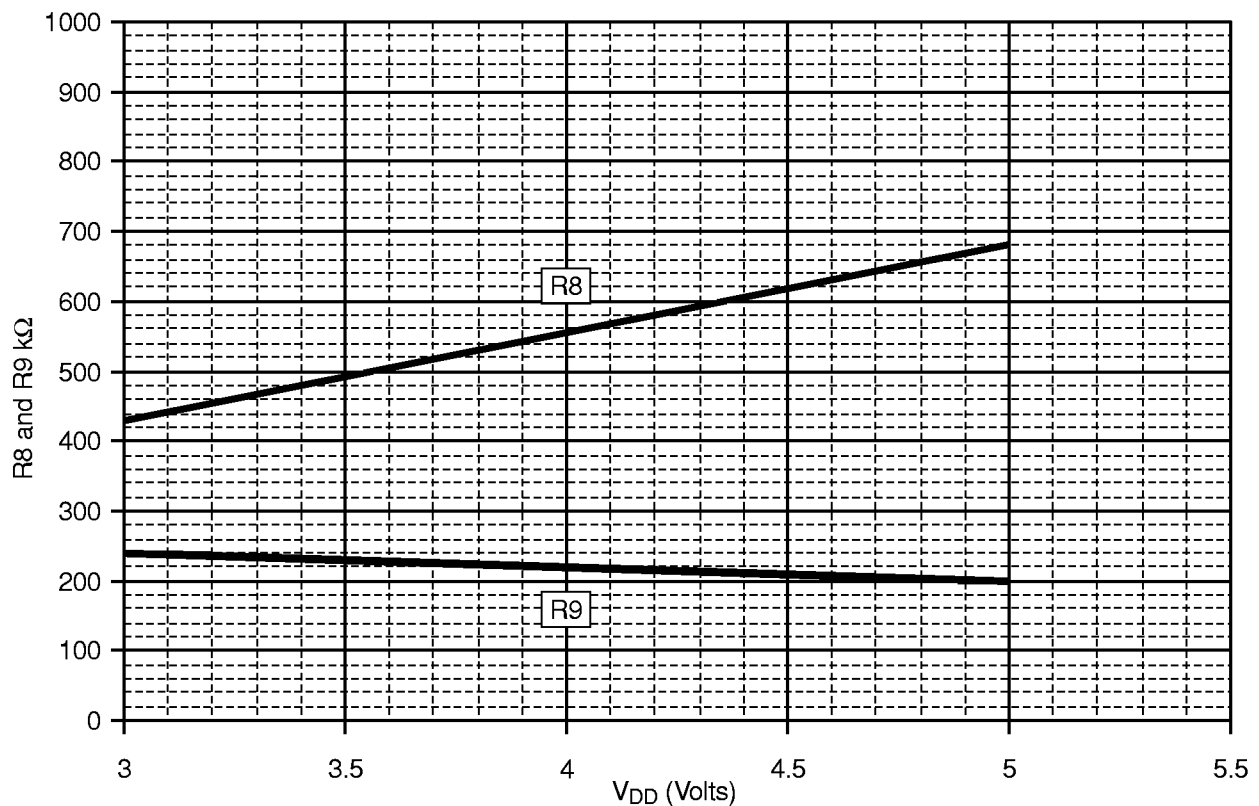


Figure 5: Input Signal Amplifier, Optimum Values of R8 and R9 vs. V_{DD}

4.3 Bandpass Filter

The Bandpass Filter is used to attenuate out of band noise and interfering signals from reaching the FSK Demodulator, Tone Alert Detector and Level Detector circuits. The characteristics of this filter differ between FSK and Tone Alert modes. Switched Capacitor filter stages clocked at 57.7kHz provide primary filtering. If the input signal is band limited to below 28.85kHz then external anti-aliasing filtering is not required.

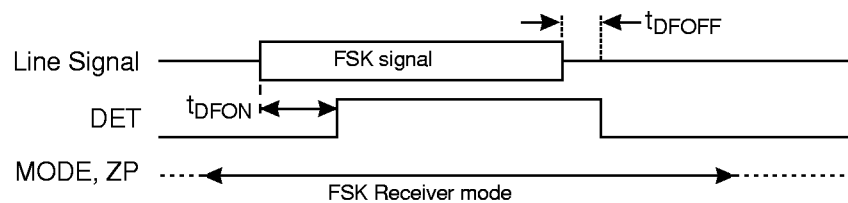
4.4 Level Detector

The Level Detector block operates by measuring the level of the signal at the output of the Bandpass Filter. It then compares it against a threshold, which depends on whether FSK Receive or Tone Alert Detect mode has been selected.

In Tone Alert Detect mode the output of the Level Detector block provides an input to the Tone Alert Signal Detector.

In FSK Receive mode the CMX602A DET output will be set high when the level has exceeded the threshold for a sufficient duration. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note: In FSK Receive mode, this circuit may also respond to non-FSK signals such as speech.



See Section 6.1 for definitions of t_{DFON} and t_{DFOFF}

Figure 6: FSK Level Detector Operation

4.5 FSK Demodulator

The FSK Demodulator block converts the 1200 baud FSK input signal to a digital data stream which is output via the RXD pin as long as the Data Retiming function is not enabled (Holding RXCLK continuously high). The RXD output does not depend on the state of the FSK Level Detector output.

Note: In the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data.

4.6 FSK Data Retiming

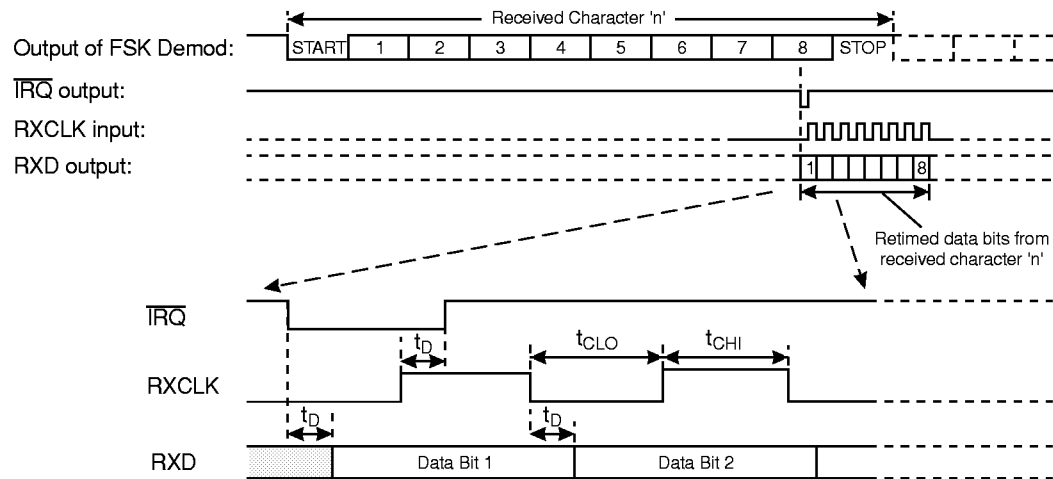
The Data Retiming block extracts the 8 data bits of each character from the received asynchronous data stream and presents them to the μC under the control of strobe pulses applied to the RXCLK input. The timing of these pulses is not critical, and they may easily be generated by a simple software loop. This facility removes the need for a UART in the μC without incurring an excessive software overhead.

The block operates on a character by character basis by first looking for the mark to space transition which signals the beginning of the start bit. Using this transition as a timing reference, the block samples the output of the FSK Demodulator in the middle of each of the following 8 received data bits and stores the results in an internal 8-bit shift register.

When the eighth data bit has been clocked into the internal shift register, the CMX602A examines the RXCLK input. If RXCLK input is low, then the \overline{IRQ} output will be pulled low, thereby sending the first of the stored data bits to the RXD output pin. Upon detecting that the \overline{IRQ} output has gone low, the μC should pulse the RXCLK pin high 8 times. The high to low transition at the end of the first 7 of these pulses will be used by the CMX602A to shift the next data bit from the shift register onto the RXD output. At the end of the eighth pulse, the FSK Demodulator output will be reconnected to the RXD output pin. The \overline{IRQ} output will be cleared the first time the RXCLK input goes high.

Thus to use the Data Retiming function, the RXCLK input should be kept low until the \overline{IRQ} output goes low; if the Data Retiming function is not required the RXCLK input should continuously be kept high.

The only restrictions on the timing of the RXCLK waveform are those shown in Figure 7 and the need to complete the transfer of all eight bits into the μC within 8.3ms (to empty the buffer before the next character is received and put into the buffer).



t_D = Internal CMX602A delay (max 1 μ S); t_{CLO} = RXCLK low time (min 1 μ S); t_{CHI} = RXCLK high time (min 1 μ S)

Figure 7: FSK Operation with Data Retiming

Note: If enabled, the Data Retiming block will interpret the FSK Channel Seizure signal (a sequence of alternating mark and space bits) as valid received characters, with values of 55 (hex). Similarly it may interpret speech or other signals as random characters.

4.7 FSK Data Without Retiming

If the Data Retiming facility is not required, the RXCLK input to the CMX602A should continuously be kept high. The asynchronous data from the FSK Demodulator is then connected directly to the RXD output pin and the $\overline{\text{TRQ}}$ output will not be activated by the FSK signal. This case is illustrated in Figure 8.

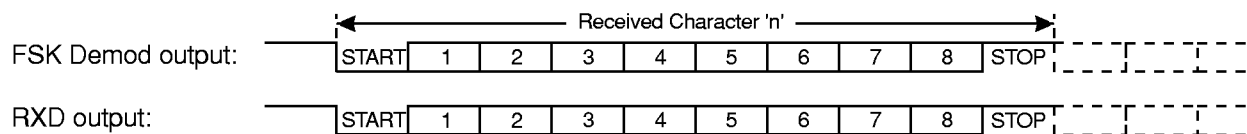


Figure 8: FSK Operation without Data Retiming (RXCLK always high)

4.8 Tone Alert Detector

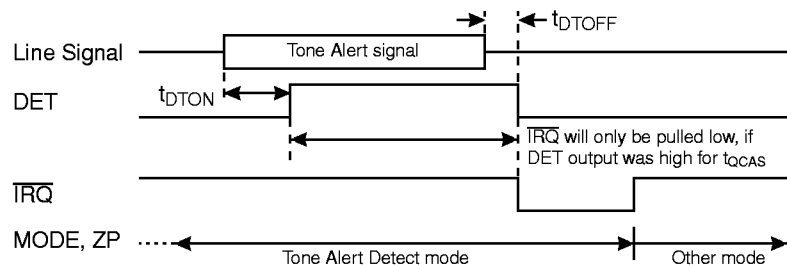
The Tone Alert Detector block is enabled when the CMX602A is set to Tone Alert Detector operating mode. It then monitors the received signal for the presence of simultaneous 2130Hz and 2750Hz tones of sufficient level and duration.

Two digital bandpass filters, centered around 2130Hz and 2750Hz, are used within the block to provide additional rejection of interfering signals.

The CMX602A DET output will be set high while Tone Alert signal is detected.

When DET goes low at the end of the Tone Alert signal, the $\overline{\text{IRQ}}$ output will be pulled low, only if DET was high for a period of time falling within the CAS qualifying time (t_{QCAS}) limits (See Section 6.1). $\overline{\text{IRQ}}$ will remain low until the CMX602A is switched out of Tone Detect mode. This $\overline{\text{IRQ}}$ falling transition indicates a valid CAS dual-tone has occurred.

Note: The t_{QCAS} timing has been optimized for the detection of 75 to 85ms CPE Alert Signals (CAS) used in off-hook applications. The longer (88ms to 110ms) Tone Alert signal employed by British Telecom for on-hook applications will not necessarily cause $\overline{\text{IRQ}}$ to go low.



See Section 6.1 for definitions of t_{DTON} , t_{DTOFF} and t_{QCAS}

Figure 9: Tone Alert Detector Operation

4.9 Ring or Line Polarity Reversal Detector

These circuits are used to detect the Line Polarity Reversal and Ringing signals associated with the Calling Line Identification protocol. Figure 10 illustrates their use in a typical application.

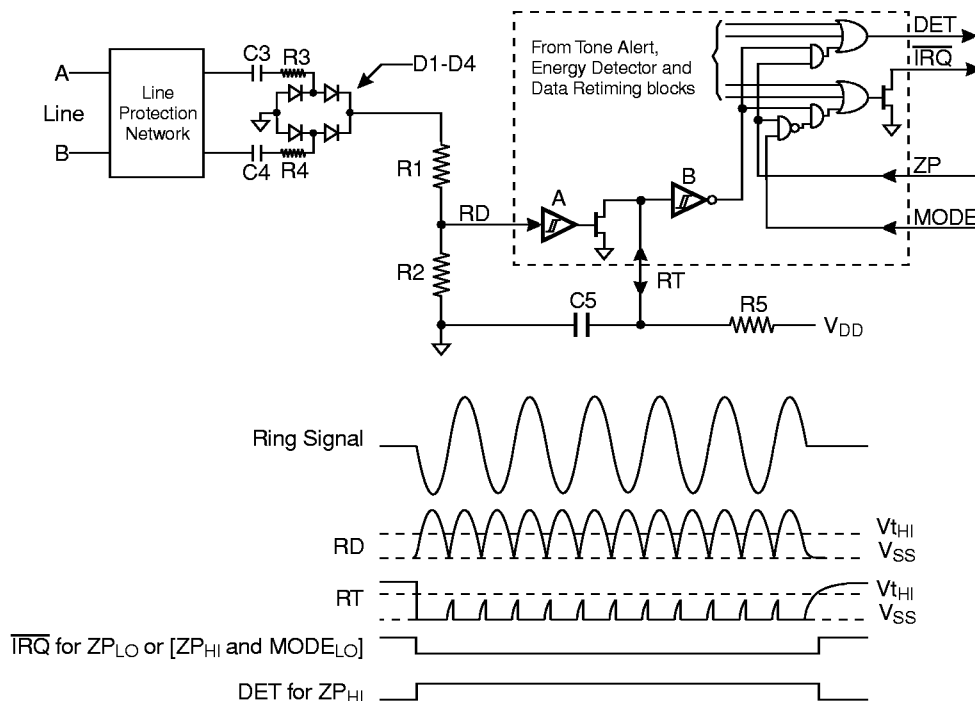


Figure 10: Ring or Line Polarity Reversal Operation

When no signal is present on the telephone line, RD will be at V_{SS} and RT pulled to V_{DD} by R5 so the output of the Schmitt trigger 'B' will be low.

The ring signal is usually applied at the subscriber's exchange as an ac voltage. The ring signal is inserted in series with one of the telephone wires and will pass through either C3 and R3 or C4 and R4 to appear at the top end of R1 in a rectified and attenuated form.

The signal prior to R1 will be further attenuated by the potential divider formed by R1 and R2 before being applied to the CMX602A input RD. If the amplitude of the signal appearing at RD is greater than the input threshold (V_{tHI}) of Schmitt trigger 'A' then the N transistor connected to RT will be turned on, pulling the voltage at RT to V_{SS} by discharging the external capacitor C5. The output of the Schmitt trigger 'B' will then go high, activating the DET and/or \overline{IRQ} outputs depending on the states of the MODE and ZP inputs.

The minimum amplitude ringing signal that is certain to be detected is:

$$\left(0.7 + V_{tHI} \frac{(R1 + R2 + R3)}{R2}\right)(0.707V_{RMS})$$

Where V_{tHI} is the high-going threshold voltage of the Schmitt trigger A (see Section 6.1).

With R1, R3 and R4 all 470k Ω as indicated in Figure 2, then setting R2 to 68k Ω will guarantee detection of ringing signals of 40V_{RMS} and above for $V_{DD} = 2.7$ to 5.5V.

A line polarity reversal may be detected using the same circuit but there will be only one pulse at RD. The British Telecom specification SIN242 indicates that the circuit must detect a +15V to -15V reversal between the two lines slewing in 30ms. For a linearly changing voltage at the input to C3 (or C4), then the voltage appearing at the RD pin will be

$$\frac{dV}{dt} C3 \left(1 - e^{-\frac{t}{T}}\right) R2$$

where $T = C3(R1 + R2 + R3)$ and $\frac{dV}{dt}$ is the input slew rate.

For $dV/dt = 500V/sec$ (15V in 30ms), R1, R3 and R4 all 470k Ω and C3, C4 both 0.1 μF as indicated in Figure 2, then setting R2 to 390k Ω will guarantee detection at $V_{DD} = 5.5V$.

If the time constant of R5 and C5 is large enough then the voltage on RT will remain below the threshold of the 'B' Schmitt trigger keeping the DET and/or \overline{IRQ} outputs active for the duration of a ring cycle

The time for the voltage on RT to charge from V_{SS} towards V_{DD} can be derived from the formula

$$V_{RT} = V_{DD} \left(1 - e^{-\frac{t}{R5C5}}\right)$$

As the Schmitt trigger high-going input threshold voltage (V_{tHI}) has a minimum value of $0.56 \times V_{DD}$, then the Schmitt trigger 'B' output will remain high for a time of at least $0.821 \times R5 \times C5$ following a pulse at RD.

Using the values provided in Figure 2 (470k Ω and 0.33 μF) gives a minimum time of 100ms (independent of V_{DD}), which is adequate for ring frequencies of 10Hz or above.

If necessary, the μC can distinguish between a ring and a reversal by timing the length of the \overline{IRQ} or DET output.

4.10 Xtal Osc and Clock Dividers

A 3.579545MHz clock present at the XTAL pin determines frequency and timing accuracy of the CMX602A. This may be generated by the on-chip oscillator inverter using the external components C1, C2, and X1 of Figure 2, or may be supplied from an external source to the XTAL input, in which case C1, C2, and X1 should not be fitted.

The oscillator is turned off in the 'Zero-Power' modes.

If the clock is provided by an external source which is not always running, then the ZP input must be set high when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by CMX602A as well as generating undefined states of the RXD, DET, and $\overline{\text{IRQ}}$ outputs.

5. Application

5.1 Calling Identity Delivery on Call Waiting (CIDCW) Application

The CMX602A supports Calling Line ID subscriber line protocols based on either the Bell 202 or CCITT V23 1200 baud FSK signaling for on hook (Type 1) and off-hook (Type 2) data transmission.

Within the Bell 202 and V.23 protocols the most difficult aspect of designing CIDCW equipment is that of correctly detecting the CAS CPE Alerting Signal in the presence of speech signals, as required within the Bellcore specifications.

This application provides guidance, suggestions, and an example circuit design to incorporate the CMX602A within the telephone unit.

5.1.1 Glossary of terms

Terms	Description
CAS	Dual-tone CPE Alerting Signal as defined in SR-TSV-002476.
CID	Calling Identity Delivery System (Bellcore).
CIDCW	Calling Identity Delivery on Call Waiting, see Bellcore Documents GR-30-CORE, and SR-TSV-002476.
CLIP	Calling Line Delivery Presentation (British Telecom)
CPE	Customer Premise Equipment i.e. the telephone set.
dBm	Signal level measurement, as used here 0dBm = 775mV _{RMS}
Hook Switch	The switch in a telephone which is operated when the handset is placed in the cradle.
On-Hook	The condition when the CPE is not being used i.e. the telephone handset is placed on the cradle, operating the hook switch.
Off-Hook	The condition when the CPE is in use i.e. the telephone handset is removed from the cradle, releasing the hook switch.

5.1.2 Requirements

Bellcore Special Report SR-TSV-002476 includes a test plan for CPE Alerting Signal Detectors, which defines three categories of test:

1. Signal Recognition Test without speech present.
2. Talkdown Test – missed signals in the presence of speech,
3. Talkoff Test - false detection's caused by speech.

The CMX602A will meet the requirements of the Signal Recognition Test without any problem. However, it will not meet the requirements of the Talkdown Test and the Talkoff Test if connected directly across the tip and ring of the 2-wire telephone line. This is because of the relatively high level of locally generated (near end) speech. (SR-TSV-002476 states that the average level of near end speech is 9dB higher than the average level of far end speech when both are measured at the tip and ring of the CPE).

These high near end speech levels can be too great to allow successful detection of the CAS Signals, and are more likely to give rise to false detection's.

A 2 to 4-wire hybrid is required to reduce the level of near end speech appearing at the CMX602A's input when it is in CAS detect mode. This should ideally provide about 16dB rejection of the near end speech although significant performance gains can be achieved with as little as 7dB.

5.1.4 Software

In Figure 12 a successful CIDCW transaction is shown using the circuit shown in Figure 11 and the 'off-hook' control algorithm described in Section 5.3.

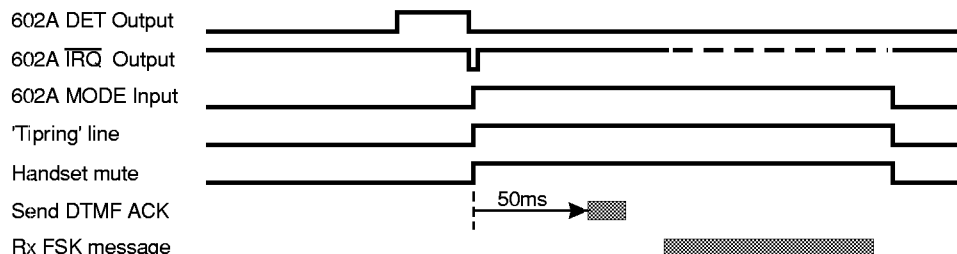


Figure 12: Successful CIDCW Transaction using the Circuit found in Figure 11

While looking for a CAS signal, the CMX602A is running in Tone Detect Mode (MODE Input low), with its input connected to the RX Speech. In this state the CMX602A's DET output directly controls the Microphone Mute line as required by the Data Sheet Algorithm. The DET output serves no other purpose at this stage.

CAS signal detection is indicated by the CMX602A's $\overline{\text{TRQ}}$ output going low. When this happens the μC should:

1. Set the CMX602A to FSK Mode by taking the MODE pin high (this will also clear the $\overline{\text{TRQ}}$ output).
2. Completely mute the local handset and keypad.
3. Set the Tipring line high, so that the CMX602A is connected directly across tip and ring (as the Rx Speech output of the phone circuits will now be muted).
4. Start a 50ms timer.

In the 50ms period between setting the CMX602A into the FSK mode and sending the ACK signal, the CMX602A's DET output should be monitored and the transaction terminated if the line goes high during this time, as described in Section 5.3.

At the end of the 50ms period, a DTMF ACK should be sent, after which the FSK message containing the waiting caller's ID will be received by the CMX602A. At the end of the message, the μC should set the CMX602A back into the 'looking for CAS' mode by taking the MODE and Tipring lines low and removing the local handset and keypad mute.

5.1.5 Printed Circuit Layout

The CMX602 is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} decoupling and V_{BIAS} decoupling are very important.

It is recommended that decoupling capacitors be placed so that connections between them and the device pins are as short as practicable and via a printed circuit ground plane, which can also be laid out to shield the receive path from interfering signals.

5.1.6 High Frequency Interfering Signals

The CMX602A input filter uses switched capacitor technology running at 57.7kHz and is therefore sensitive to input signals at multiples of this frequency.

A linear anti-alias filter is included on chip between the output of the Input Signal Amplifier and the input to the switched capacitor filter. This should provide adequate attenuation of out of band signals for most applications. Additional attenuation may be added if necessary. This can be accomplished by adding a 22pF capacitor in parallel with the input amplifier feedback resistor R8.

5.1.7 If the Ring Detect Circuit is not Used

The RD pin should be connected to V_{SS} and RT to V_{DD} .

5.1.8 Common Mode Interface

The interface circuits between the telephone line and the CMX602A as shown in figure XXX have been designed to reduce the effects of common mode noise voltages appearing between the line and the CMX602A's ground connection (VSS pin). However, excessive levels of common mode noise can cause the problems with the detection of the ringing signal or the line polarity reversal, with reception of CAS, the Tone Alert signal used in British Telecom's CLIP system, and FSK data signals.

The extent of the problem depends mainly on the power supply used for the CMX602A and the connection (if any) between this power supply and the tip and ring lines.

5.2 'On-Hook' Operation

The systems described in this section operate when the telephone set is not in use (on-hook) to display the number of a calling party before the call is answered. System specific descriptions are provided as well as a flowchart for on-hook applications (Figure 15).

5.2.1 Bellcore System

Figure 13 illustrates the line signaling and CMX602A input and output signals for the Bellcore 'On-Hook' Caller ID system as defined in Bellcore documents GR-30-CORE and SR-TSV-002476 and also in ETS 300 659-1 Section 6.1.1.

As for the British Telecom system, the 'Chan Seize' signal is a '1010...' FSK bit sequence. The Bellcore specifications do not require AC or DC line terminations while the FSK data is being received, however ETS 300 659-1 allows for the possibility of an AC termination begin applied.

Note: For simplicity of presentation, the Data Retiming function is not used in Figure 13 (RXCLK is kept high).

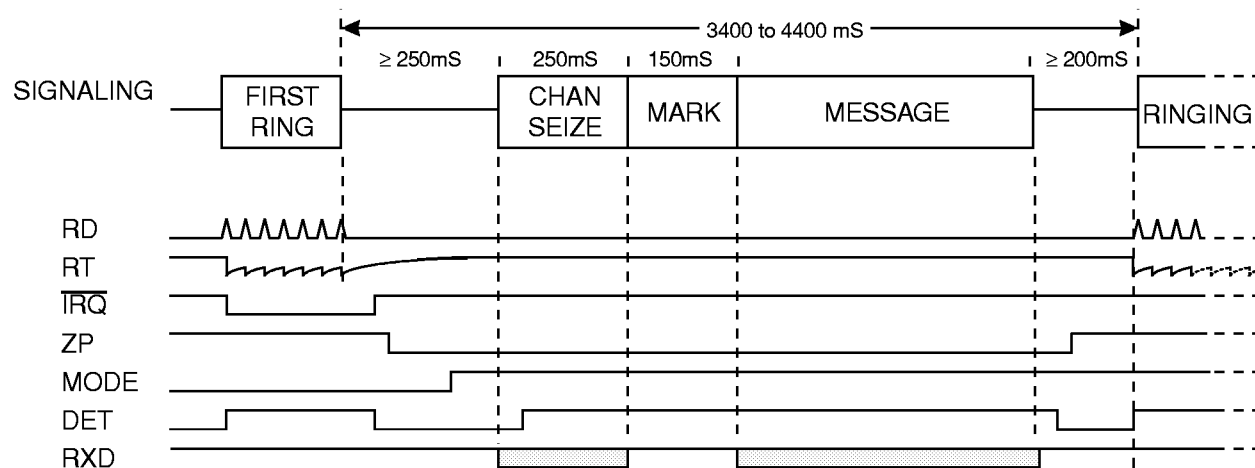


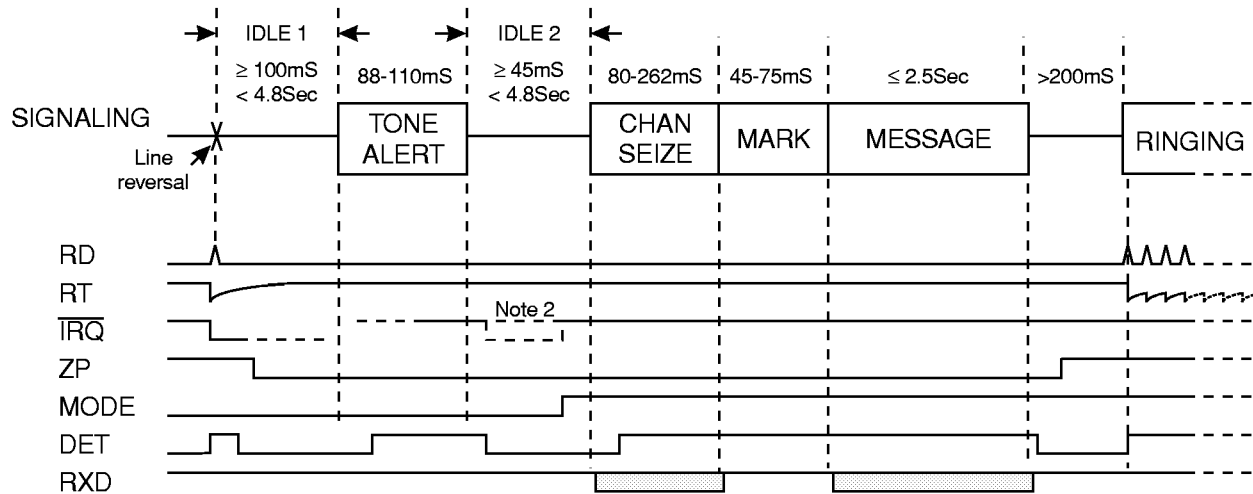
Figure 13: Bellcore System Signals

5.2.2 British Telecom System

Figure 12 illustrates the line signaling and CMX602A input and output signals for the British Telecom 'On-Hook' Caller ID system as defined in the British Telecom specifications SIN227 and SIN242 part 1. A similar system is described in ETSI 300 659-1 Section 6.1.2c.

The Tone Alert signal consists of simultaneous 2130Hz and 2750Hz tones. The 'Chan Seize' signal consists of a '1010..' FSK bit sequence. Not shown are the requirements for AC and DC loads, including a short initial Current Wetting Pulse, to be applied to the line 20ms after the end of the Tone Alert signal and to be maintained during reception of the FSK signal.

Note: For simplicity of presentation, the Data Retiming function is not used in Figure 14 (RXCLK is kept high).



Notes:

1. IDLE 1 + IDLE 2 ≤ 5 sec
2. TRQ may go low at end of DET high period but this is not guaranteed.

Figure 14: British Telecom System Signals

5.2.3 Other 'On-Hook' Systems

ETS 300 659-1 also allows for systems where the FSK transmission is preceded by a Dual Tone Alert signal similar to that used by British Telecom but without line reversal (ETS 300 659-1 Section 6.1.2a) or by a Ringing Pulse alerting Signal (ETS 300 659-1 Section 6.1.2b).

The U.K. CCA (Cable Communications Association) specification TW/P&E/312 precedes the FSK signals by a 200 to 450ms ring burst. AC and DC line terminations during FSK reception are optional.

Mercury Communications Ltd. Specification MNR 19 allows for either the British Telecom system or that specified by CCA.

As these are all slight variants on the Bellcore and British Telecom systems, they can also be supported by the CMX602A.

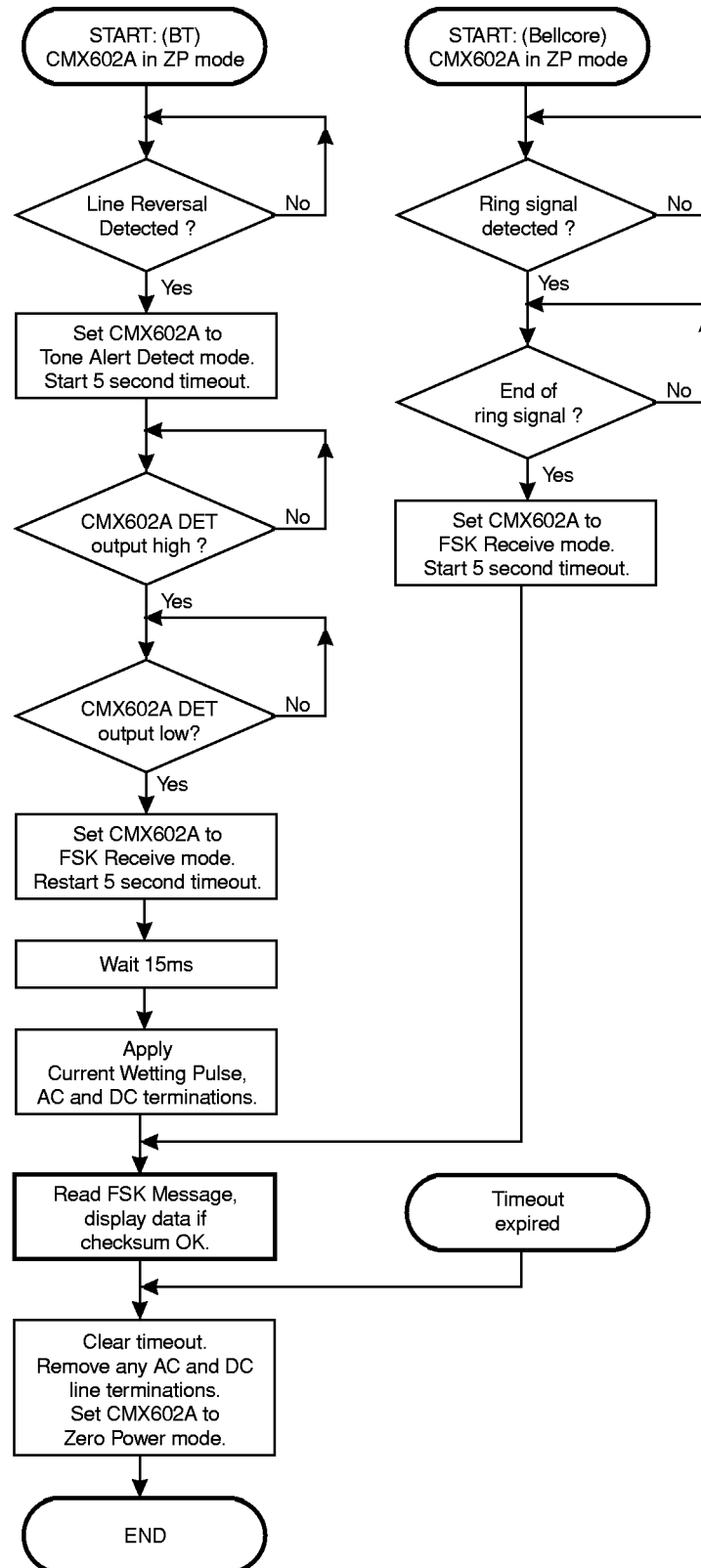
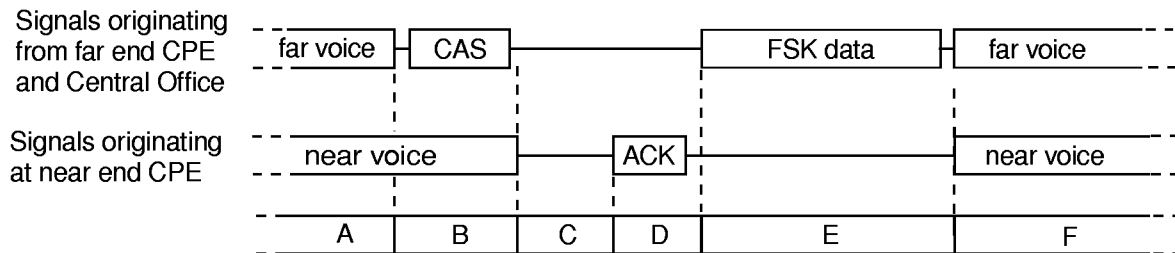


Figure 15: Flow Chart for 'On-Hook' Operation of CMX602A

5.3 'Off-Hook' Operation

The CIDCW (Calling Identity on Call Waiting) system, as described in this section, operates when the telephone set is in use (off-hook) to display the number of a waiting caller without interrupting the current call. Bellcore documents GR-30-CORE and SR-TSV-002476, British Telecom specifications SIN227 and SIN242 part 2 and ETS 300-659-2 all describe similar systems in which a successful CIDCW transaction consists of a sequence of actions between the near end CPE (Customer Premises Equipment - e.g. a telephone) and the Central Office as indicated in Figure 16.



- Normal conversation with both near and far voice present.
- Central Office mutes far end voice, emits CAS, and becomes silent.
- CPE recognizes CIDCW initiation and mutes near end voice and keypad.
- CPE emits DTMF ACK to Central Office to signal its readiness to receive Caller ID data stream.
- Central Office recognizes ACK and emits FSK Data stream of Caller ID data which is received and decoded by CPE.
- CIDCW transaction is complete. CPE unmutes near end voice and Central Office unmutes far end voice returning to normal conversation with both near and far voice present.

Figure 16 CIDCW Transaction From Near End CPE Perspective

The CAS signal is transmitted by the Central Office to initiate a CIDCW transaction and consists of an 80ms burst of simultaneous 2130Hz and 2750Hz tones.

CAS detection is very important because a 'missed' signal causes Caller ID information to be lost and a false signal detection produces a disruptive tone which is heard by the far end caller. Because the CAS signals must be detected in the presence of conversations, which both mask and masquerade as the tone signals, this function is difficult to accomplish correctly.

Because the number of false responses (Talk-offs) and missed signals (Talk-downs) are related to the speech levels at the CMX602A input, the level of near end speech from the local handset is normally greater than that of far end speech coming from the Central Office. A further improvement in overall performance can be obtained by taking the CMX602A's audio input from the receive side of the telephone set hybrid where this is possible.

The internal algorithms used by the CMX602A to drive the DET and $\overline{\text{IRQ}}$ outputs in Tone Alert Detect mode have been optimized for the detection of off-hook CAS signals in the presence of speech when used according to the following principles:

- If it is possible to mute the local speech from the microphone rapidly (within 0.5ms) without introducing noise (i.e. where the CIDCW equipment is built into the telephone set), then this muting should be done whenever the CMX602A is in Tone Alert Detect mode and the DET output is high. Doing this will markedly reduce the number of false responses generated by local (near end) speech. Note that the DET output is not used for any other purpose in an off-hook application when the CMX602A is set to Tone Alert Detect mode.
- When the $\overline{\text{IRQ}}$ output goes low in Tone Alert Detect mode, this indicates that a CAS has been detected. The local handset and keypad should then be muted as required by the Bellcore specification and the CMX602A switched to FSK Receive mode to be ready to receive the FSK data. Doing this will also clear the $\overline{\text{IRQ}}$ output.
- The CMX602A's DET output should be monitored for a period of 50ms after changing to FSK Receive mode and before sending the ACK signal. The transaction should be abandoned if the DET output goes high during this time, which would be the case if a false CAS detect had been caused by far end speech.

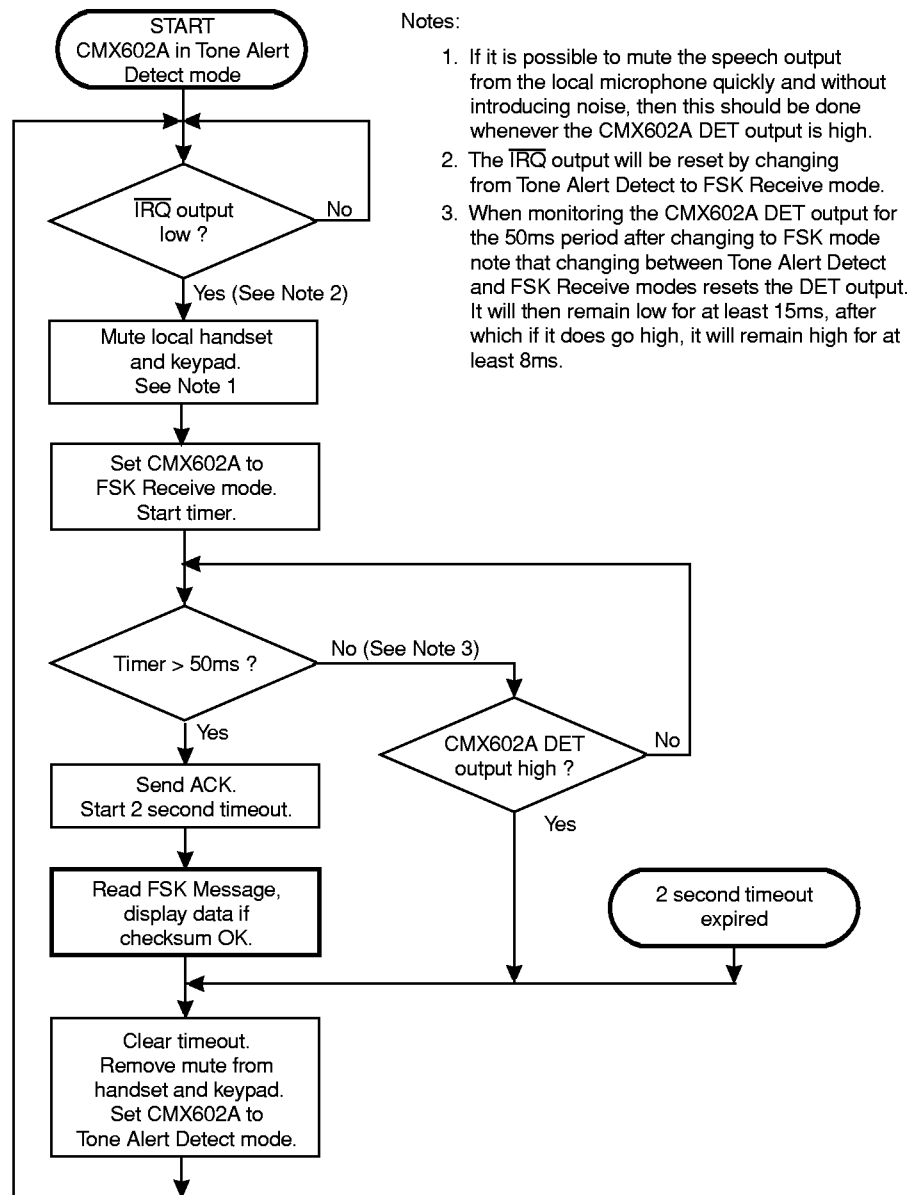


Figure 17, Flow Chart for 'Off-Hook' Operation of CMX602A

6. Performance Specification

6.1 Electrical Performance

6.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	$V_{DD} + 0.3$	V
Current into or out of V_{DD} and V_{SS} pins	-30	30	mA
Current into or out of any other pin	-20	20	mA
D4 / P3 Package			
Total Allowable Power Dissipation at $T_{AMB} = 25^{\circ}\text{C}$		800	mW
Derating above 25°C		13	mW/ $^{\circ}\text{C}$ above 25°C
Storage Temperature	-55	125	$^{\circ}\text{C}$
Operating Temperature	-40	85	$^{\circ}\text{C}$

6.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply ($V_{DD} - V_{SS}$)	1	2.7	5.5	V
Operating Temperature	1	-40	85	$^{\circ}\text{C}$
Xtal frequency	2	3.575965	3.583125	MHz

Operating Limits Notes:

1. Operating temperature range -10°C to 60°C at $V_{DD} < 3.0\text{V}$.
2. A Xtal frequency of $3.579545\text{MHz} \pm 0.1\%$ is required for correct Tone Alert and FSK detection.

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

$V_{DD} = 2.7V$ at $T_{AMB} = 10^{\circ}C$ to $60^{\circ}C$ and $V_{DD} = 3.0V$ to $5.0V$ at $T_{AMB} = -40^{\circ}C$ to $85^{\circ}C$

Xtal Frequency = $3.579545MHz \pm 0.1\%$, 0dBV corresponds to $1.0V_{RMS}$

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (ZP input high) at $V_{DD} = 5.0V$	1,2		0.02	1.0	μA
I_{DD} (ZP input low) at $V_{DD} = 3.0V$	1		0.5	1.0	mA
I_{DD} (ZP input low) at $V_{DD} = 5.0V$	1		1.0	2.0	mA
Logic 1 input level (RXCLK and XTAL inputs)		70%			V_{DD}
Logic 0 input level (RXCLK and XTAL inputs)				30%	V_{DD}
Logic input leakage current ($V_{IN} = 0$ to V_{DD}) excluding XTAL input		-1.0		1.0	μA
Output logic 1 level ($I_{OH} = 360\mu A$)		$V_{DD} - 0.4$			V
Output logic 0 level ($I_{OL} = 360\mu A$)				0.4	V
\overline{IRQ} output 'off' state current ($V_{OUT} = V_{DD}$)				1.0	μA
Schmitt Trigger input thresholds (Figure 18)					
High going (V_{tHI})		$(0.56)(V_{DD})$		$(0.56)(V_{DD}) + 0.6$	V
Low going (V_{tLO})		$(0.44)(V_{DD}) - 0.6$		$(0.44)(V_{DD})$	V
Tone Alert Detector					
'Low' tone nominal frequency			2130		Hz
'High' tone nominal frequency			2750		Hz
Start of Tone Alert signal to DET high time (t_{DTON} Figure 9)			55.0		ms
End of Tone Alert signal to DET and \overline{IRQ} low time (t_{DTOFF} Figure 9)		0.5		10.0	ms
DET high time to ensure \overline{IRQ} goes low (t_{QCAS} see Figure 9)		8.0		45.0	ms
To ensure detection:	3				
'Low' tone frequency deviation from nominal				± 20	Hz
'High' tone frequency deviation from nominal				± 30	Hz
Tone level of each simultaneously applied tone	4	-40.0		-2.2	dBV
2750Hz tone level with respect to 2130Hz tone level		-7.0		7.0	dB
Signal to Noise ratio	5	20.0			dB
Dual Tone Burst Duration for DET output		75			ms
Dual Tone Burst Duration to ensure \overline{IRQ} goes low		75		85	ms

	Notes	Min.	Typ.	Max.	Units
To ensure non-detection:	6				
'Low' tone frequency deviation from nominal		±75			Hz
'High' tone frequency deviation from nominal		±95			Hz
Level (total)	4			-46.0	dBV
Dual Tone Burst Duration				45.0	ms
FSK Receiver					
Transmission rate		1188	1200	1212	Baud
V23 Mark (logic 1) frequency		1280	1300	1320	Hz
V23 Space (logic 0) frequency		2068	2100	2132	Hz
Bell202 Mark (logic 1) frequency		1188	1200	1212	Hz
Bell202 Space (logic 0) frequency		2178	2200	2222	Hz
Valid input level range	4	-40.0		-8.0	dBV
Acceptable twist (mark level with respect to space level)					
V23		-7.0		7.0	dB
Bell202		-10.0		10.0	dB
Acceptable Signal to Noise ratio					
V23	5	20.0			dB
Bell202	5	30.0			dB
Level Detector 'on' threshold level	4			-40.0	dBV
Level Detector 'off' to 'on' time (t_{DFON} Figure 6)				25.0	ms
Level Detector 'on' to 'off' time (t_{DFOFF} Figure 6)		8.0			ms
Input Signal Amplifier					
Input impedance	7	10.0			MΩ
Voltage gain			500		V/V
XTAL Input					
'High' pulse width	8	100			ns
'Low' pulse width	8	100			ns

Operating Characteristics Notes:

1. At 25°C, not including any current drawn from the CMX602A pins by external circuitry other than X1, C1, and C2.
2. RD, MODE, RXCLK inputs at V_{SS} , ZP input at V_{DD} . See Figure 19.
3. All conditions must be met to ensure detection.
4. For $V_{DD} = 5.0V$ with equal level tones and with the input signal amplifier external components as shown in Section 3. The internal threshold levels are proportional to V_{DD} . For other supply voltages or different signal level ranges the voltage gain of the input signal amplifier should be adjusted by selecting the appropriate external components as described in Section 4.2
5. Flat Noise in the 300Hz-3400Hz band for V23 and 200Hz-3200Hz for Bell202.
6. Meeting any of these conditions will ensure non-detection.
7. Open loop, small signal, low frequency measurements.
8. Timing for an external input to the XTAL pin.

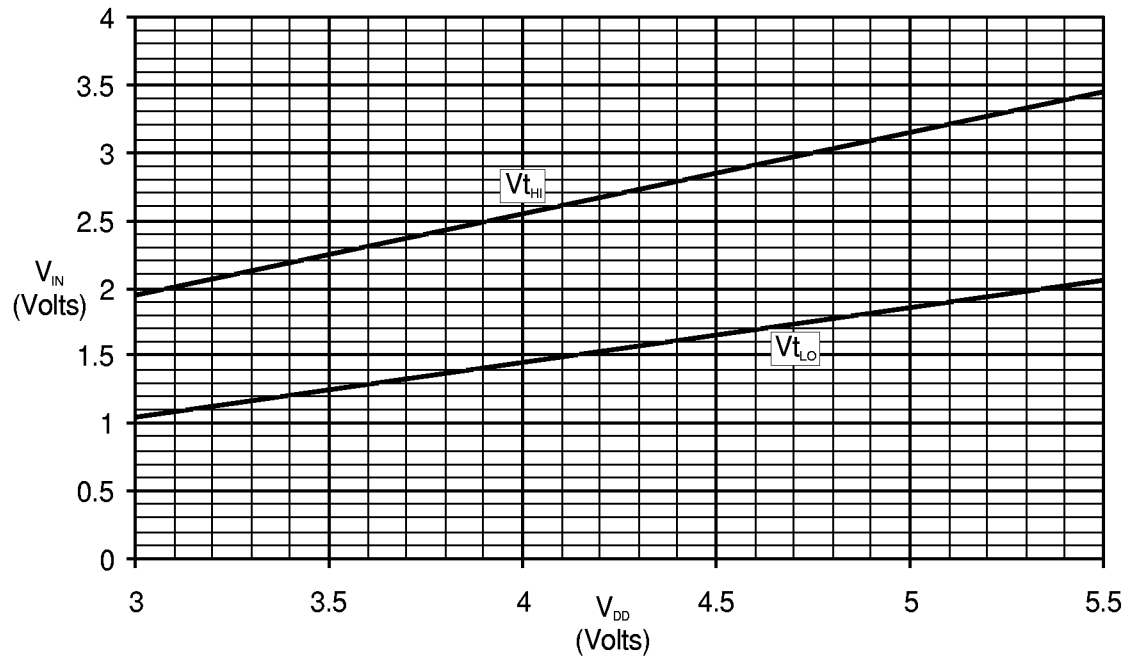


Figure 18: Schmitt Trigger typical input voltage thresholds vs. V_{DD}

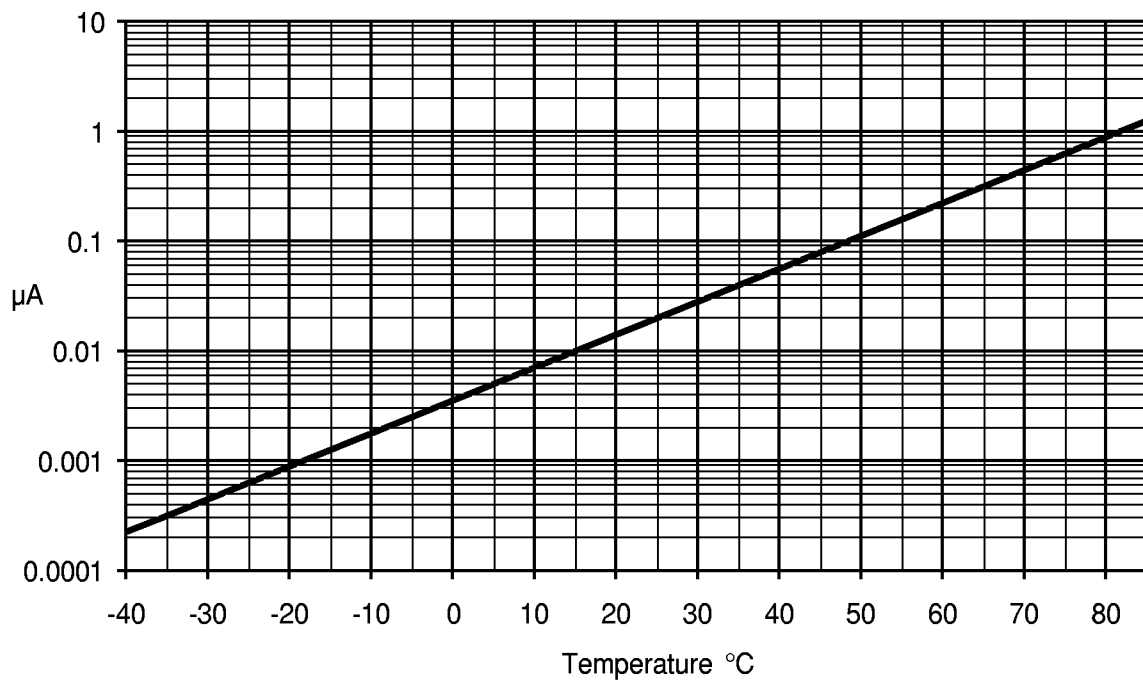


Figure 19: Typical 'Zero-Power' I_{DD} vs. Temperature ($V_{DD} = 5.0V$)

6.2 Packaging

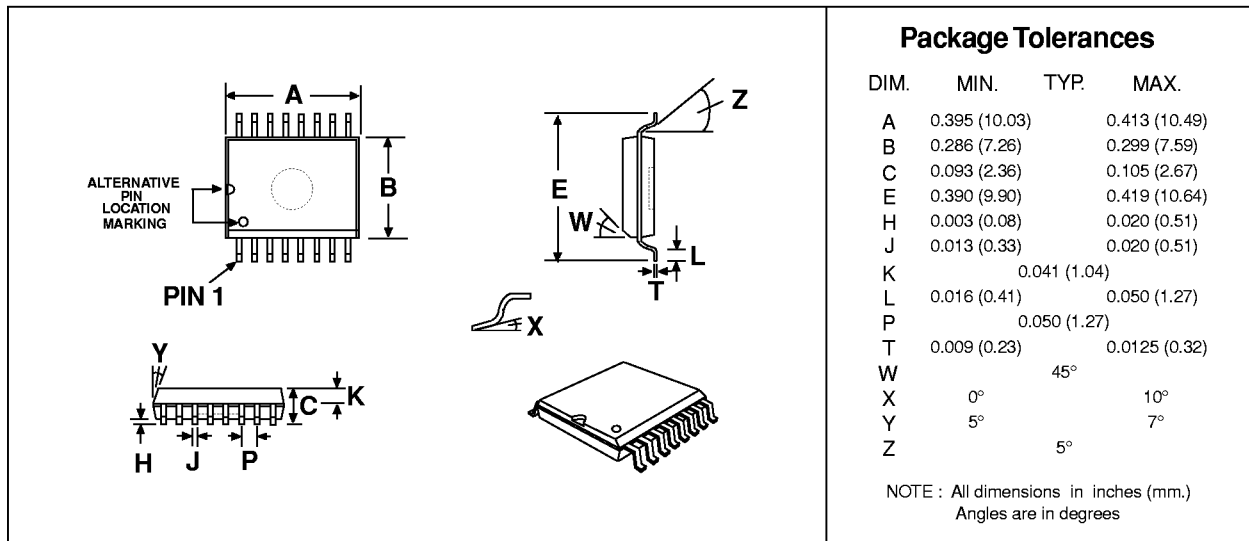


Figure 20 : 16-pin SOIC Mechanical Outline: *Order as part no. CMX602AD4*

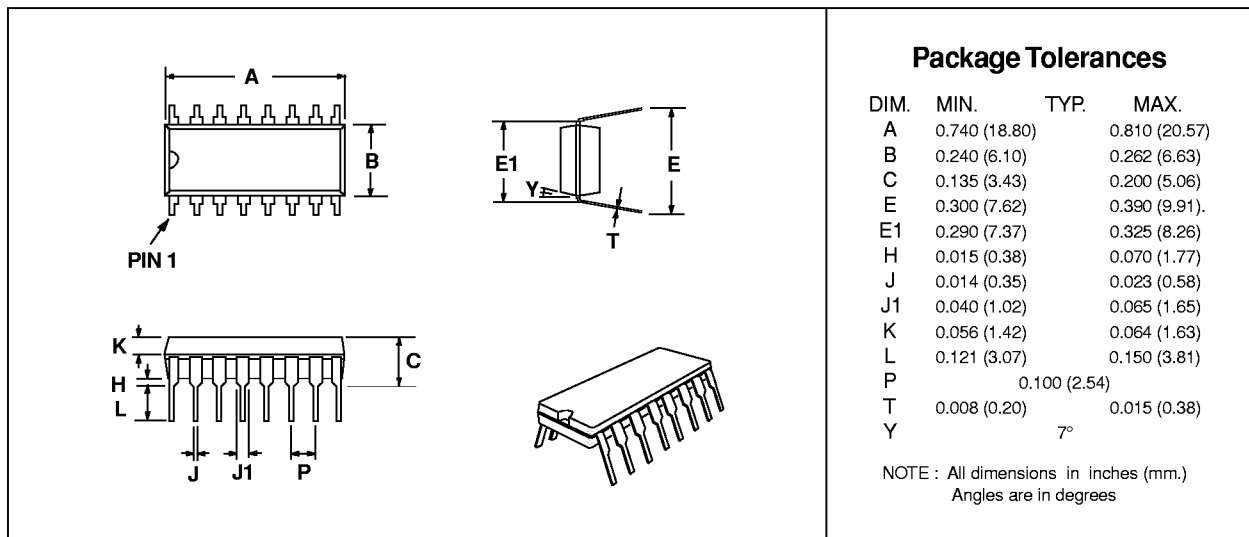


Figure 21 : 16-pin PDIP Mechanical Outline: *Order as part no. CMX602AP3*