DATASHEET

REVISION 9/22/21

Dual Driver and Receiver

UT54LVDM055LV

Features

- Two drivers and two receivers with individual enables
- >400.0 Mbps (200 MHz) switching rates
- ±340mV differential signaling
- 3.3 V power supply
- TTL compatible inputs
- 10mA LVDS output drivers
- TTL compatible outputs
- Cold spare all pins
- Ultra low power CMOS technology
- Operational environment; total dose irradiation testing to MIL- STD-883 Method 1019
  - Total dose: 300 krad(Si)
  - Latchup immune (LET ≤100 MeV-cm^2/mg)
- Packaging options:
  - 18-lead flatpack (0.8 grams)
- Standard Microcircuit Drawing 5962-06202
  - QML Q and V compliant part
- Compatible with TIA/EIA-899

Introduction

The UT54LVDM055LV Dual Driver/Dual Receiver is designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400.0 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The UT54LVDM055LV Driver accepts low voltage TTL input levels and translates them to low voltage (350mV) differential output signals. In addition, the driver supports a three-state function that may be used to disable the output stage, disabling the load current, and thus dropping the device to a low idle power state.

The UT54LVDM055LV Receiver accepts low voltage (350mV) differential input signals and translates them to 3V CMOS output levels. The receiver supports a three-state function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (35Ω) input fail-safe. Receiver output will be HIGH for all fail-safe conditions.

All pins have Cold Spare buffers. These buffers will be high impedance when V_{DD} is tied to V_{SS}.

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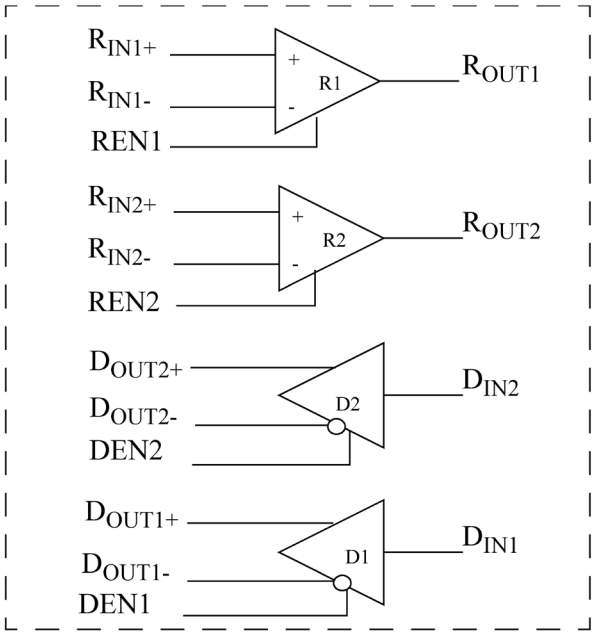

Figure 1. UT54LVDM055LV Dual Driver and Receiver Block Diagram

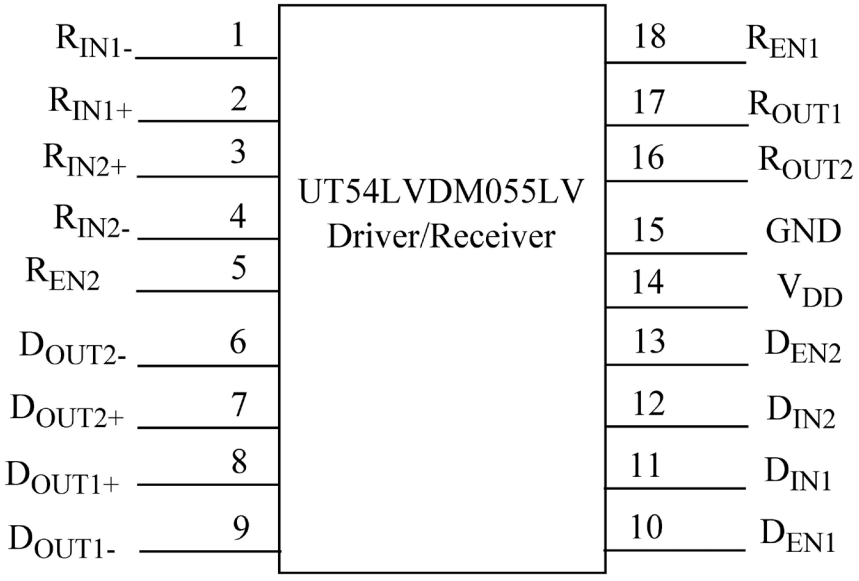

Figure 2. UT54LVDM055LV Pinout

Dual Driver and Receiver

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Truth Table

Enables	Input	Output	
D_{EN}	D_{IN}	D_{OUT+}	D_{OUT-}
L	X	Z	Z
H	L	L	H
	H	H	L

Enables	Input	Output
R_{EN}	R_{IN+} - R_{IN-}	R_{OUT}
L	X	Z
H	$V_{ID} \geq 0.1V$	H
	$V_{ID} \leq -0.1V$	L
	Full Fail-safe OPEN/SHORT or Terminated	H

Pin Description

Pin No.	Name	Description
11, 12	D_{IN}	Driver input pin, TTL/CMOS compatible
7, 8	D_{OUT+}	Non-inverting driver output pin, LVDS levels
6, 9	D_{OUT-}	Inverting driver output pin, LVDS levels
10, 13	D_{EN}	Driver active high enable pin
2, 5	R_{IN+}	Non-inverting receiver input pin
1, 4	R_{IN-}	Inverting receiver input pin
16, 17	R_{OUT}	Receiver output pin
5, 18	R_{EN}	Receiver active high enable pin
14	V_{DD}	Power supply pin, +3.3 ± 0.3V
15	V_{SS}	Ground pin

Applications Information

The UT54LVDM055LV provides two drivers and two receivers in the same package. Each driver and each receiver has a dedicated output enable pin. This allows maximum flexibility for the device.

The intended application of these devices and signaling technique is for both point-to-point (single termination) and multipoint (double termination) data transmissions over controlled impedance media. The transmission media may be printed-circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application specific characteristics.)

The UT54LVMS055LV differential line driver is a balanced current source design. A current mode driver, has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The current mode **requires** that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 3. AC or

unterminated configurations are not allowed. The 10mA loop current will develop a differential voltage of 350mV across the 35Ω termination resistor which the receiver detects with a 250mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (350mV - 100mV = 250mV)). The signal is centered around +1.2V (Driver Offset, VOS) with respect to ground as shown in Figure 4.

Note: The steady-state voltage (VSS) peak-to-peak swing is twice the differential voltage (VOD) and is typically 700mV.

The UT54LVDM055LV receiver's are capable of detecting signals as low as 100mV, over a +/- 1V common-mode range centered around +1.2V. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground). The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. The termination resistor converts the current sourced by the driver into voltages that are detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities, as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

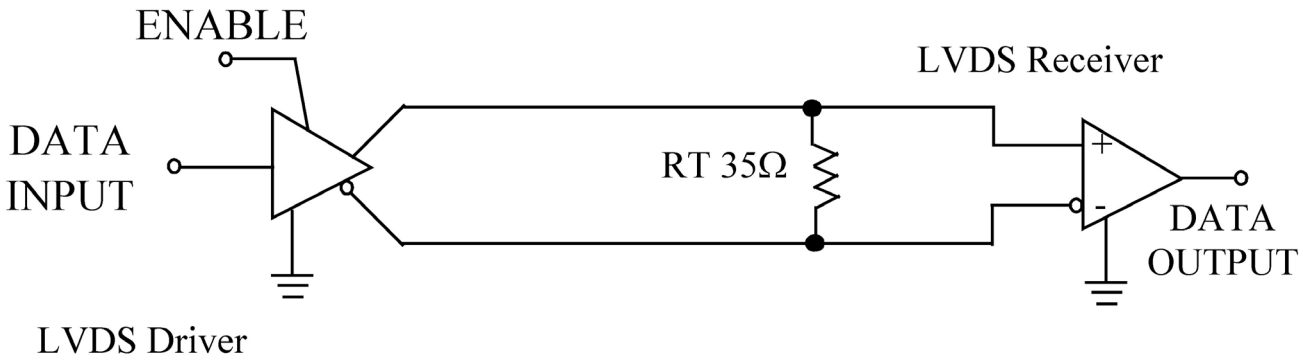

Figure 3. Point-to-Point Application

Receiver Fail-Safe

The UT54LVDM055LV receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

Open Input Pins.

The UT54LVDM055LV is a dual receiver device, and if an application requires only 1 receiver, the unused channel inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

Terminated Input.

If the driver is disconnected (cable unplugged), or if the driver is in a three-state or power-off condition,

the receiver output will again be in a HIGH state, even with the end of cable 35Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.

Shorted Inputs.

If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (V_{SS} to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	3E5	rad(Si)
Single Event Latchup (SEL)	≤100	MeV-cm^2/mg

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin during operation	-0.3 to (V_{DD} + 0.3V)
	Voltage on any pin during cold spare	-.3 to 4.0V
ESD_{HBM}	HBM ESD Rating	1000V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	1.25 W
T_J	Maximum junction temperature [2]	+150°C
Θ_{JC}	Thermal resistance, junction-to-case [3]	10°C/W
I_I	DC input current	±10mA

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) Maximum junction temperature may be increased to +175°C during burn-in and life test.
3) Test per MIL-STD-883, Method 1012.

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Recommended Operating Conditions

Symbol	Parameter	Limits
V_{DD}	Positive supply voltage	3.0 to 3.6V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage, receiver inputs DC input voltage, logic inputs	2.4V 0 to V_{DD}

DC Electrical Characteristics Driver * [1, 2, 4]

(V_{DD} = 3.3V ± 0.3V; -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IH}	High-level input voltage	(TTL)	2.0		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL}	Low-level output voltage	R_L = 35Ω	0.855		V
V_{OH}	High-level output voltage	R_L = 35Ω		1.750	V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or GND, V_{DD} = 3.6V	-5	+5	µA
I_{CS}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-10	+10	µA
V_{OD} [1]	Differential Output Voltage	R_L = 35Ω(figure 5)	250	400	mV
ΔV_{OD} [1]	Change in Magnitude of V_{OD} for Complementary Output States	R_L = 35Ω(figure 5)		35	mV
V_{OS}	Offset Voltage	R_L = 35Ω, V_{OS} =	1.055	1.550	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	R_L = 35Ω(figure5)$\left(\frac{VOH + VOL}{2}\right)$		35	mV
V_{CL}	Input clamp voltage	I_{CL} = +18mA		-1.5	V
I_{OS} [2,3]	Output Short Circuit Current	V_{IN} = V_{DD}, V_{OUT+} = 0V or V_{IN} = GND, V_{OUT-} = 0V, D_{EN} = V_{DD}		40	mA
I_{OZ}	Output Three-State Current	D_{EN} = 0.8V V_{OUT} = 0V or V_{DD}, V_{DD} = 3.6V	-5	+5	µA
I_{CCL} [4]	Loaded supply current, drivers and receivers enabled	R_L = 35Ω all channels R_{EN} = D_{EN} = V_{DD} V_{IN} = V_{DD} or V_{SS}(all inputs)		40.0	mA
I_{CCZ} [4]	Loaded supply current, drivers and receivers disabled	D_{IN} = V_{DD} or V_{SS} R_{EN} = D_{EN} = V_{SS}		15.0	mA

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.
3) Guaranteed by characterization.
4) Receivers are included for parameters I_{CCL} and I_{CCZ}.

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AC Switching Characteristics Driver*[1, 2, 3]

(V_{DD} = +3.3V ± 0.3V, T_C = -55°C to +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Parameter	MIN	MAX	Unit
t_{PHLD} [6]	Differential Propagation Delay High to Low (figures 5 and 6)	0.5	1.8	ns
t_{PLHD} [6]	Differential Propagation Delay Low to High (figures 5 and 6)	0.5	1.8	ns
t_{SKD}	Differential Skew (t_{PHLD} - t_{PLHD}) (figures 5 and 6)	0	0.4	ns
t_{SK1} [1]	Channel-to-Channel Skew (figures 5 and 6)	0	0.5	ns
t_{SK2} [5]	Chip-to-Chip Skew (figure 5 and 6)		1.3	ns
t_{TLH} [4]	Rise Time (figures 5 and 6)		1.5	ns
t_{THL} [4]	Fall Time (figures 5 and 6)		1.5	ns
t_{PHZ}	Disable Time High to Z (figures 7 and 8)		5	ns
t_{PLZ}	Disable Time Low to Z (figures 7 and 8)		5	ns
t_{PZH}	Enable Time Z to High (figures 7 and 8)		7.0	ns
t_{PZL}	Enable Time Z to Low (figures 7 and 8)		7.0	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50, $t_r \leq$ 1ns, and $t_f \leq$ 1ns.
3) C_L includes probe and jig capacitance.
4) Guaranteed by characterization
5) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
6) May be tested at higher load capacitance and the limit interpolated from characterization data to guarantee this parameter.

DC Electrical Characteristics Receiver *[1, 2, 4]

(V_{DD} = 3.3V ± 0.3V; -55°C< T_C<+125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IH}	High-level input voltage	(TTL)	2.0		V
V_{IL}	Low-level input voltage	(TTL)		0.8	V
V_{OL}	Low-level output voltage	I_{OL} = 2mA, V_{DD} = 3.0V		0.25	V
V_{OH}	High-level output voltage	I_{OH} = -0.4mA, V_{DD} = 3.0V	2.7		V
I_{IN}	Logic input leakage current	Enables = R_{EN} = 0 and 3.6V, V_{DD} = 3.6	-5	+5	µA
I_I	LVDS Receiver input Current	V_{IN} = 2.4V, V_{DD} = 3.6	-15	+15	µA
I_{CS}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD}=V_{SS}	-10	+10	µA
V_{TH} [3]	Differential Input High Threshold	V_{CM} = +1.2V		+100	mV
V_{TL} [3]	Differential Input Low Threshold	V_{CM} = +1.2V	-100		mV
I_{OZ} [3]	Output Three-State Current	Disabled, V_{OUT} = 0 V or V_{DD} R_{EN} = 0.8V	-5	+5	µA
V_{CL}	Input clamp voltage	I_{CL} = -18mA		-1.5	V
I_{OS} [2, 3]	Output Short Circuit Current	Enabled, V_{OUT} = 0 V [2] R_{EN} = V_{DD}		-75	mA

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed 1 second.
3) Guaranteed by characterization.
4) Refer to driver DC characteristics for I_{CCL} and I_{CCZ}.

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AC Switching Characteristics Receiver *[1, 2, 3]

(V_{DD} = +3.3V ± 0.3V, T_A = -55°C to +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Symbol	Parameter	MIN	MAX	Unit
t_{PHLD} [6]	Differential Propagation Delay High to Low (figures 9 and 10)	1.0	2.0	ns
t_{PLHD} [6]	Differential Propagation Delay Low to High (figures 9 and 10)	1.0	2.0	ns
t_{SKD}	Differential Skew (t_{PHLD} - t_{PLHD}) (figures 9 and 10)	0	0.35	ns
t_{SK1} [1]	Channel-to-Channel Skew (figures 9 and 10)	0	0.5	ns
t_{SK2} [5]	Chip-to-Chip Skew (figures 9 and 10)		1.0	ns
t_{TLH} [4]	Rise Time (figures 9 and 10)		1.2	ns
t_{THL} [4]	Fall Time (figures 9 and 10)		1.2	ns
t_{PHZ}	Disable Time High to Z (figures 11 and 12)		4.0	ns
t_{PLZ}	Disable Time Low to Z (figures 11 and 12)		4.0	ns
t_{PZH}	Enable Time Z to High (figures 11 and 12)		3.0	ns
t_{PZL} [7]	Enable Time Z to Low (figures 11 and 12)		3.0	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Channel-to-Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.
2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_0 = 50Ω, t_r and t_f (0% - 100%) ≤ 1ns for R_{IN} and t_r and t_f ≤ 1ns for EN or $\overline{EN}$.
3) C_L includes probe and jig capacitance.
4) Guaranteed by characterization.
5) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.
6) May be tested at higher load capacitance and the limit interpolated from characterization data to guarantee this parameter.
7) During t_{PZL} the output may transition High before going Low.

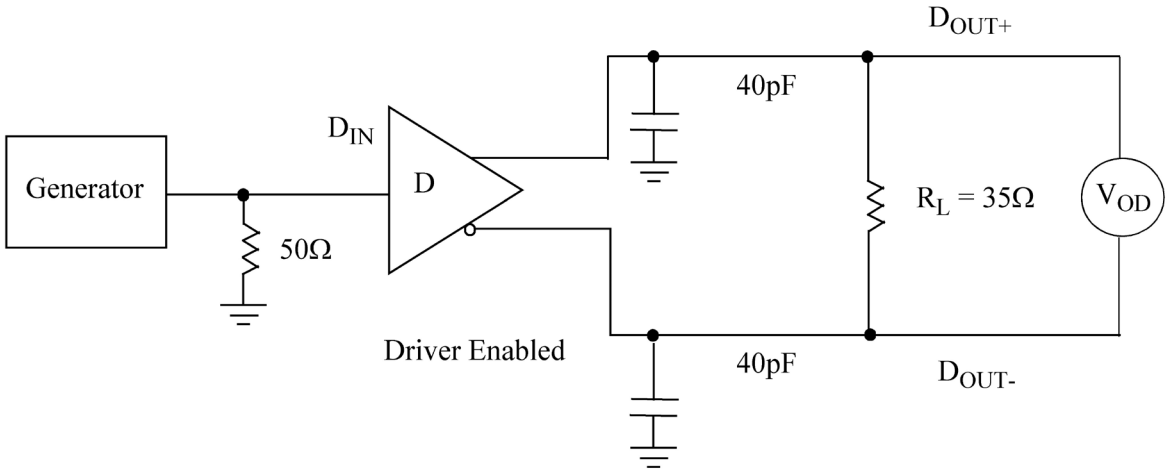

Figure 4. Driver V_{OD} and V_{OS} Test Circuit or Equivalent Circuit

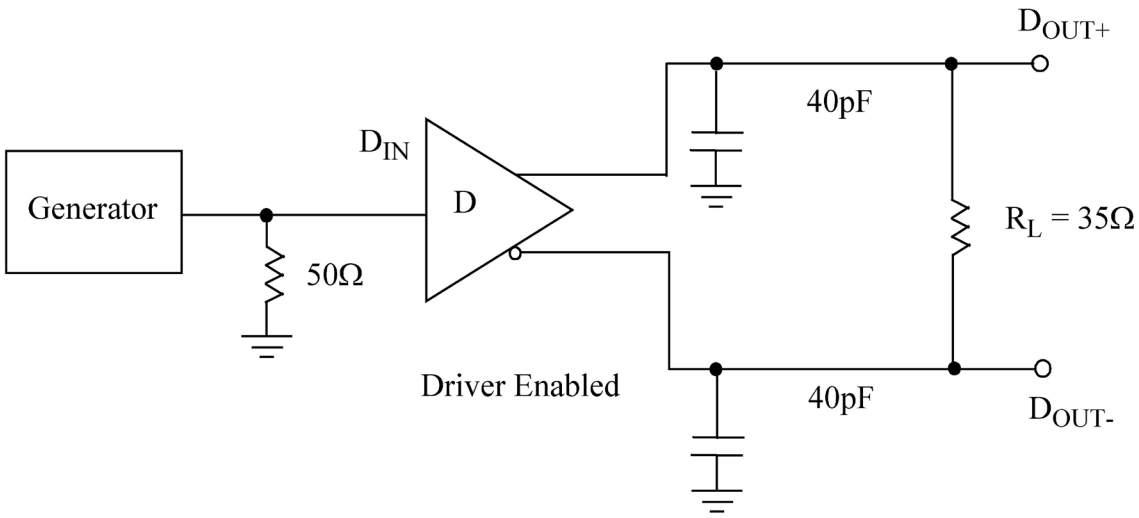

Figure 5. Driver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit

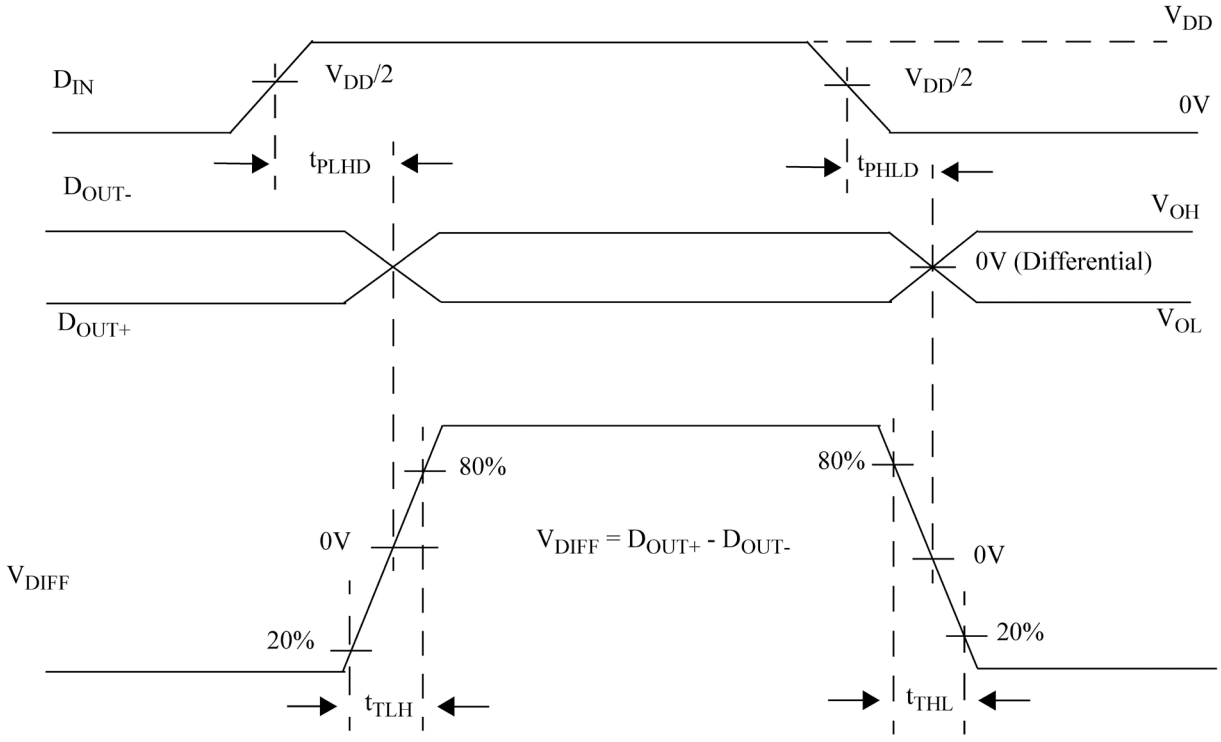

Figure 6. Driver Propagation Delay and Transition Time Waveforms or Equivalent Circuit

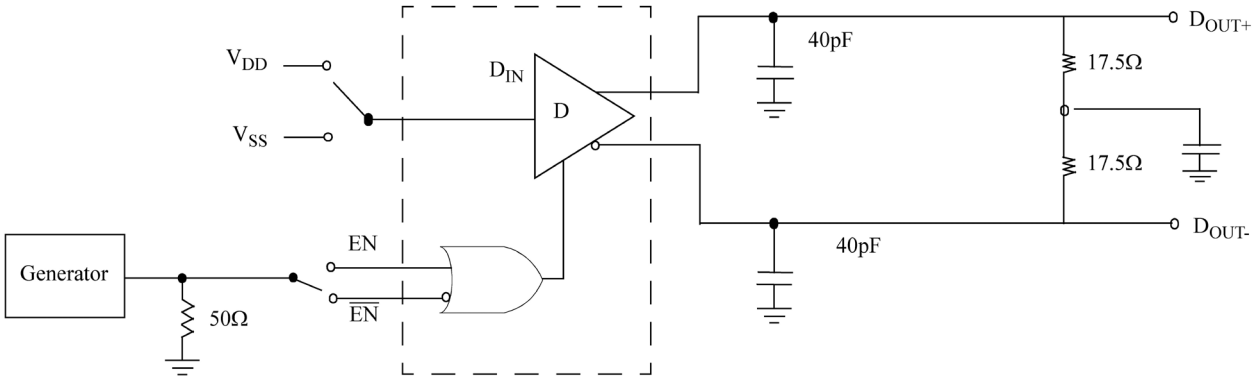

Figure 7. Driver Three-State Delay Test Circuit or Equivalent Circuit or Equivalent Circuit

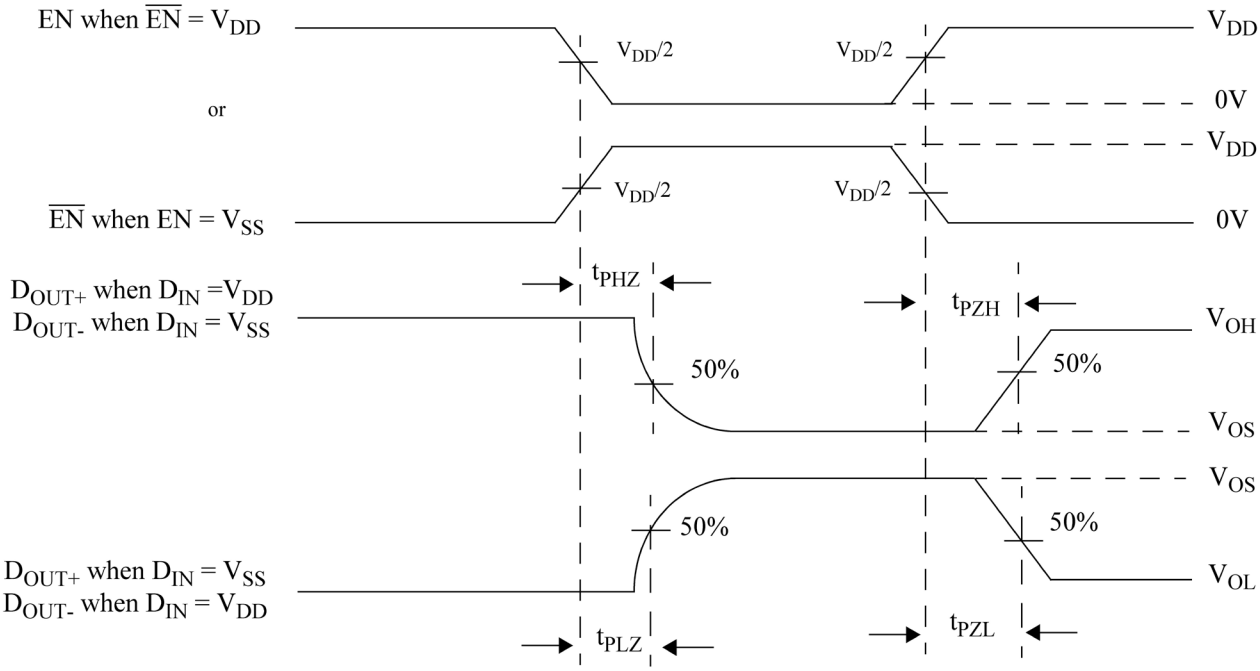

Figure 8. Driver Three-State Delay Waveform or Equivalent Circuit

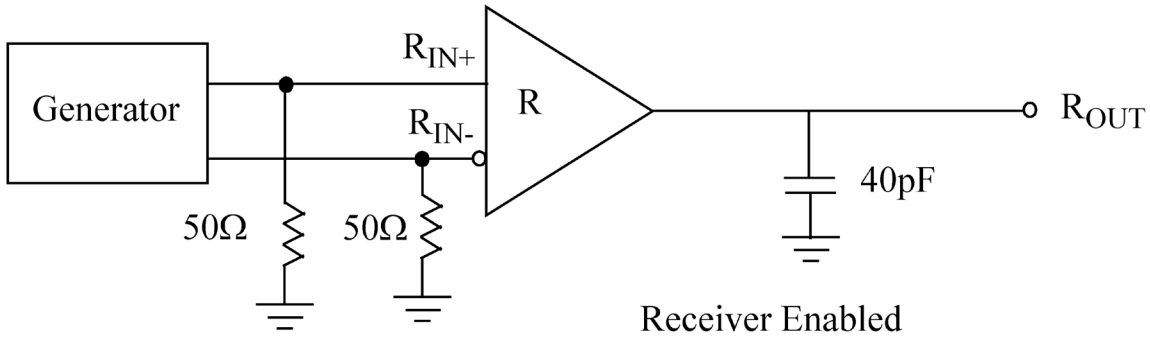

Figure 9. Receiver Propagation Delay and Transition Time Test Circuit or Equivalent Circuit

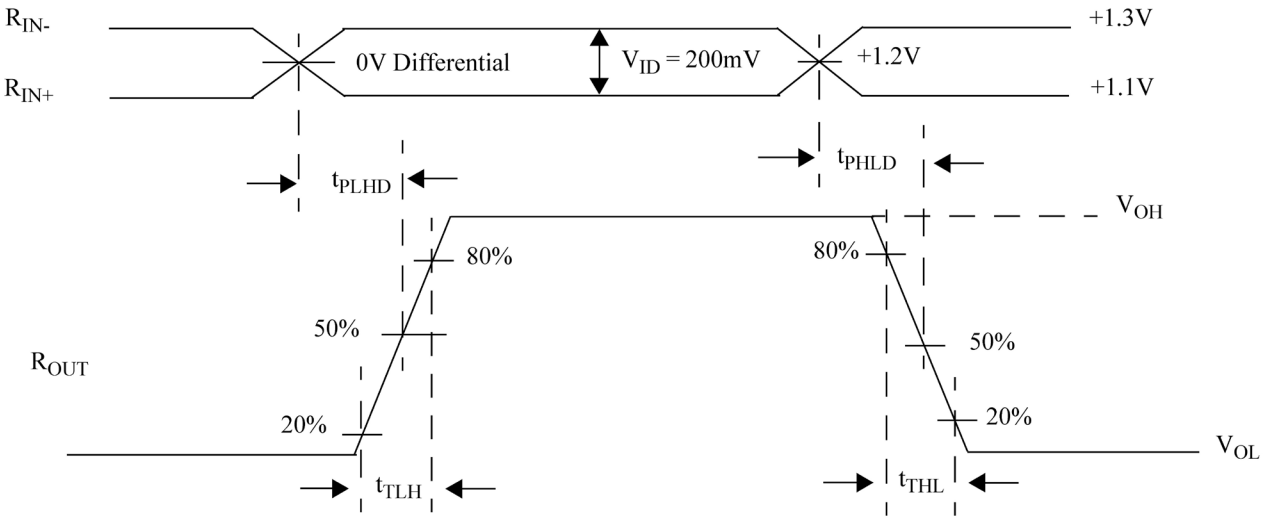

Figure 10. Receiver Propagation Delay and Transition Time Waveforms or Equivalent Circuits

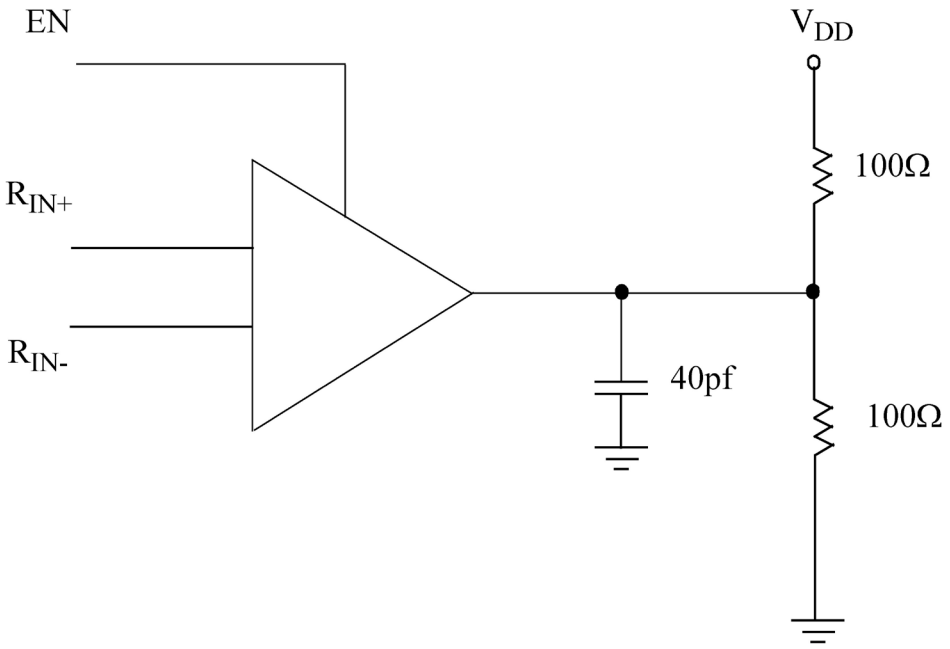

Figure 11. Receiver Three-State Delay Test Circuit or Equivalent Circuit

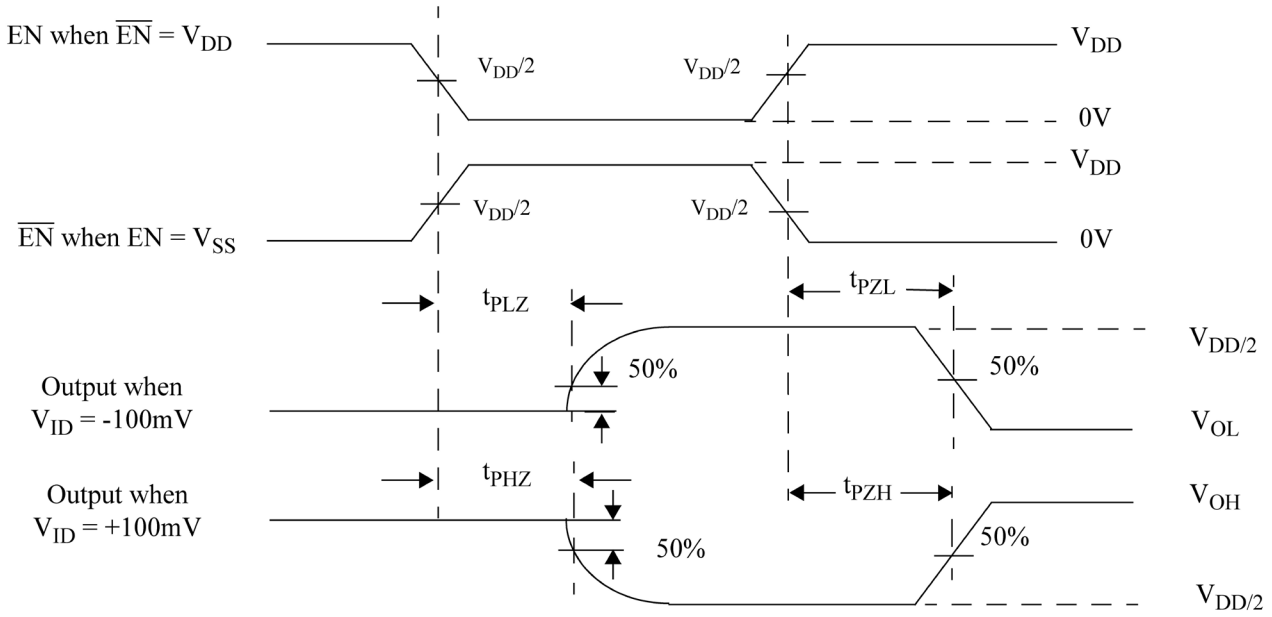

Figure 12. Receiver Three-State Delay Waveform or Equivalent Circuit

Dual Driver and Receiver

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Packaging

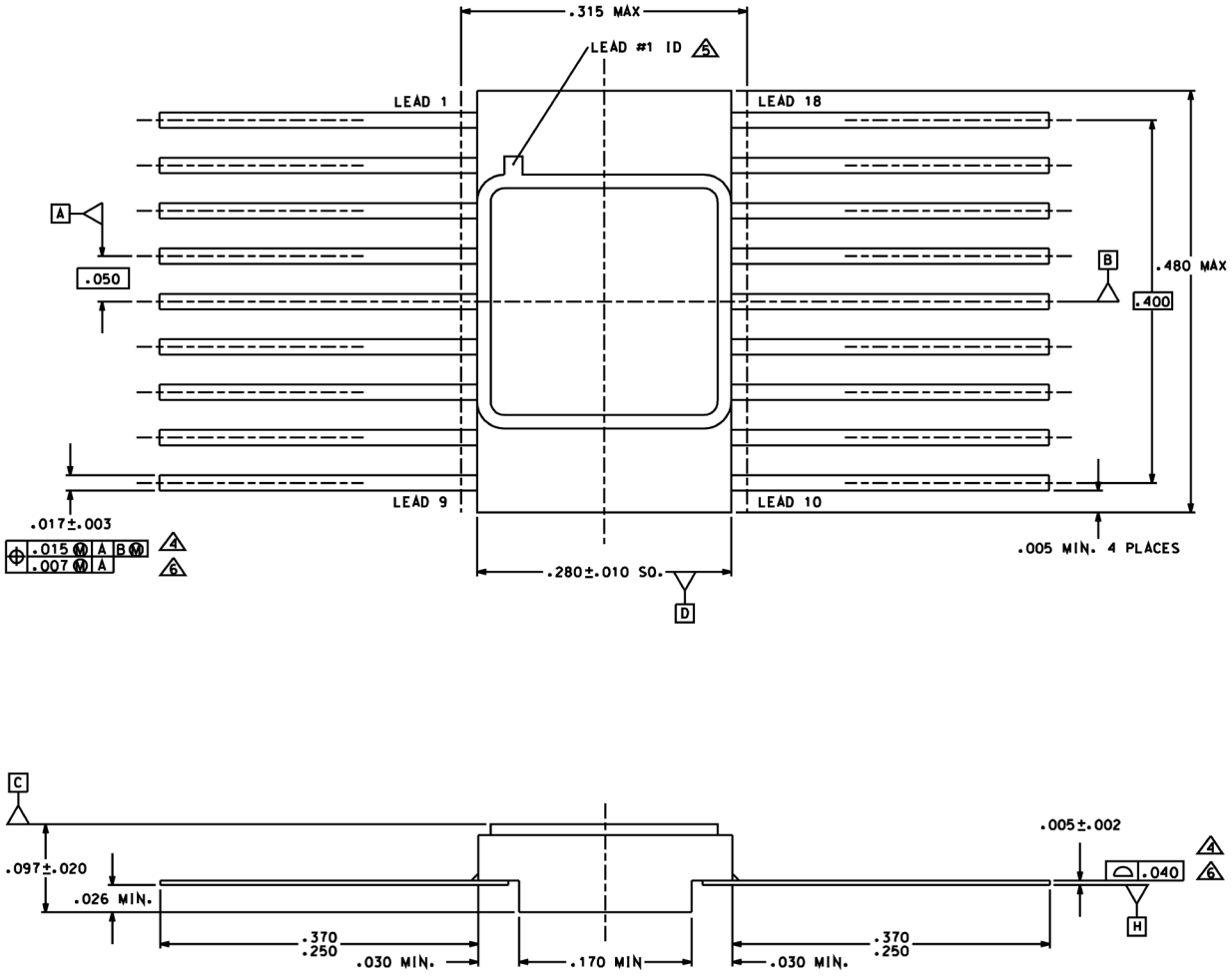

Figure 13. 18-pin Ceramic Flatpack

Notes:

1) All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2) The lid is electrically connected to VSS.
3) Lead finishes are in accordance to MIL-PRF-38535.
4) Lead position and coplanarity are not measured.
5) ID mark symbol is vendor option and may be different than shown.
6) With solder, increase maximum by 0.003.
7) Package weight 0.8 grams.

Dual Driver and Receiver

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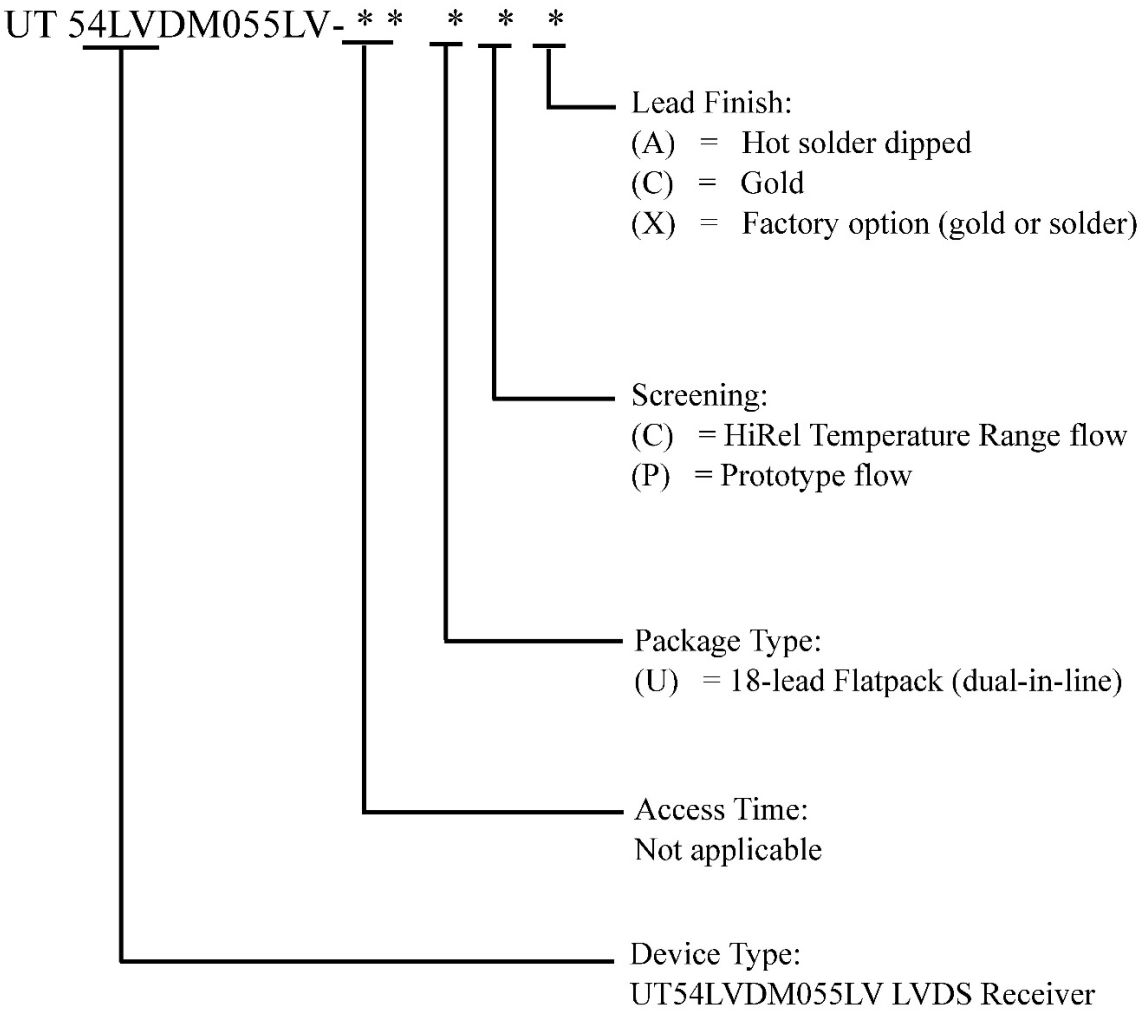
Ordering Information

UT54LVDM055LV Dual Driver/Receiver:



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Prototype flow per CAES Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4) HiRel Temperature Range flow per CAES Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

Dual Driver and Receiver

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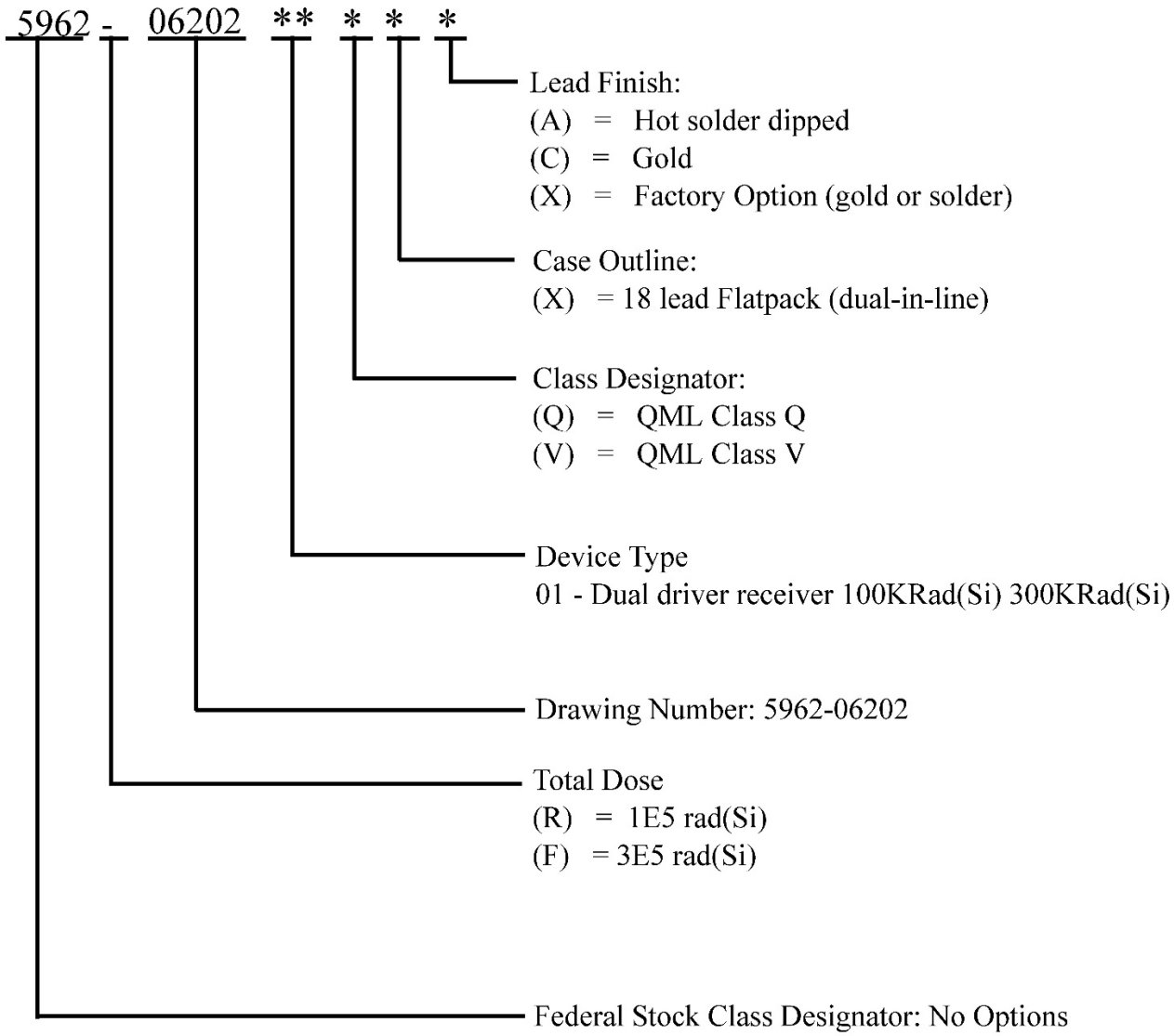
UT54LVDM055LV Dual Driver/Receiver: SMD



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

Dual Driver and Receiver

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Data Sheet Revision History

REV	Revision Date	Description of Change	Author
1.0.0	12-08	Last official release	MM
1.0.1	9-17-15	Page 1, added package weight. Added Applied new CAES Data Sheet template to the document.	MM
1.0.2	6-24-16	Corrected TID on page 5	BM
1.0.3	8-16-21	Added HBM ESD Rating: AMR Table, p.5	BM
1.0.4	9-22-21	SEL Limit sign, p.1, 5	BM

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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