AWD5101S4

800/1900 MHz Dual Band Driver MMIC

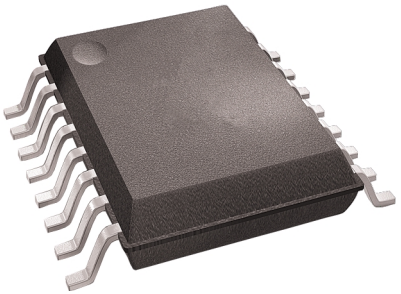
Advanced Product Information - Rev. 2

FEATURES

- High linearity
- 2 inputs / 2 outputs
- Low cost
- 16 Pin SSOP plastic package
- 50Ω input / output
- On chip bias circuit (only requires fixed voltages)
- Bias mode switching for optimum performance in linear or analog modes

APPLICATIONS

- Dual band triple mode CDMA/TDMA handsets
- CDMA/TDMA base stations



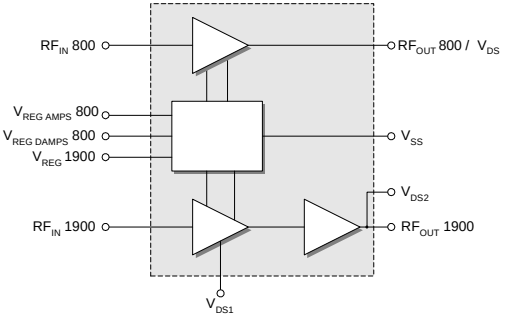
S4
16 Pin SSOP Plastic Package

Description

The AWD5101 is a monolithic dual band driver amplifier for 3V dual band, triple mode portable handset applications. This part is designed for optimum performance in both the 800MHz and 1900 MHz frequency bands. It can be used for linear applications including TDMA and CDMA in both bands as well as analog applications such as AMPS.

Pin	Signal	Max Rating
1	RF_{IN} 800	3 dBm
2	Vreg 800A	5V, 0 V_{DC}
3	Vreg 800D	5V, 0 V_{DC}
4	V_{SS}	(-) V_{DC}, 0 V_{DC}
5	Vreg 1900	5V, 0 V_{DC}
7	RF_{IN} (1900)	0 dBm
8	V_{DS1} (1900)	10 V_{DC}
9	V_{DS2} (1900)	10 V_{DC}
10	RF_{OUT} (1900)	-
16	RF_{OUT} 800/Vds (800)	10 V_{DC}

Block Diagram



Operating Temperature: -20° to 70° C
Storage Temperature: -55° to 100° C

Electrical Characteristics :AMPS 800 [1]

V_{DS} = V_{DS1} = V_{DS2} = +3.4V, $V_{REG800A}$ = 3.1V $V_{REG800D}$ = $V_{REG1900}$ = Open; V_{SS} = (-3.15V), Tc = 25°C, 50Ω System

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency	fo	824	-	849	MHz
Power Output	P_{OUT}	13	-	-	dBm
Gain	Gain	-	14	-	dB
Drain Current	Id	-	21	-	mA
Idle Drain Current (V_{REG} 800 open)	Id+Id1+Id2	-	25	-	μA
Intermodulation	IM3 IM5 IM7	-	35 50 60	-	dBc
Harmonic 2nd 3rd	-	-	 25 33	-	dBc
Stability: -80 dBc, all spurious outputs relative to desired signal	-	-	-80 dBc	-	VSWR load, all phase angles V_{DS}= +3.4V, Load VSWR ≤ 3:1 In band and Load VSWR ≤10:1 out of band and Zs = 50 Ω
Input VSWR	Γ_{IN}	-	1.8:1	-	-
Output VSWR	Γ_{OUT}	-	1.6:1	-	-
Positive regulated Current	$I_{REG\ 800A}$	-	1.7	-	mA
Negative Supply Current	-	-	1.5	-	mA
Rx Noise @ 869 - 894	Nrx	-	-	(-)154	dBm/Hz

[1] As measured in ANADIGICS test fixture.

Note: *Id* = *Id* (V_{DS})
Id1 = *Id1* (V_{DS1})
Id2 = *Id2* (V_{DS2})

Electrical Characteristics: DAMPS 800/CDMA 800 [1]

V_{DS} = V_{DS1} = V_{DS2} = +3.4V, $V_{REG800D}$ = 3.1V $V_{REF800A}$ = $V_{REG1900}$ = Open; V_{ss} =(-3.15V) Tc = 25°C, 50Ω System

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency	fo	824	-	849	MHz
Power Output	P_{OUT}	10.5	-	-	dBm
Gain	Gain	-	14.5	-	dB
Drain Current	Id	-	26	-	mA
Idle Drain Current (V_{REG} 800 D open)	Id+Id1+Id2	-	25	-	μA
Intermodulation	IM3 IM5 IM7	-	35 50 60	-	dBc
Harmonic 2nd 3rd	-	-	 35 55	-	dBc
Stability: -80 dBc, all spurious outputs relative to desired signal	-	-	-80 dBc	-	VSWR load, all phase angles V_{DS} =+3.4V, Load VSWR ≤3:1 In band and Load VSWR ≤10:1 out of band and Zs = 50Ω
Input VSWR	IN	-	1.4:1	-	-
Output VSWR	OUT	-	1.4:1	-	-
Positive regulated Current	I_{REF} 800D	-	2.5	-	mA
Negative Supply Current	-	-	2	-	mA
Rx Noise @ 869-894	Nrx	-	-	(-)153	dBm/Hz
Adj. Channel Power rejection @ ±885 kHz offset, Primary Channel Bandwidth = 1.23 MHz, Adjacent Channel Bandwidth = 30 kHz	ACPR	-	54.2	-	dBc @ 885 MHz Offset

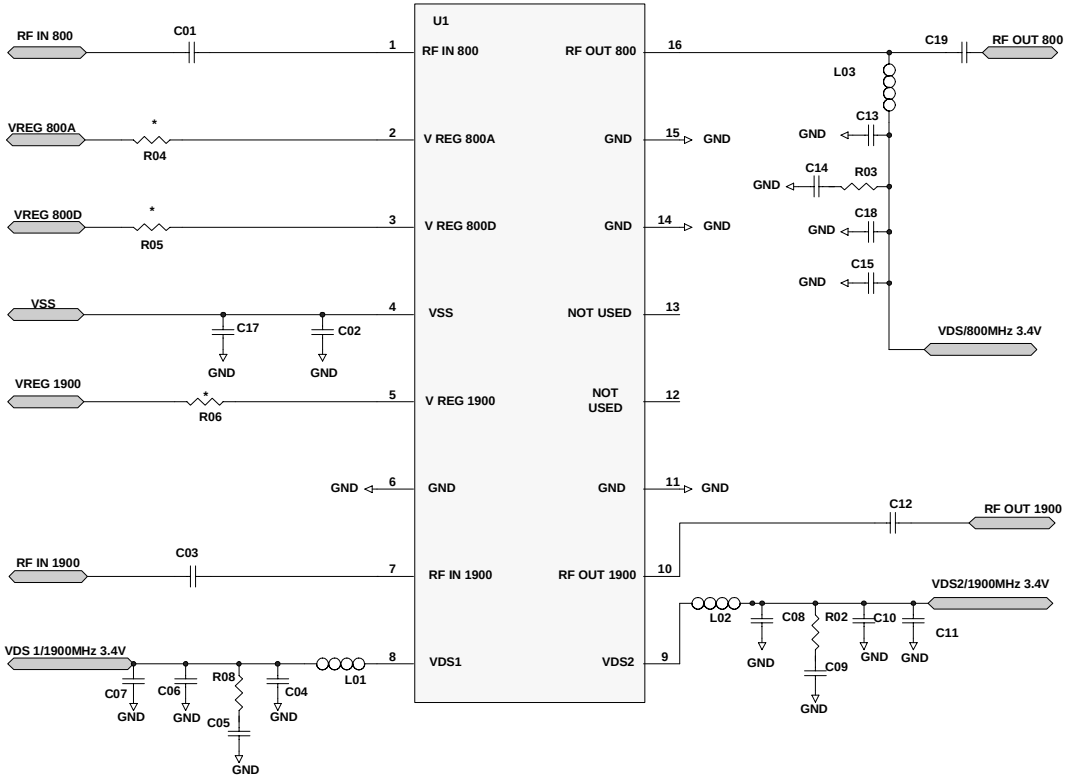
[1] As measured in ANADIGICS test fixture.

Electrical Characteristics :DAMPS 1900/CDMA 1900 (1)

V_{DS} = V_{DS1} = V_{DS2} = + 3.4V, $V_{REG1900}$ = 3.1V $V_{REG800A}$ = $V_{REG800D}$ = Open; V_{ss} = (-3.15V) Tc = 25°C, 50Ω System

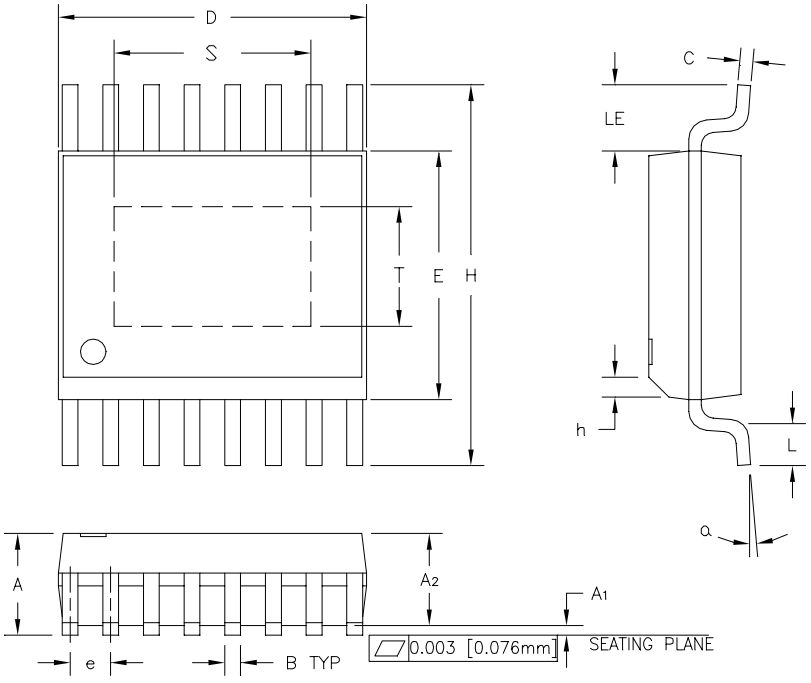
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency	fo	1850	-	1910	MHz
Power Output	P_{OUT}	11	-	-	dBm
Gain	Gain	-	21	-	dB
Drain Current	Id1 + Id2	-	45	-	mA
Idle Drain Current (V_{REG} 1900 open)	Id+Id1+Id2	-	25	-	μA
Intermodulation	IM3 IM5 IM7	-	35 50 60	-	dBc
Harmonic 2nd 3rd	-	-	 35 55	-	dBc
Stability: -80 dBc, all spurious outputs relative to desired signal	-	-	-80 dBc	-	VSWR load, all phase angles V_{DS1} =V_{DS2}=+3.4V, Load VSWI ≤ 3:1 In band and Load VSWR ≤ 10:1 out of band and Zs = 50Ω
Input VSWR	IN	-	1.5:1	-	-
Output VSWR	OUT	-	1.3:1	-	-
Positive regulated Current	I_{REF} 1900	-	1.5	-	mA
Negative Supply Current	-	-	1	-	mA
Rx Noise @ 1930 - 1990	Nrx	-	-	(-)148	dBm/Hz
Adj. Channel Power rejection @ ±1.25 MHz offset, Primary Channel Bandwidth = 1.23 MHz, Adjacent Channel Bandwidth = 30 kHz	ACPR	-	57	-	dBc @ 1.25 MHz Offset

Pin	Signal	Description
1	RF_{IN} 800	RF_{IN} 800 MHz for AMPS and DAMPS mode
2	Vreg 800A	Bias and drain voltage to the bias circuit in AMPS mode (3.1V)
3	Vreg 800D	Voltage to the bias circuit in DAMPS mode (3.1V)
4	V_{SS}	Negative voltage for the bias circuit (-) 3.15V
5	Vreg 1900	Voltage to the bias circuit in TDMA PCS mode (3.1V)
6	GND	RF and DC ground
7	RF_{IN} (1900)	RF_{IN} 1900 MHz
8	V_{DS1} (1900)	Drain of 1st stage (3.4V)
9	V_{DS2} (1900)	Drain of 2nd Stage (3.4V)
10	RF_{OUT} (1900)	RF power output 1900 MHz
11-15	GND	RF and DC Ground
16	RF_{OUT} 800/Vds (800)	RF power output 800 MHz



Part Type	Designator	Value	Part Type	Designator	Value	Part Type	Designator	Value
CAP	C01	68 pF	CAP	C10	47 nF	INDUCTOR	L01	12 nH
CAP	C02	68 pF	CAP	C11	2.2 uF	INDUCTOR	L02	18 nH
CAP	C03	33 pF	CAP	C12	33 pF	INDUCTOR	L03	33 nH
CAP	C04	33 pF	CAP	C13	68 pF	Resistor	R02	10 ohm
CAP	C05	47 nF	CAP	C14	47 nF	Resistor	R03	20 ohm
CAP	C06	47 nF	CAP	C15	2.2 uF	Resistor	R04	560 ohm
CAP	C07	2.2 uF	CAP	C17	1 uF	Resistor	R05	330 ohm
CAP	C08	33 pF	CAP	C18	47 nF	Resistor	R06	750 ohm
CAP	C09	47 nF	CAP	C19	68 pF	Resistor	R08	10 ohm

Package Outline Diagram



SYMBOL	MILLIMETERS		INCHES		NOTE
	MIN.	MAX.	MIN.	MAX.	
A	1.45	1.55	0.057	0.061	
A_1	0.00	0.10	0.000	0.004	6
A_2	–	1.45	–	0.057	
B	0.20	0.30	0.008	0.012	
C	0.19	0.25	0.007	0.009	
D	4.80	5.00	0.189	0.196	2
E	3.80	4.00	0.150	0.157	3
e	0.64 BSC		0.025 BSC		4
H	5.80	6.20	0.228	0.244	
h	0.36	0.41	0.014	0.016	
L	0.40	1.27	0.016	0.050	
LE	0.90	1.20	0.035	0.047	
α	0°	8°	0°	8°	
S	–	2.8	–	0.110	5
T	–	2.5	–	0.100	5

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 [0.15mm] PER SIDE.
3. DIMENSION "E" DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 [0.25mm] PER SIDE.
4. MAXIMUM LEAD TWIST/SKEW TO BE 0.002 [0.05mm]
5. DIMENSION "S" AND "T" INDICATE EXPOSED DOWNSET AREA.
6. A_1 STAND OFF IS MEASURED FROM BOTTOM OF EXPOSED PAD TO THE SEATING PLANE.
7. FOLLOWED FORM JEDEC MO–137.

PRELIMINARY
DRAWING
REF. ONLY

NOTES

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