Preliminary

# Am79h1068/Am79h1069-125

## FOXIchip™ Set
## (Fiber Optic Xmitter – Receiver Interface with TAXI™)

Advanced Micro Devices

## DISTINCTIVE CHARACTERISTICS

- **Complete 'Byte-to-Light™' solution for fiber optic links**
- **TTL bus I/O:**
  - 12.5 Mbytes/sec transfer rate
  - Selectable 8, 9 or 10 Data lines with respectively 4, 3 or 2 Command lines
  - Asynchronous input using STRB/ACK
- **Synchronous serial optical link:**
  - High performance 1300 nm optics
  - 125 Mbaud, 2 Km
  - PLL synchronizer on board
  - NRZI, 4B/5B or 5B/6B encoding
  - ST® optical connectors
- **Pin compatible with 28-Pin DIP Am7968/Am7969-125DC TAXIchip™ Set**
- **Single +5 Volt supply**

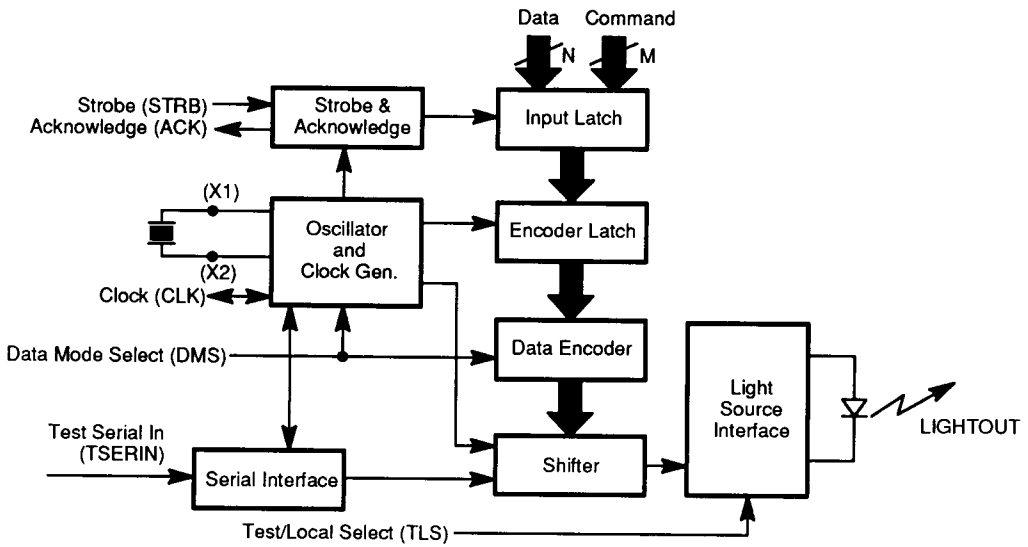
## GENERAL DESCRIPTION

The Am79h1068 Transmitter and the Am79h1069 Receiver are designed for use in optical fiber links for high speed, point-to-point data communications. Both are TTL compatible on the "electrical side," and can be connected to a bus. A simple STRB/ACK handshake is used to write data into the Transmitter. The parallel data supplied to the Transmitter is encoded, serialized and converted into light signals, that can be sent over optical fiber. The light source is a high-performance 1300 nm ELED. The light detector is a high-performance planar PIN photodiode. Both Transmitter and Receiver contain ST optical connectors. At the Receiver end the data is reconstructed into parallel words, which can be used by the local bus. The Receiver supplies a Data or Command strobe (DSTRB or CSTRB) as timing for each output word. The whole operation is transparent to the user.



Publication #14380 Rev. A Amendment /0
Issue Date: May 1990

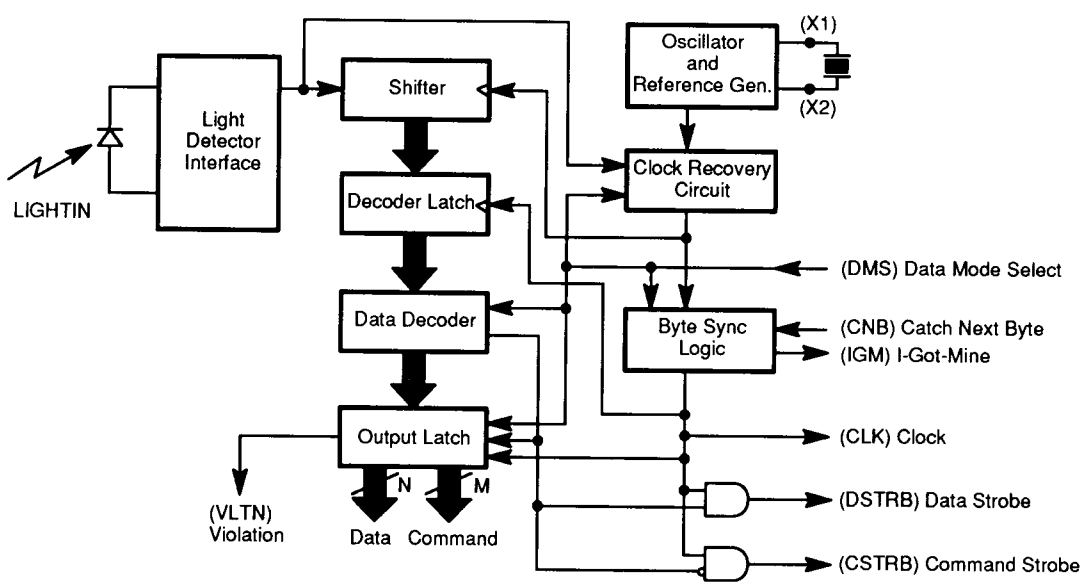
## BLOCK DIAGRAM
## Am79h1068 FOXI Transmitter




**Note:**
N can be 8, 9, or 10 bits, and N + M = 12 bits

14380-001A

## BLOCK DIAGRAM
## Am79h1069 FOXI Receiver



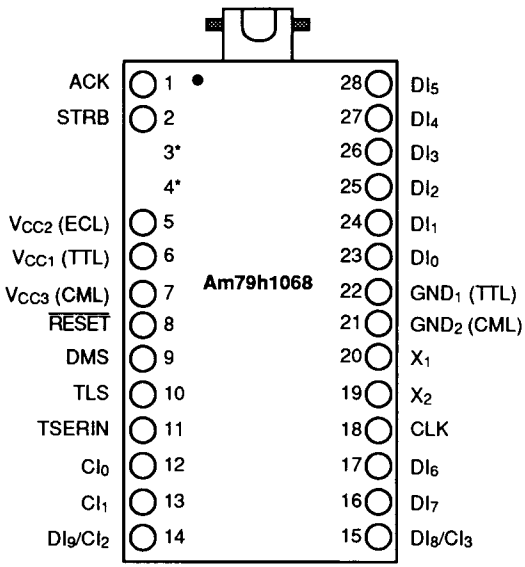

**Note:**
N can be 8, 9, or 10 bits, and N + M = 12 bits

14380-002A

## CONNECTION DIAGRAMS

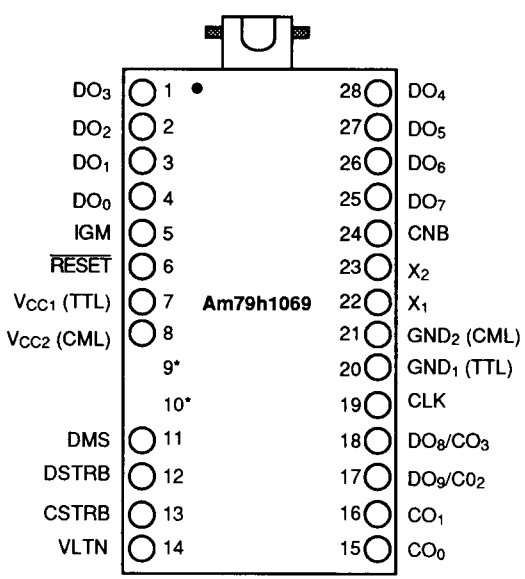
### Top View

### PDIP




14380-003A

### PDIP

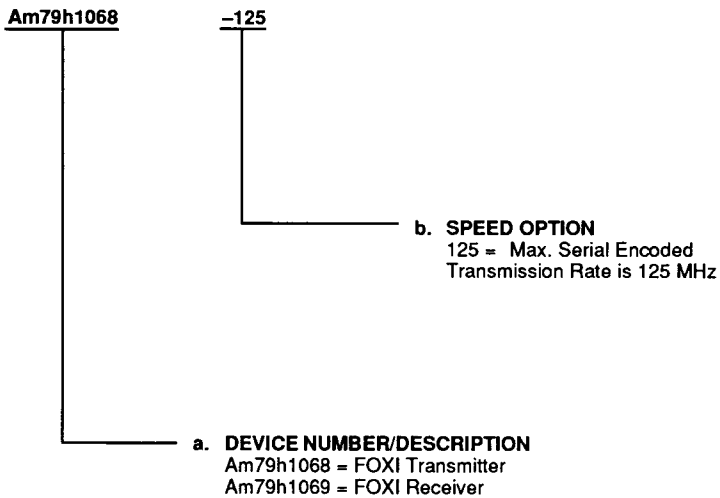



14380-004A

* No Pin

## ORDERING INFORMATION
## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
**a. Device Number**
**b. Speed Option (if applicable)**




| Valid Combinations | |
|---|---|
| AM79h1068-125 | |
| AM79h1069-125 | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## SIGNAL DESCRIPTION
## Am79h1068 FOXI Transmitter

### $DI_0 - DI_7$
**Parallel Data In (TTL Inputs)**

These eight inputs accept parallel Data from the host system, to be latched, encoded and transmitted.

### $DI_8/CI_3$
**Parallel Data (8) In or Command (3) In (TTL Input)**

*$DI_8/CI_3$* input is either Data or Command, depending upon the state of *DMS*.

### $DI_9/CI_2$
**Parallel Data (9) In or Command (2) In (TTL Input)**

*$DI_9/CI_2$* input is either Data or Command, depending upon the state of *DMS*.

### $CI_0 - CI_1$
**Parallel Command In (TTL Inputs)**

These two inputs accept parallel Command information from the host system. If one or more Command bits are logic "1", the Command bit pattern is latched, encoded, and transmitted in place of any pattern on the Data inputs.

### STRB
**Input Strobe Signal (TTL Input)**

A rising edge on the *STRB* input causes the Data *($DI_0 - DI_9$)* or the Command *($CI_0 - CI_3$)* inputs to be latched into the Am79h1068 Transmitter. The *STRB* signal is normally taken Low after *ACK* has risen.

### ACK
**Input-Strobe Acknowledge (TTL Output)**

*ACK* High signifies that the Am79h1068 is ready to accept new Data or Command. The timing of *ACK's* response to *STRB* depends on the condition of the input Latch (in given CLK cycle).

If the Input Latch is empty, data is immediately stored and *ACK* closely follows *STRB*. If the Input Latch contains previously stored data when *STRB* is asserted, *ACK* is delayed until the next falling edge of *CLK*. Note that for *ACK* to rise, *STRB* must maintain HIGH for both of the above conditions.

### $X_1$, $X_2$
**Crystal Oscillator Inputs (Inputs)**

These two crystal pins connect to an internal parallel mode oscillator which operates at the fundamental frequency of the crystal. During normal operation, the byte rate is set by the crystal frequency.

Alternatively, $X_1$ can be driven by an external TTL frequency source. In multiple FOXI systems this external source could be another Am79h1068's *CLK* output.

### DMS
**Data Mode Select (Input)**

Data Mode Select input determines the Data pattern width. When it is wired to GND, the Am79h1068 Transmitter will assume Data to be eight bits wide, with four bits of Command. When it is wired to $V_{CC}$, the Am79h1068 Transmitter will assume Data to be nine bits wide, with three bits of Command. If *DMS* is left floating (or terminated to 1/2 $V_{CC}$), the Am79h1068 will assume Data to be ten bits wide, with two bits of Command.

### TLS
**Test/Local Select (Input)**

*TLS* input determines the mode of operation. When *TLS* is wired to GND, the Am79h1068 Transmitter assumes a Local mode. It will output NRZI data, and will enable its *CLK* output driver. *TLS* pin should always be grounded during normal operation.

When *TLS* is wired to $V_{CC}$ (Test Mode 1), Transmitter operation is similar to Local Mode Operation except that serial output data is NRZ, *CLK* becomes an input, and ACK timing is modified. This Mode is useful for Automatic Test Equipment (ATE) testing at full speed and removes the need for match loop testing often required for NRZI data streams.

When this input is left unconnected, it floats to an intermediate level which puts the Am79h1068 Transmitter into its Test Mode 2. In Test Mode 2, the internal clock multiplier is switched out, and the internal logic is clocked directly from the *CLK* pin. Test Mode 2 is included to ease ATE testing by making the internal logic of the FOXI synchronous to the external clock instead of the internal PLL.

### CLK
**Clock (TTL I/O)**

*CLK* is an I/O pin for the byte rate clock reference that drives internal logic. When *TLS* is connected to GND (Local mode), *CLK* is enabled as a free-running (byte-rate) clock output which runs at the Crystal Oscillator frequency; this output can be used to drive the $X_1$ input of a FOXI Receiver or other system logic. In Test mode *CLK* becomes an input. In Test Mode 1 *CLK* is a Byte rate input and in Test Mode 2 it is a Bit rate input.

### $\overline{\text{RESET}}$
**PLL RESET (Input)**

This pin is normally left open. It can be momentarily grounded to force the internal PLL to reactivate lock. This allows for correction in the unlikely occurrence of PLL lockup on application of power.

$\overline{\text{RESET}}$ has an internal pull-up resistor which causes it to float high when left unconnected (50 K ohm nominal).

### TSERIN
**Test Serial Input (Pseudo ECL Input)**

This pin is left unconnected in Local Mode operation. TSERIN can be used to input serial data patterns into the Shifter in Test Mode operation.

### $V_{CC1}$, $V_{CC2}$, $V_{CC3}$
**Power Supply**

*$V_{CC1}$*, *$V_{CC2}$*, and *$V_{CC3}$* are +5.0 Volt nominal power supply pins. *$V_{CC1}$* powers TTL I/O, *$V_{CC2}$* powers ECL circuitry, the LED and optical drive circuits, and *$V_{CC3}$* powers internal Logic and Analog circuitry.

### $GND_1$, $GND_2$
**Ground Pins**

*$GND_1$* is a TTL I/O Ground and *$GND_2$* is an internal Logic and Analog Ground.

### LIGHTOUT
**Optical Serial Output (ST Connector)**

This signal can be coupled into a fiber using the ST connector. The signal is a series of Light-On and Light-Off levels, representing the 4B/5B NRZI encoded data. The light source is a high performance 1300 nm ELED.

## Am79h1069 FOXI RECEIVER

### $DO_0 - DO_7$
**Parallel Data Out (TTL Outputs)**

These eight outputs reflect the most recent Data received by the Am79h1069 Receiver.

### $DO_8/CO_3$
**Parallel Data (8) Out or Command (3) Out (TTL Output)**

*$DO_8/CO_3$* output will be either a Data or Command bit, depending upon the state of *DMS*.

### $DO_9/CO_2$
**Parallel Data (9) Out or Command (2) Out (TTL Output)**

*$DO_9/CO_2$* output will be either a Data or Command bit, depending upon the state of *DMS*.

### $CO_0 - CO_1$
**Parallel Command Out (TTL Output)**

These two outputs reflect the most recent Command data received by the Am79h1069 Receiver.

### DSTRB
**Data Strobe (TTL Output)**

The rising edge of this output signals the presence of new Data on the *$DO_0 - DO_9$* lines. Data is valid just before the rising edge of *DSTRB*.

### CSTRB
**Command Strobe (TTL Output)**

The rising edge of this output signals the presence of new Command data on the *$CO_0 - CO_3$* lines. Command bits are valid just before the rising edge of *CSTRB*.

### VLTN
**Violation (TTL Output)**

VLTN High indicates that an invalid code has been detected. It changes state at the same time *$DO_i$* or *$CO_i$* change and will be followed by either *DSTRB* or *CSTRB*. This pin goes LOW when the next valid byte is decoded.

### IGM
**I-Got-Mine (TTL Output)**

The function of this pin depends on the timing relationship between CNB & CLK. If the limitations shown in the AC table are not met, the function of this pin is not guaranteed.

### CLK (TTL Output)

This clock runs at the byte rate, and is synchronous with the serial input. It falls at the time the Decoder Latch is loaded from the Shifter, and rises at mid-byte. The *CLK* output of the FOXI Receiver is not suitable as a frequency source for another FOXI Transmitter or Receiver. It is intended to be used by the host system as a clock synchronous with the received data.

### CNB
**Catch Next Byte Input (TTL Input)**

In Local Mode, *CNB* must be connected to the FOXI Receiver's *CLK* output. Each received byte will be captured, decoded and latched to the outputs.

### $X_1$, $X_2$
**Crystal Oscillator Inputs (Inputs)**

These two crystal pins are connected to an internal parallel mode oscillator which operates at the fundamental frequency of the crystal. During normal operation, the crystal sets the expected data rate. The actual byte rate is set by the incoming serial stream.

Alternatively, *$X_1$* can be driven by an external frequency source. In multiple FOXI systems, this external source could be a FOXI Transmitter's *CLK* output or an external TTL frequency source.

### DMS
**Data Mode Select (Input)**

*DMS* selects the Data pattern width. When it is wired to GND, the Am79h1069 Receiver will assume Data to be eight bits wide, with four bits of Command. When it is wired to $V_{CC}$ the Am79h1069 Receiver will assume Data to be nine bits wide, with three bits of Command. If *DMS* is left floating (or terminated to 1/2 $V_{CC}$), the Am79h1069 Receiver will assume Data to be ten bits wide, with two bits of Command.

### $\overline{\text{RESET}}$
**PLL RESET (Input)**

This pin is normally left open. It can be momentarily grounded to force the internal PLL to reactivate lock. This allows for correction in the unlikely occurance of PLL Lockup on application of power.

$\overline{\text{RESET}}$ has an internal pull-up resistor (50 K nominal) which causes it to float high when left unconnected.

### $V_{CC1}$, $V_{CC2}$
**Power Supply**

*$V_{CC1}$* and *$V_{CC2}$* are +5.0 Volt nominal power supply pins. *$V_{CC1}$* powers TTL I/O, and *$V_{CC2}$* powers internal Logic, and Analog circuitry.

### $GND_1$, $GND_2$
**Ground**

*$GND_1$* is a TTL I/O Ground, *$GND_2$* is an internal Logic and Analog Ground.

### LIGHTIN
**Optical Serial Input (ST Connector)**

This signal is coupled using the ST connector to a high performance planar PIN photo diode.

## FUNCTIONAL DESCRIPTION

### General

The Am79h1068 Transmitter and the Am79h1069 Receiver make possible the implementation of a high speed serial link using optical fiber as the medium. They include the necessary data handling, timing and control functions together with the optical transducers. The design of the Transmitter/Receiver pair allows the use of the serial link as a generic bus-to-bus connection.

### Link Operation

The link is unidirectional: a parallel word is sent from one end and recovered at the other end. For each point-to-point direction a pair of FOXIs and a separate fiber are required.

The FOXI parallel interface is TTL with a maximum transfer rate of 12.5 Mbytes/sec. The word to be transmitted is latched in the Transmitter, encoded, serialized, converted into light and sent over the fiber at rates up to 125 Mbaud. At the Receiver end the serial string of symbols is converted into an electrical signal, deserialized, decoded and clocked out as parallel words.

### The Structure of the Parallel Word (Electrical Interface to the System)

"Data" means, in the FOXI sense, a group of 8, or 9, or 10 bits (depending on the "data mode selection"). Another group, called "Command", has 4, or 3, or 2 bits, correspondingly. The two groups are treated differently. A Command word is recognized by the Transmitter logic if at least one of the input Command lines ($CI_n$) is not zero at the rising edge of STRB. If so, the Data word at the Transmitter input is ignored and a Command word is transmitted. The Receiver will clock out a Command word using Command Strobe (CSTRB); Data output lines stay unchanged. If all input Command lines are zero at the rising edge of STRB, Data is transmitted. The Receiver then uses Data Strobe (DSTRB) to clock out the word; the Command outputs remain unchanged. In a given byte cycle time, it is possible to transmit either a Data word or a Command word, but not both.

Data represents the normal data channel message traffic between host systems. Commands can come from a communication control section of the host system. Commands are assumed to occur at a relatively infrequent rate but have priority over Data. Examples include communication specific commands such as REQUEST-TO-SEND, CLEAR-TO-SEND, or application specific commands such as MESSAGE-ADDRESS-FOLLOWS, MESSAGE-TYPE-FOLLOWS, INITIALIZE-YOUR-SYSTEM, ERROR, RETRANSMIT, HALT, etc.

### The Structure of the Serial Word (Transmitter to Receiver Interface)

When transmitted over fiber, Command or Data words look similar: they are encoded versions (symbols) of the original words. The encoding used in FOXI is 4B/5B and 5B/6B, resulting in symbol pairs of 10, or 11, or 12 bits for both Data and Command. They correspond to Data Mode selection of 8, or 9, or 10 bits. The transmitted bits are represented in NRZI form:

- "1" as a transition (Light ON-to-OFF or Light OFF-to-ON).
- "0" as no-transition (Light stays ON or Light stays OFF).

### Timing

The operation of the link is based on two clock frequencies: the "byte" (or parallel) rate and the baud (or serial) rate. Both the Transmitter and the Receiver have a crystal controlled oscillator that generates the byte rate, and a PLL multiplier that generates the baud rate. The CLK output of each one is a byte rate clock. The byte rate is the maximum average rate at which data can be input to the Transmitter.

Transmission over the fiber uses the serial clock generated in the Transmitter. A clock recovery circuit in the Receiver tracks the serial data, synchronizes to it, and separates clock and data. The recovered serial clock is then divided down to generate a synchronized byte rate on the Receiver side.

### Transmitter Input Asynchronous Operation

On average, the input byte rate (STRB rate) should be less than or equal to the CLK rate. When the STRB rate is less than the CLK rate, some of the CLK cycles will pass with no input STRB. In these cycles FOXI automatically pads with "Sync". STRB can be input at any phase in respect with CLK edges, without loss of information. Individual bytes can be strobed into the Transmitter at intervals less than the CLK cycle, if the STRB/ACK protocol (handshake) is observed.

### STRB/ACK Handshake

The input parallel word is latched in at the rising edge of STRB. The input latch consists of two stages. If both are empty at the strobe edge, the input word is transferred directly to the second stage and ACK goes HIGH. If the second stage is "busy" (contains a previously stored word), the input word is stored in the first stage of the latch; at the falling edge of CLK, the words are moved forward and ACK goes HIGH.

### The Encoding Scheme

To guarantee that the Am79h1069's PLL can stay locked onto an incoming bit stream, the data encoding scheme must provide an adequate number of transitions in each data pattern. This implies a limit on the maximum time allowed between transitions. The encoding scheme is based on the 4-bit/5-bit (4B/5B) code used by the ANSI X3T9.5 (FDDI) committee.

An ANSI X3T9.5 compatible system uses an 8-bit parallel data pattern. This pattern is divided into two 4-bit nibbles which are each encoded into a 5-bit symbol. Of the thirty-two possible symbols with these five bits, sixteen are chosen to represent the sixteen input Data patterns.

Some of the others are used as Command symbols. Those remaining represent invalid patterns that fail either the run-length or DC balance tests.

Transmitters in 8-bit mode use two 4B/5B encoders to encode eight Data bits into a 10-bit symbol pair. In 9-bit mode, Transmitters use one 5B/6B encoder and one 4B/5B encoder to encode nine Data bits into an 11-bit symbol pair. In 10-bit mode, two 5B/6B encoders are used to encode ten bits of Data into a 12-bit symbol pair (see Tables 1 and 2 for encoding patterns).

The Am79h1068 Transmitter further converts all symbols using NRZI (Non Return to Zero, Invert on Ones). This combination of 4B/5B encoding and NRZI ensures at least two transitions per symbol and permits a maximum of three consecutive non-transition bit times.

## The Sync Signal

The unique symbol pair called Sync is generated and sent by the Transmitter if a CLK cycle passes without any STRB input. Sync is recognized by a state machine in the Receiver. Its main purpose is byte alignment of the Receiver; it is needed if the Receiver loses phase or byte synchronization with the incoming signal. It is good practice to use Sync for "padding" byte cycles in which no information needs to be transmitted.

When Sync is detected in the Receiver, Data outputs remain in their previous state, all Command outputs go to "0", and CSTRB is asserted since Sync is a legal Command.

The encoded NRZI representation of Sync does not generate DC shifts of the "baseline". This helps to bring AC coupled links and circuits, and AGC-controlled amplifiers to the middle of their operating range (DC operating point and gain).

## Error Detection

Noise-induced bit errors can distort transmitted bit patterns. The Am79h1069 Receiver logic detects errors by recognizing invalid symbols that violate the code. They are indicated by the assertion of the violation (VLTN) output pin. This signal rises at the same time Data or Command outputs change, and remains HIGH until a valid symbol is detected by the Data Decoder. The error detection method used in the Receiver cannot identify bit errors which transform one valid Command or Data into another. Fault-sensitive systems should use additional error checking mechanisms to guarantee message integrity. (Refer to application notes #14229A TAXI Error Management and #12572A Implementing Parallel Cyclic Redundancy Check (CRC) for Reliable High-Speed Point-to-Point Communication Using TAXI)

## Operational Modes

## Local Mode

This is the normal mode of operation. A Transmitter/Receiver pair is used to transfer bytes of data over a private serial link. The following connections are to be made to select Local Mode:

| | |
|---|---|
| – for Am79h1068 | Pin 10 (TLS) to ground |
| – for Am79h1069 | Pin 24 (CNB) to Pin 19 (CLK) |

Local mode provides a fast and efficient parallel throughput because data can be transferred on every clock cycle. It is not necessary for the host to match the byte rate set by the Transmitter's crystal oscillator; the Am79h1068 automatically sends a Sync pattern during each clock cycle in which no new Data or Command messages are being transmitted.

## Test Mode

Test Mode 2 in the Transmitter allows testing of the logic in the Latches, Encoder, and Shifter without having to use the PLL clock multiplier. If TLS is open or terminated to approximately $V_{CC/2}$, the internal VCO is switched out, and CLK becomes a bit-rate-clock input. This means that the serial output rate will be at the CLK rate and not at 10X, 11X, or 12X, as is the case in normal operation.

The FOXI Receiver will acquire and track the test system data stream and should cause no significant test problems if the tester maintains a continuous frequency of data. Therefore no equivalent of Test Mode 1 or 2 is provided on the FOXI Receiver.

## Oscillator

The Am79h1068 and Am79h1069 contain an inverting amplifier intended to form the basis of a parallel mode crystal oscillator. In designing this oscillator, it is necessary to consider several factors related to the application.

The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the TAXIchips is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystal are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO).

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained, crystal oscillators operate at their fundamental frequency.

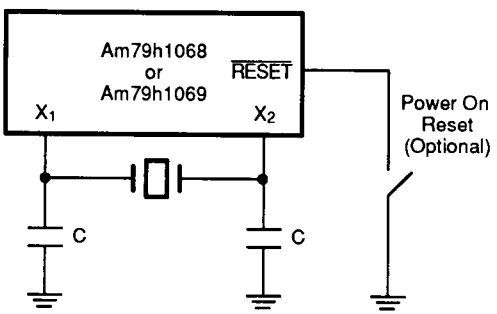
## Crystal

A typical crystal for use with the FOXI is specified as follows:

| | |
|---|---|
| Fundamental Frequency | 4 to 12.5 MHz ± 0.1% |
| Resonance Mode | Parallel |
| Load Capacitor (Correlation) | 75 pF |
| Operating Temperature Range | 0 to 70°C |
| Temperature Stability | ±100 ppm |
| Drive Level (Correlation) | 2 mW |
| Effective Series Resistance | 25 Ω (max) |
| Holder: Type | Low profile |
| Aging for 10 years | ±10 ppm |

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.

A crystal is connected between $X_1$ and $X_2$, as shown in Figure 1.




C* = 150 pF for a 12.5 MHz Crystal, 220 pF for a 4 MHz Crystal

* Values shown are typical. C is determined by Crystal specifications and trace capacitances.

14380-005A

**Figure 1. Crystal Connection**

Table 1. FOXI Encoder Patterns

| 4B/5B ENCODER SCHEME | | | 5B/6B ENCODER SCHEME | | |
|---|---|---|---|---|---|
| HEX Data | 4-BIT Binary Data | 5-BIT Encoded Symbol | HEX Data | 5-Bit Binary Data* | 6-Bit Encoded Symbol |
| 0 | 0000 | 11110 | 00 | 00000 | 110110 |
| 1 | 0001 | 01001 | 01 | 00001 | 010001 |
| 2 | 0010 | 10100 | 02 | 00010 | 100100 |
| 3 | 0011 | 10101 | 03 | 00011 | 100101 |
| 4 | 0100 | 01010 | 04 | 00100 | 010010 |
| 5 | 0101 | 01011 | 05 | 00101 | 010011 |
| 6 | 0110 | 01110 | 06 | 00110 | 010110 |
| 7 | 0111 | 01111 | 07 | 00111 | 010111 |
| 8 | 1000 | 10010 | 08 | 01000 | 100010 |
| 9 | 1001 | 10011 | 09 | 01001 | 110001 |
| A | 1010 | 10110 | 0A | 01010 | 110111 |
| B | 1011 | 10111 | 0B | 01011 | 100111 |
| C | 1100 | 11010 | 0C | 01100 | 110010 |
| D | 1101 | 11011 | 0D | 01101 | 110011 |
| E | 1110 | 11100 | 0E | 01110 | 110100 |
| F | 1111 | 11101 | 0F | 01111 | 110101 |
| | | | 10 | 10000 | 111110 |
| | | | 11 | 10001 | 011001 |
| | | | 12 | 10010 | 101001 |
| | | | 13 | 10011 | 101101 |
| | | | 14 | 10100 | 011010 |
| | | | 15 | 10101 | 011011 |
| | | | 16 | 10110 | 011110 |
| | | | 17 | 10111 | 011111 |
| | | | 18 | 11000 | 101010 |
| | | | 19 | 11001 | 101011 |
| | | | 1A | 11010 | 101110 |
| | | | 1B | 11011 | 101111 |
| | | | 1C | 11100 | 111010 |
| | | | 1D | 11101 | 111011 |
| | | | 1E | 11110 | 111100 |
| | | | 1F | 11111 | 111101 |

***Note:**

HEX data is parallel input data which is represented by the 4- or 5-bit binary data listed in the column to the immediate right of HEX data. Binary bits are listed from left to right in the following order.

8-Bit Mode: $D_7$, $D_6$, $D_5$, $D_4$, (4-Bit Binary), and $D_3$, $D_2$, $D_1$, $D_0$, (4-Bit Binary)

9-Bit Mode: $D_8$, $D_7$, $D_6$, $D_5$, $D_4$, (5-Bit Binary), and $D_3$, $D_2$, $D_1$, $D_0$, (4-Bit Binary)

10-Bit Mode: $D_8$, $D_7$, $D_6$, $D_5$, $D_4$, (5-Bit Binary), and $D_9$, $D_3$, $D_2$, $D_1$, $D_0$, (5-Bit Binary)

Serial bits are shifted out with the most significant bit of the most significant nibble coming out first.

**Table 2. FOXI Command Symbols**

| Am79h1068 Transmitter | | | | Am79h1069 Receiver | |
|---|---|---|---|---|---|
| Command Input | | | | Command Output | |
| **HEX** | **Binary** | **Encoded Symbol** | **Mnemonic** | **HEX** | **Binary** |
| **8-Bit FOXIs** | | | | | |
| 0 | 0000 | XXXXX XXXXX | Data (Note 2) | No Change (Note 2) | No Change |
| No STRB (Note 1) | No STRB (Note 1) | 11000 10001 | JK (8-bit Sync) | 0 | 0000 |
| 1 | 0001 | 11111 11111 | I I | 1 | 0001 |
| 2 | 0010 | 01101 01101 | TT | 2 | 0010 |
| 3 | 0011 | 01101 11001 | TS | 3 | 0011 |
| 4 | 0100 | 11111 00100 | I H | 4 | 0100 |
| 5 | 0101 | 01101 00111 | TR | 5 | 0101 |
| 6 | 0110 | 11001 00111 | SR | 6 | 0110 |
| 7 | 0111 | 11001 11001 | SS | 7 | 0111 |
| 8 (Note 3) | 1000 | 00100 00100 | HH | 8 | 1000 |
| 9 | 1001 | 00100 11111 | HI | 9 | 1001 |
| A (Note 3) | 1010 | 00100 00000 | HQ | A | 1010 |
| B | 1011 | 00111 00111 | RR | B | 1011 |
| C | 1100 | 00111 11001 | RS | C | 1100 |
| D (Note 3) | 1101 | 00000 00100 | QH | D | 1101 |
| E (Note 3) | 1110 | 00000 11111 | Q I | E | 1110 |
| F (Note 3) | 1111 | 00000 00000 | QQ | F | 1111 |
| **9-Bit FOXIs** | | | | | |
| 0 | 000 | XXXXXX XXXXX | Data (Note 2) | No Change (Note 2) | No Change |
| No STRB (Note 1) | No STRB (Note 1) | 011000 10001 | LK (9-bit Sync) | 0 | 000 |
| 1 | 001 | 111111 11111 | I'I | 1 | 001 |
| 2 | 010 | 011101 01101 | T'T | 2 | 010 |
| 3 | 011 | 011101 11001 | T'S | 3 | 011 |
| 4 | 100 | 111111 00100 | I'H | 4 | 100 |
| 5 | 101 | 011101 00111 | T'R | 5 | 101 |
| 6 | 110 | 111001 00111 | S'R | 6 | 110 |
| 7 | 111 | 111001 11001 | S'S | 7 | 111 |
| **10-Bit FOXIs** | | | | | |
| 0 | 00 | XXXXXX XXXXXX | Data (Note 2) | No Change (Note 2) | No Change |
| No STRB (Note 1) | No STRB (Note 1) | 011000 100011 | LM (10-bit Sync) | 0 | 00 |
| 1 | 01 | 111111 111111 | I' I' | 1 | 01 |
| 2 | 10 | 011101 011101 | T'T' | 2 | 10 |
| 3 | 11 | 011101 111001 | T'S' | 3 | 11 |

**Notes:**

1. Command pattern Sync cannot be explicitly sent by Am79h1068 Transmitter with any combination of inputs and STRB, but is used to pad between user data.
2. A strobe with all Zeros on the Command input lines will cause Data to be sent. See Table 1.
3. While these Commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

## Am79h1068 Transmitter Functional Block Description (Refer to block diagram)

### Crystal Oscillator/Clock Generator

The serial link speed is derived from a master frequency source (byte rate). This source can either be the built-in Crystal Oscillator, or a clock signal applied through the $X_1$ pin. The Byte rate signal is buffered and sent to the *CLK* output when Am79h1068 Transmitter is in Local mode.

The byte rate is also multiplied by ten (8-bit mode), eleven (9-bit mode), or twelve (10-bit mode), using the internal PLL, to create the Bit rate.

The working serial frequency can be varied between 40 and 125 MHz. The crystal frequency required to achieve the maximum 125 Mbaud on the serial link, and the resultant usable data transfer rate will be:

| Mode | Crystal Frequency | Am79h1068 Input and Am79h1069 Maximum Parallel Throughput | Internal Divide Ratio |
|---|---|---|---|
| 8-Bit | 12.5 MHz | 80 ns/pattern (100 Mbit/sec) | 125/10 |
| 9-Bit | 11.36 MHz | 88 ns/pattern (102 Mbit/sec) | 125/11 |
| 10-Bit | 10.42 MHz | 96 ns/pattern (104 Mbit/sec) | 125/12 |

### Input Latch

The Am79h1068's Input Latch accommodates asynchronous strobing of Data and Command by being divided into two stages.

If *STRB* is asserted when both stages are empty, Data or Command bits are transferred directly to the second stage of the Input Latch and *ACK* rises shortly after *STRB*. This pattern is now ready to move to the Encoder Latch at the next falling edge of *CLK*.

Input data is held in the first stage of the Input Latch only when the second stage is "busy" (contains previously stored data). The Transmitter will be busy when *STRB* is asserted a second time in a given *CLK* cycle. Contents of the first stage are not protected from subsequent *STRBs* within the same *CLK* cycle. At the falling edge of *CLK*, previously stored data is transferred from the second stage to the Encoder Latch and the new data is clocked into the second stage of the Input Latch. In Local mode *ACK* will rise at this time.

### Encoder Latch

The input to the Encoder Latch is clocked by an internal signal which is synchronous with the shifted byte being sent on the serial link. After a new input byte is strobed into the Input Latch, it is transferred to the Encoder Latch during the next CLK cycle.

### Data Encoder

Encodes twelve data inputs (8, 9, 10 Data inputs and 4, 3, 2 Command inputs) into 10, 11, or 12 bits. The Command inputs select the transmitted symbol pair. If all Command inputs are LOW, the symbol pair for the Data inputs will be sent. If Command inputs have any other pattern, then the symbol pair representing that Command will be transmitted.

### Shifter

The Shifter is parallel-loaded from the Encoder, at the first available byte boundary, and shifted until the next byte boundary. The Shifter is being serially loaded at all times. As data is being shifted out of the Transmitter, the Shifter fills from the LSB. If parallel data is available at the end of the byte, it is parallel-loaded into the Shifter and will be shifted out during the next clock cycle. Otherwise, the serially loaded data fills the next byte. The serial data which loads into the Shifter is generated by an internal state machine which generates a repeating Sync pattern.

### Light Source Interface

This is a light source driver. It translates logic levels at the Shifter output into drive currents for the LED, which is a high-performance 1300 nm MOVPE ELED.

## Am79h1069 Receiver Functional Block Description (Refer to block diagram)

### Light Detector Interface

A light detector (PIN photodiode) converts the input light signals from the fiber into electrical signals. The Detector Interface amplifies and filters the signal, and reshapes it into an appropriate logic signal. This signal is supplied to the Shifter as serial data and to the PLL as a timing reference.

### Crystal Oscillator/Reference Clock Generator

The clock recovery PLL in the Am79h1069 must be supplied with a reference frequency at the expected byte rate of the data to be recovered. The source of this frequency can either be the built-in Crystal Oscillator, or an external clock signal applied through the $X_1$ pin. The crystal frequency is then multiplied by ten (8-bit mode), eleven (9-bit mode) or twelve (10-bit mode) using an internal PLL and is used to set the expected serial data rate.

### Clock Recovery Circuit

Using a clock recovery PLL the input signal is separated into clock and data. The PLL is "biased" to the expected data frequency by the Reference Clock Generator, to facilitate locking. After achieving lock, it tracks the incoming data.

### Shifter

The Shifter is serially loaded from the Light Detector Interface, using the recovered bit clock.

### Byte Sync Logic

The incoming data stream is continuous, without any signal which denotes byte boundaries. The Byte Sync Logic will continuously monitor the data stream, and upon discovering the reserved code used for Sync, will

initialize a synchronous bit counter which counts bits, and indicates byte boundaries.

The logic signal that times data transfers from the Shifter to the Decoder Latch is buffered and sent to the *CLK* output. It is intended to be used by the host system as a clock synchronous with the received data. This output is synchronous with the byte boundary and the Receiver's internal byte clock.

Byte Sync Logic is responsible for generating the internal strobe signals for Parallel Output Latches. Parallel outputs are made on a byte boundary, after *CNB* falls, or when Sync is detected.

## Decoder Latch

Data is loaded from the Shifter to this latch at each symbol/byte boundary. It holds the input to the Data Decoder.

## Data Decoder

The Data Decoder decodes ten, eleven, or twelve bit encoded words. In 8-bit mode, data is decoded into either an 8-bit Data pattern or a 4-bit Command pattern. In 9-bit mode, data is decoded into either a 9-bit Data pattern or a 3-bit Command pattern. In 10-bit mode, data is decoded into either a 10-bit Data pattern or a 2-bit Command pattern.

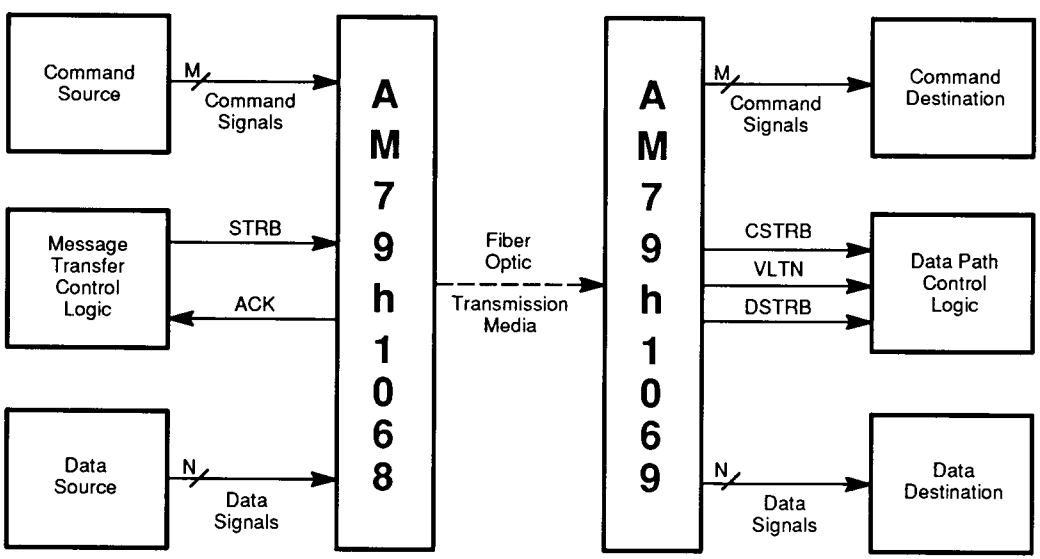
The Decoder separates Data symbols from Command symbols, and causes DSTRB or CSTRB output to be asserted.

## Parallel Output Latch

The output Latch will be clocked by the byte clock, and will reflect the most recent data on the link. Any Data pattern will be latched to the Data outputs and will not affect the status of the Command outputs. Likewise, any Command pattern will be latched to the Command outputs without affecting the state of the Data outputs.

Any data transfer, either Data or Command, will be synchronous with an appropriate output strobe. There will be *CSTRBs* when Sync bytes are detected, since Sync is a valid Command code.

Any pattern which does not decode to a valid Command or Data pattern is flagged as a violation. The output of the decoder during these violations is indeterminate and will result in either a *CSTRB* or *DSTRB* output when the indeterminate pattern is transferred to the respective output latch.




**Note:**

N can be 8, 9, or 10 bits of parallel data, and N + M = 12 bits.

**Figure 2. FOXI System Block Diagram**

14380-006A

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| StorageTemperature | –20 to +85°C |
| Case Temperature Under Bias | 0 to +70°C |
| Relative Humidity | 95% |
| Soldering Temperature | 240°C for 10 seconds |
| Supply Voltage to Ground Potential Continuous | 0 to +6.0 V |
| DC Voltage Applied to Outputs | –0.5 V to $V_{CC}$ max. |
| DC Input Voltage | –0.5 V to 5.5 V |
| DC Output Current | ±100 mA |
| DC Input Current | –30 to +5.0 mA |

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## OPERATING RANGES

**Commercial (C) Devices**

| | |
|---|---|
| Temperature ($T_C$) | 0 to +70°C |
| Supply Voltage ($V_{CC}$) | +4.5 to +5.5 V |

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified
## Am79h1068 FOXI Transmitter

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DI_0$–$DI_7$, $DI_8/CI_3$, $DI_9/CI_2$, $CI_0$–$CI_1$, STRB, ACK, CLK** | | | | | | |
| $V_{OH1}$ | Output HIGH Voltage ACK | $V_{CC}$ = Min., $I_{OH}$ = –1 mA<br>$V_{IN}$ = 0 or 3 V | | 2.4 | | V |
| $V_{OH2}$ | Output HIGH Voltage CLK | $V_{CC}$ = Min., $I_{OH}$ = –3 mA<br>$V_{IN}$ = 0 or 3 V | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage ACK,CLK | $V_{CC}$ = Min., $I_{OL}$ = 8 mA<br>$V_{IN}$ = 0 or 3 V | | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. (Note 9) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. (Note 9) | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min. $I_{IN}$ = –18 mA | | | –1.5 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4 V | | | –400 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | | 50 | µA |
| $I_I$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = 5.5 V | | | 50 | µA |
| $I_{SC}$ | Output Short Circuit Current ACK, CLK (Note 4) | | | –15 | –85 | mA |
| **Miscellaneous Signals: $X_1$, $V_{CC1}$, $V_{CC2}$, $V_{CC3}$** | | | | | | |
| $V_{IHX}$ | Input HIGH Voltage $X_1$ | | | 2.0 | | V |
| $V_{ILX}$ | Input LOW Voltage $X_1$ | | | | 0.8 | V |
| $I_{ILX}$ | Input LOW Current $X_1$ | $V_{IN}$ = 0.45 V | | | –900 | µA |
| $I_{IHX}$ | Input HIGH Current $X_1$ | $V_{IN}$ = 2.4 V | | | +600 | µA |
| $I_{CC}$ | Supply Current | DMS = 0 V | Pin $V_{CC1}$ (TTL) | | 30 | mA |
| | | $V_{CC1}$ = $V_{CC2}$ | Pin $V_{CC2}$ (ECL) | | 205 | mA |
| | | = $V_{CC3}$ = Max. | Pin $V_{CC3}$ (CML) | | 215 | mA |

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | Min. | Typ. (Note 2) | Max. | Unit |
|---|---|---|---|---|---|---|
| **Optical Output Characteristics: LIGHTOUT** | | | | | | |
| λc | Center Wavelength | | 1270 | 1300 | 1380 | nm |
| FWHM | Spectral Width | | | 90 | 120 | nm |
| $P_{OUT}$ | Output Power | Average output power from a 62.5 µm core, NA = 0.275 fiber, while transmitting "command 1" (square wave) | –20<br>10 | –15<br>or<br>32 | –14<br>40 | dBm<br>µW |

**Note:**

See notes following end of Switching Characteristics tables.

## Am79h1069 FOXI Receiver

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DO_0$–$DO_7$, $DO_8/CO_3$, $DO_9/CO_2$, $CO_0$–$CO_1$, DSTRB, CSTRB, IGM, CLK, CNB, VLTN** | | | | | | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OH}$ = −1 mA | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OL}$ = −1 mA | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. (Note 9) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. (Note 9) | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min. | $I_{IN}$ = −18 mA | | −1.5 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4 V | | | −400 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | | 50 | µA |
| $I_I$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = 5.5 V | | | 50 | µA |
| $I_{SC}$ | Output Short Circuit Current (Note 4) | | | −15 | −85 | mA |
| **Miscellaneous Signals: $X_1$, $V_{CC1}$, $V_{CC2}$** | | | | | | |
| $V_{IHX}$ | Input HIGH Threshold $X_1$ | | | 2.0 | | V |
| $V_{ILX}$ | Input LOW Threshold $X_1$ | | | | 0.8 | V |
| $I_{ILX}$ | Input LOW Current $X_1$ | $V_{IN}$ = 0.45 V | | | −900 | µA |
| $I_{IHX}$ | Input HIGH Current $X_1$ | $V_{IN}$ = 2.4 V | | | +600 | µA |
| $I_{CC}$ | Supply Current | $V_{CC1}$ = $V_{CC2}$ = Max. | Pin $V_{CC1}$ (TTL) | | 55 | mA |
| | Worst Case = Cold | DMS = 0 V | Pin $V_{CC2}$ (CML) | | 450 | mA |

| Parameter Symbol | Parameter Description | Test Conditions (Note 1) | Min. | Typ. (Note 2) | Max. | Unit |
|---|---|---|---|---|---|---|
| **Optical Input Characteristics: LIGHTIN** | | | | | | |
| λc | Center Wavelength | | 1240 | 1300 | 1390 | nm |
| S | Input Sensitivity | Average input power from 62.5 µm core, 0.275 NA fiber (Note 21) | | −28<br>or<br>1.0 | −26<br><br>2.5 | dBm<br><br>µW |
| Pmax | Maximum Input Power | Average input power from 62.5 µm core, 0.275 NA fiber | −14<br><br>40 | −12<br>or<br>63 | −9<br><br>130 | dBm<br><br>µW |

**Note:**

See notes following end of Switching Characteristics tables.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 20)

### Am79h1068 Transmitter (Notes 10, 13)

| No. | Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DI_0$–$DI_7$, $DI_8/CI_3$, $DI_9/CI_2$, $CI_0$–$CI_1$, STRB, ACK, CLK** | | | | | | |
| 1 | $t_P$ | CLK Period | | 8n | 25n | ns |
| 2 | $t_{PW}$ | CLK Pulse Width HIGH | | 30 | | ns |
| 3 | $t_{PW}$ | CLK Pulse Width LOW | | 30 | | ns |
| 4 | $t_{PW}$ | STRB Pulse Width HIGH (Note 7) | | 15 | | ns |
| 5 | $t_{PW}$ | STRB Pulse Width LOW | | 15 | | ns |
| 6 | $t_{BB}$ | Internal Byte Boundary to CLK↓ (Note 11) | | $\frac{-t_1}{5n} + 1$ | 20 | ns |
| 9 | $t_S$ | Data–STRB Setup Time | | 5 | | ns |
| 10 | $t_H$ | Data–STRB Hold Time | | 15 | | ns |
| 11 | $t_H$ | ACK↑ to STRB↓ Hold (Note 8) | TTL Output Load | 0 | | ns |
| 12 | $t_H$ | ACK↓ to STRB↑ Hold | TTL Output Load | 0 | | ns |
| 13 | $t_{PD}$ | STRB↑ to ACK↑ (Note 18) | TTL Output Load | | 40 | ns |
| 14 | $t_{PD}$ | STRB↓ to ACK↓ | TTL Output Load | | 23 | ns |
| 15A | $t_{PD}$ | CLK↓ to ACK↑ (Note 18) | TTL Output Load | | $\frac{3t_1}{n} + 33$ | ns |
| 16 | $t_R$ | ACK Rise Time (Note 3) | TTL Output Load | | 17 | ns |
| 17 | $t_F$ | ACK Fall Time (Note 3) | TTL Output Load | | 10 | ns |
| 18 | $t_R$ | CLK Rise Time (Note 3) | TTL Output Load | | 17 | ns |
| 19 | $t_F$ | CLK Fall Time (Note 3) | TTL Output Load | | 10 | ns |
| **Optical Signals** | | | | | | |
| 20 | $t_{PD}$ | CLK↓ to LIGHTOUT delay | | $\frac{t_1}{n} - 2$ | $\frac{2t_1}{n} + 8$ | ns |
| 21 | $t_r$ | LIGHTOUT Rise Time | | 1 | 4 | ns |
| 22 | $t_f$ | LIGHTOUT Fall Time | | 1 | 4 | ns |
| 23 | $t_{PW}$ | LIGHTOUT Pulse Width Distortion | Average output power from a 62.5 µm core, NA = 0.275 fiber, while transmitting "command 1" (square wave) | | $\frac{t_1}{n}$ ±5% | ns |
| **Miscellaneous Signals: $X_1$ (Note 15)** | | | | | | |
| 29 | $t_{PW}$ | $X_1$ Pulse Width HIGH (Note 12) | TTL Output Load on CLK | 35 | | ns |
| 30 | $t_{PW}$ | $X_1$Pulse Width LOW (Note 12) | TTL Output Load on CLK | 35 | | ns |
| 32 | $t_{PD}$ | $X_1$↑ to CLK↑ | TTL Load | | 25 | ns |
| 33 | $t_{PD}$ | $X_1$↓ to CLK↓ | TTL Load | | 32 | ns |

**Note:**

See notes following end of Switching Characteristics tables.

## Am79h1069 Receiver (Notes 13, 14)

| No. | Parameter Symbol | Parameter Description | Test Conditions | Min. | Max. | Units |
|---|---|---|---|---|---|---|
| **Bus Interface Signals:** | | **$DO_0$–$DO_7$,$DO_8$/$CO_3$,$DO_9$/$CO_2$,$CO_0$–$CO_1$,DSTRB,CSTRB, IGM,CLK,CNB,VLTN** | | | | |
| 35 | $t_P$ | $X_1$ Clock Period | | 8n | 25n | ns |
| 36 | $t_{PD}$ | Data Valid to STRB↑ Delay | TTL Output Load | $\frac{2t_{35}}{n}$ | | ns |
| 37 | $t_{PD}$ | CLK↓ to STRB↑ | TTL Output Load | | $\frac{2t_{35}}{n}+15$ | ns |
| 38 | $t_{PD}$ | CLK↑ to STRB↓ | TTL Output Load | $\frac{t_{35}}{n}-7$ | | ns |
| 39 | $t_{PD}$ | CLK↓ to Data Valid Delay | TTL Output Load | | $\frac{-t_{35}}{n}+23$ | ns |
| 40 | $t_{PW}$ | STRB Pulse Width | TTL Output Load | $\frac{5t_{35}}{2n}$ | $\frac{5t_{35}}{n}$ | ns |
| 41 | $t_{PW}$ | CLK Pulse Width HIGH | TTL Output Load | $\frac{5t_{35}}{n}-15$ | | ns |
| 42 | $t_{PW}$ | CLK Pulse Width LOW | TTL Output Load | $\frac{5t_{35}}{n}-15$ | | ns |
| 43 | $t_{PD}$ | LIGHTIN to CLK ↓ Delay | TTL Output Load | $\frac{t_{35}}{2n}+17$ | $\frac{t_{35}}{n}+26$ | ns |
| 44 | $t_{PD}$ | CLK ↑ to IGM ↓ | TTL Output | | $\frac{2t_{35}}{n}+7$ | ns |
| 45 | $t_{PD}$ | CLK ↑ to IGM ↑ | TTL Output | | $\frac{2t_{35}}{n}+10$ | ns |
| 46 | $t_{PD}$ | CLK ↓ to IGM ↓ | TTL Output | | 20 | ns |
| 47 | $t_S$ | CNB↑ to CLK↑ Setup Time (Note 5) | | $-\left(\frac{2t_{35}}{n}-32\right)$ | | ns |
| 47A | $t_S$ | CNB↓ to CLK↑ Setup Time (Note 19) | | $-\left(\frac{t_{35}}{n}-31\right)$ | | ns |
| 48 | $t_H$ | CNB↓ to CLK↑ Hold | | $\frac{2t_{35}}{n}+5$ | | ns |
| 49 | $t_{PW}$ | CNB Pulse Width LOW | | $\frac{2t_{35}}{n}$ | | ns |
| 50 | $t_R$ | STRB Rise Time (Note 3) | TTL Output Load | | 17 | ns |
| 51 | $t_F$ | STRB Fall Time (Note 3) | TTL Output Load | | 10 | ns |
| 52 | $t_R$ | CLK Rise Time (Note 3) | TTL Output Load | | 17 | ns |
| 53 | $t_F$ | CLK Fall Time (Note 3) | TTL Output Load | | 10 | ns |
| **Optical Signals** | | | | | | |
| 57 | $t_j$ | LIGHTIN peak-to-peak jitter tolerance | | | 2.5 | ns |
| **Miscellaneous: $X_1$ (Note 15)** | | | | | | |
| 60 | $t_{PW}$ | $X_1$ Pulse Width HIGH | | 35 | | ns |
| 61 | $t_{PW}$ | $X_1$ Pulse Width LOW | | 35 | | ns |

**Note:**

See notes following end of Switching Characteristics tables.

**Notes:**

Notes listed correspond to the respective references made in the DC characteristics and the Switching characteristics tables.

1. For conditions shown as Min. or Max., use the appropriate value specified under operating range.
2. Typical limits are at $V_{CC}$ = 5.0 V, 25°C ambient and maximum loading.
3. Rise and Fall time measurements are made at 20% and 80% points.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. If the CNB↑ to CLK↑ setup time is violated, IGM will stay LOW.
7. $t_4$ guarantees that data is latched. ACK ($t_{11}$) timing may not be valid.
8. If $t_{11}$ is not met, ACK response and timing are not guaranteed, but data will still be latched on STRB↑ (see $t_4$).
9. Measured with device in Test mode while monitoring output logic states.
10. For the FOXI Transmitter, "n" is determined by the state of DMS and TLS inputs.

| DMS | TLS | "n" |
|---|---|---|
| GND | OPEN | n = 1; 8 Bit Test Mode |
| | GND | n = 10; 8 Bit Local Mode |
| VCC | OPEN | n = 1; 9 Bit Test Mode |
| | GND | n = 11; 9 Bit Local Mode |
| Open or $\frac{1}{2}$ VCC | OPEN | n = 1; 10 Bit Test Mode |
| | GND | n = 12; 10 Bit Local Mode |

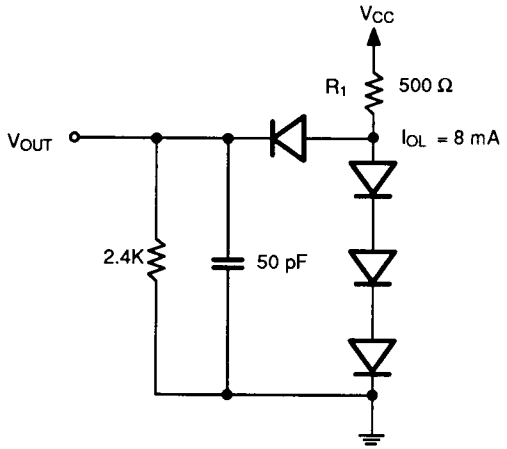
11. $t_6$ (Internal Byte Boundary to CLK↓) is created by the variation of internal STRB propagation delays relative to internal byte boundaries over temperatures and $V_{CC}$. The internal byte boundary determines the byte in which data will come out (SEROUT±). If STRB occurs before the byte boundary, then the data will be sent out two bytes later. If STRB occurs after the byte boundary, then the output data will be delayed by one additional byte.
12. $X_1$ Pulse Width is measured at a point where CLK output exactly meets CLK input ($t_2$ or $t_3$) spec limit.
13. For the FOXI Transmitter, 'Data' is either $DI_0 - DI_7$, $DI_8/CI_3$, $DI_9/CI_2$, $CI_0 - CI_1$. For the FOXI Receiver, 'STRB' is either CSTRB or DSTRB and 'Data' is either $DO_0 - DO_7$, $DO_8/CO_3$, $DO_9/CO_2$, $CO_0 - CO_1$.
14. For the FOXI Receiver, 'n' is determined by the state of the DMS input.

| DMS | "n" |
|---|---|
| GND | n = 10; 8-Bit Local Mode |
| VCC | n = 11; 9-Bit Local Mode |
| Open or $\frac{1}{2}$ VCC | n = 12; 10-Bit Local Mode |

15. Jitter on $X_1$ input must be less than ±0.2 ns.
16. This specification applies to any edge of an incoming pattern.
18. ACK delay is determined by $t_{13}$ when the input latch is empty or by $t_{15}$ when the latch is full (Busy mode). Also note that ACK will not rise if STRB does not remain HIGH until ACK rises.
19. If $t_{47A}$ (CNB↓ to CLK↑ setup) is violated, then output data will occur one byte time later.
20. All timing references are made with respect to +1.5 V for TTL–level signals.
21. Input power needed to transfer 50 Mbytes with no error, while transmitting the FDDI DDJ test pattern.

† Not included in production tests.

## SWITCHING TEST CIRCUITS




**TTL Output Load**

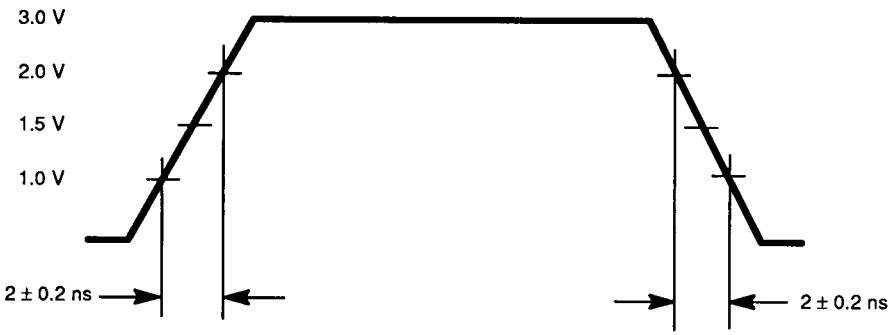
**Notes:**

1. All diodes IN916 or IN3064, or equivalent
2. $C_L$ = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.

14380-007A

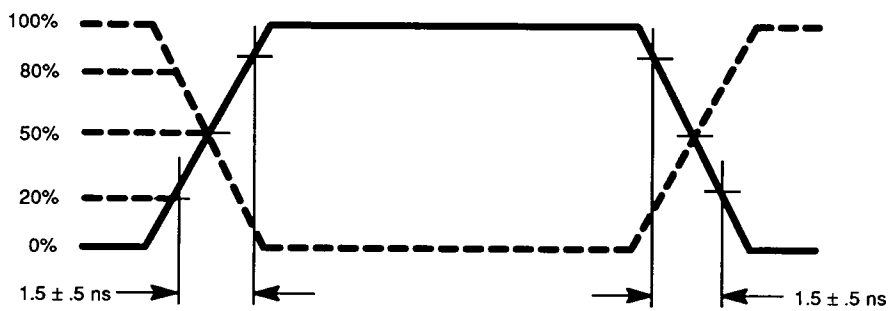
## SWITCHING TEST WAVEFORMS

**TTL Input Waveform**




14380-009A

**Optical Input Waveform**

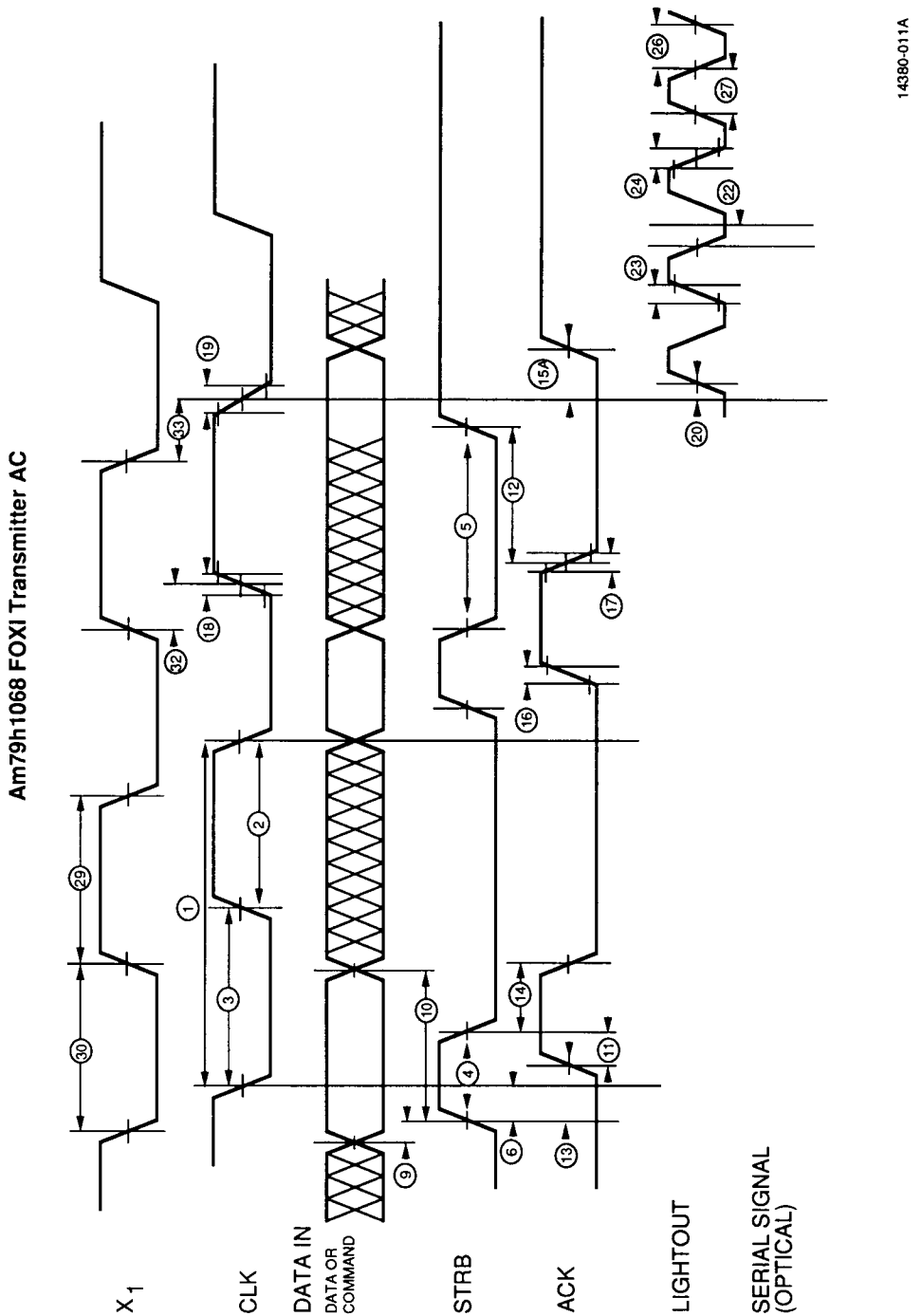



14380-010A

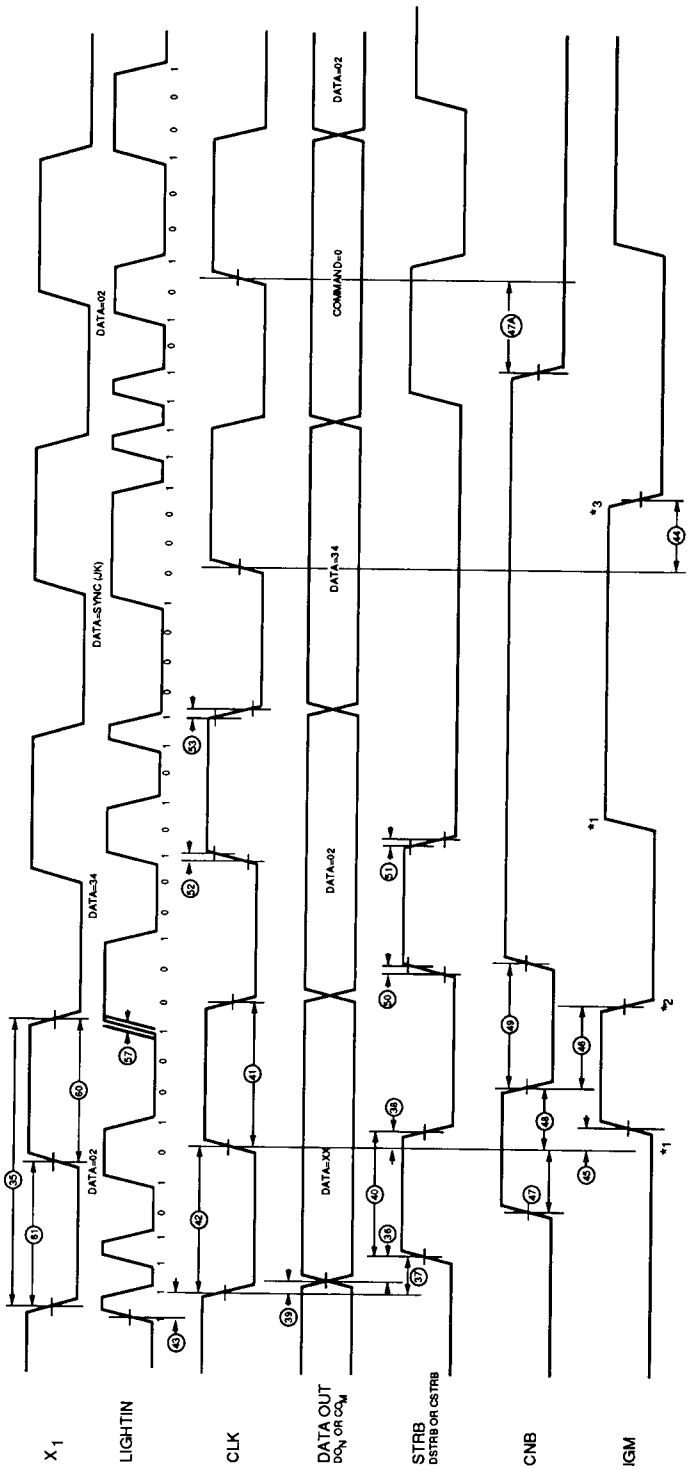
## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must Be Steady | Will Be Steady |
| | May Change from H to L | Will Be Changing from H to L |
| | May Change from L to H | Will Be Changing from L to H |
| | Don't Care Any Change Permitted | Changing State Unknown |
| | Does Not Apply | Center Line is High Impedence "Off" State |

KS000010

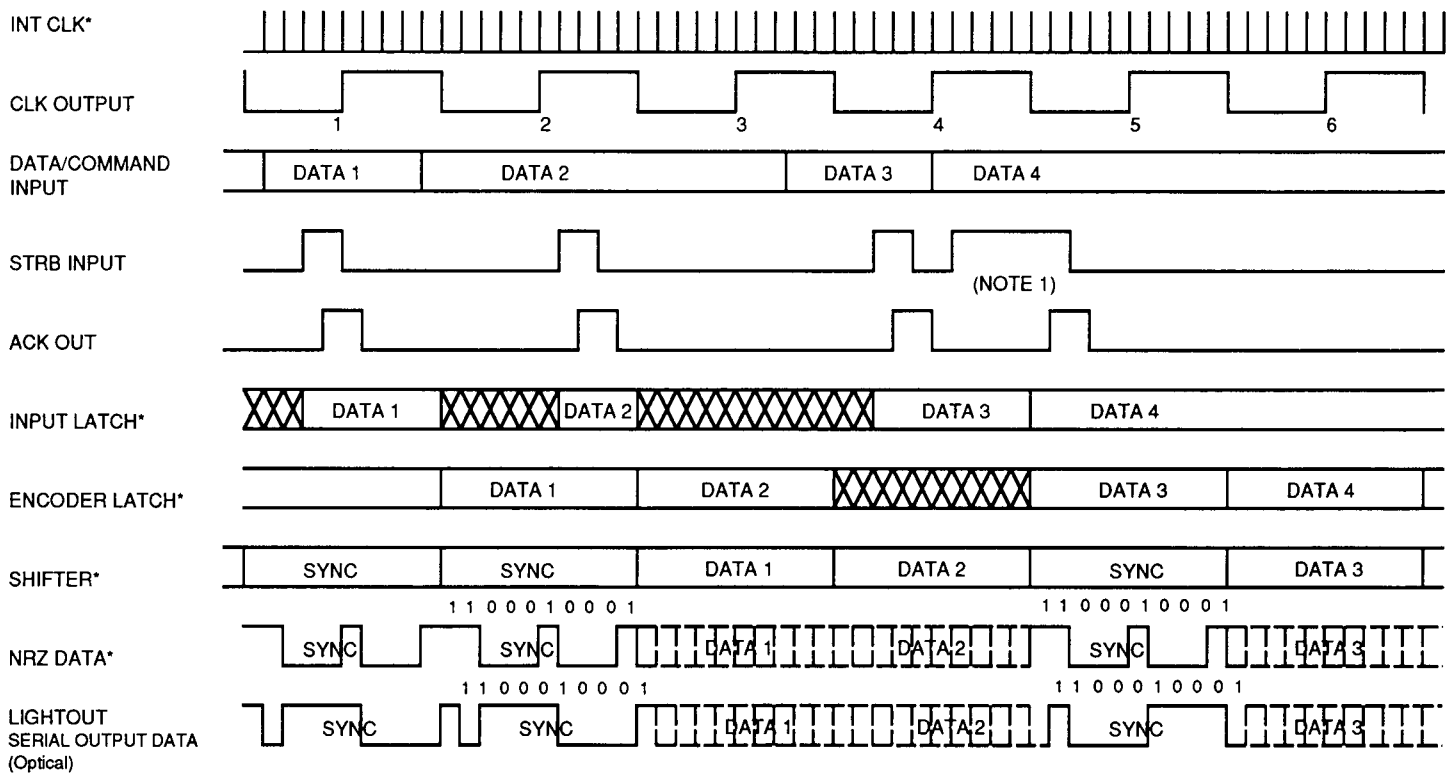

Am79h1068 FOXI Transmitter AC
X1
CLK
DATA IN
DATA OR COMMAND
STRB
ACK
LIGHTOUT
SERIAL SIGNAL (OPTICAL)
14380-011A

**Am79h1069 FOXI Receiver AC**




Note: This diagram illustrates how timing relationships are measured. Functional operation is illustrated on following pages.

**FOXI Transmitter**



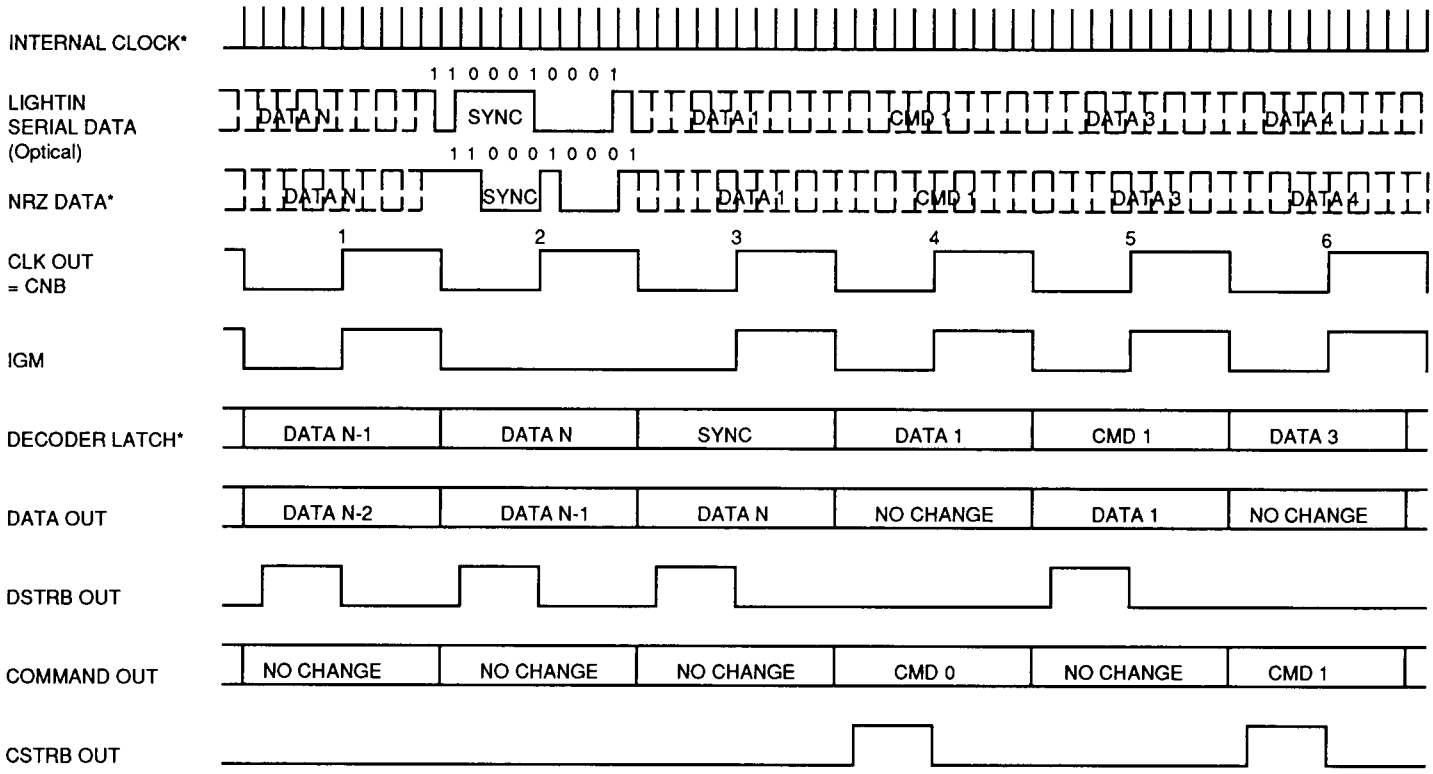

**STRB to LIGHTOUT Timing**
**(8-Bit Local Mode)**

14380-013A

*Internal Signals

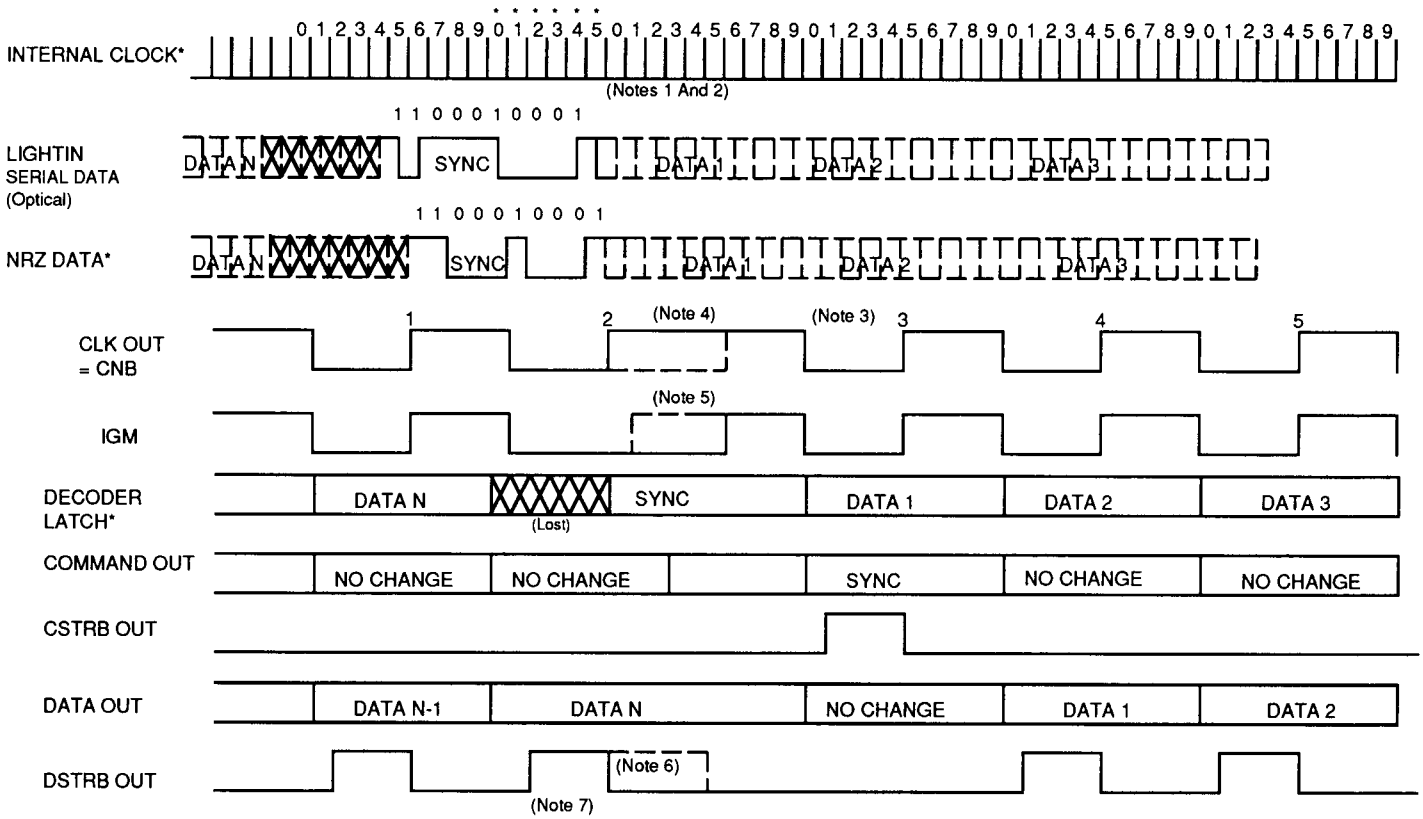
**Note:**
1. The input Latch is BUSY when the second STRB comes in; the internal STRB-ACK is delayed until the next CLK window.

## FOXI Receiver




**FOXI Receiver Timing**
**(8-Bit Local Mode)**

14380-014A




**Timing Showing External Effect of Sync Error (8-Bit Local Mode)**

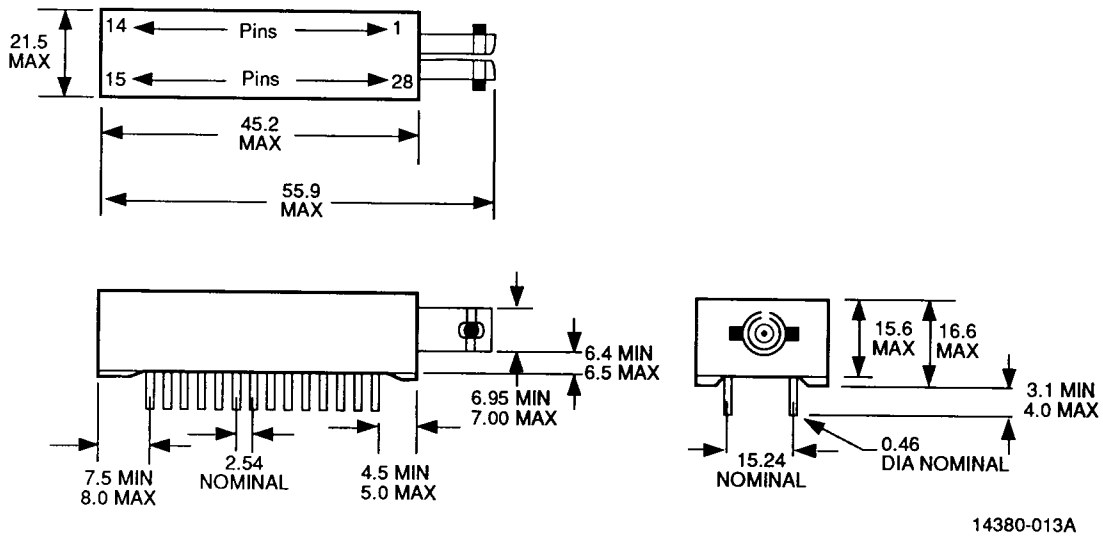
14380-015A

*Internal Signals

**Notes:**

1. Sync detected in Shifter, but not synchronized with internal state machine.
2. State machine re-synched to new sync position.
3. CLK output delayed to new position.
4. CLK LOW or HIGH time gets stretched depending on what states of the internal machine are skipped.
5. IGM rises at the 65$^{th}$ state of the state machine.
6. STRB falls at the rising edge of the CLK Out.
7. STRB may be shifted one bit time if the state machine is reset at state 1.

## PHYSICAL DIMENSION*




* For reference only. All dimensions are measured in mm. BSC is an ANSI standard for Basic Space Centering.

## Sales Offices

## North American

| | | |
|---|---|---|
| ALABAMA | (205) | 882-9122 |
| ARIZONA | (602) | 242-4400 |
| CALIFORNIA, | | |
| Culver City | (213) | 645-1524 |
| Newport Beach | (714) | 752-6262 |
| Roseville | (916) | 786-6700 |
| San Diego | (619) | 560-7030 |
| San Jose | (408) | 452-0500 |
| Woodland Hills | (818) | 992-4155 |
| CANADA, Ontario, | | |
| Kanata | (613) | 592-0060 |
| Willowdale | (416) | 224-5193 |
| COLORADO | (303) | 741-2900 |
| CONNECTICUT | (203) | 264-7800 |
| FLORIDA, | | |
| Clearwater | (813) | 530-9971 |
| Ft. Lauderdale | (305) | 776-2001 |
| Orlando (Casselberry) | (407) | 830-8100 |
| GEORGIA | (404) | 449-7920 |
| ILLINOIS, | | |
| Chicago (Itasca) | (708) | 773-4422 |
| Naperville | (708) | 505-9517 |
| KANSAS | (913) | 451-3115 |
| MARYLAND | (301) | 381-3790 |
| MASSACHUSETTS | (617) | 273-3970 |
| MICHIGAN | (313) | 347-1522 |
| MINNESOTA | (612) | 938-0001 |
| NEW JERSEY, | | |
| Cherry Hill | (609) | 662-2900 |
| Parsippany | (201) | 299-0002 |
| NEW YORK, | | |
| Liverpool | (315) | 457-5400 |
| Poughkeepsie | (914) | 471-8180 |
| Rochester | (716) | 272-9020 |
| NORTH CAROLINA | (919) | 878-8111 |
| OHIO, | | |
| Columbus (Westerville) | (614) | 891-6455 |
| OREGON | (503) | 245-0080 |
| PENNSYLVANIA | (215) | 398-8006 |
| SOUTH CAROLINA | (803) | 772-6760 |
| TEXAS, | | |
| Austin | (512) | 346-7830 |
| Dallas | (214) | 934-9099 |
| Houston | (713) | 785-9001 |
| UTAH | (801) | 264-2900 |

## International

| | | |
|---|---|---|
| BELGIUM, Bruxelles | TEL | (02) 771-91-42 |
| | FAX | (02) 762-37-12 |
| | TLX | 846-61028 |
| FRANCE, Paris | TEL | (1) 49-75-10-10 |
| | FAX | (1) 49-75-10-13 |
| | TLX | 263282F |
| WEST GERMANY, | | |
| Hannover area | TEL | (0511) 736085 |
| | FAX | (0511) 721254 |
| | TLX | 922850 |
| München | TEL | (089) 4114-0 |
| | FAX | (089) 406490 |
| | TLX | 523883 |
| Stuttgart | TEL | (0711) 62 33 77 |
| | FAX | (0711) 625187 |
| | TLX | 721882 |
| HONG KONG, | TEL | 852-5-8654525 |
| Wanchai | FAX | 852-5-8654335 |
| | TLX | 67955AMDAPHX |
| ITALY, Milan | TEL | (02) 3390541 |
| | | (02) 3533241 |
| | FAX | (02) 3498000 |
| | TLX | 843-315286 |
| JAPAN, | | |
| Atsugi | TEL | 462-29-8460 |
| | FAX | 462-29-8458 |
| Kanagawa | TEL | 462-47-2911 |
| | FAX | 462-47-1729 |
| Tokyo | TEL | (03) 346-7550 |
| | FAX | (03) 342-5196 |
| | TLX | J24064AMDTKOJ |

## International (Continued)

| | | |
|---|---|---|
| Osaka | TEL | 06-243-3250 |
| | FAX | 06-243-3253 |
| KOREA, Seoul | TEL | 822-784-0030 |
| | FAX | 822-784-8014 |
| LATIN AMERICA, | | |
| Ft. Lauderdale | TEL | (305) 484-8600 |
| | FAX | (305) 485-9736 |
| | TLX | 5109554261 AMDFTL |
| NORWAY, Hovik | TEL | (03) 010156 |
| | FAX | (02) 591959 |
| | TLX | 79079HBCN |
| SINGAPORE | TEL | 65-3481188 |
| | FAX | 65-3480161 |
| | TLX | 55650 AMDMMI |
| SWEDEN, | | |
| Stockholm | TEL | (08) 733 03 50 |
| (Sundbyberg) | FAX | (08) 733 22 85 |
| | TLX | 11602 |
| TAIWAN | TEL | 886-2-7213393 |
| | FAX | 886-2-7723422 |
| | TLX | 886-2-7122066 |
| UNITED KINGDOM, | | |
| Manchester area | TEL | (0925) 828008 |
| (Warrington) | FAX | (0925) 827693 |
| | TLX | 851-628524 |
| London area | TEL | (0483) 740440 |
| (Woking) | FAX | (0483) 756196 |
| | TLX | 851-859103 |

## North American Representatives

| | | |
|---|---|---|
| CANADA | | |
| Burnaby, B.C. | | |
| DAVETEK MARKETING | (604) | 430-3680 |
| Calgary, Alberta | | |
| DAVETEK MARKETING | (403) | 291-4984 |
| Kanata, Ontario | | |
| VITEL ELECTRONICS | (613) | 592-0060 |
| Mississauga, Ontario | | |
| VITEL ELECTRONICS | (416) | 676-9720 |
| Lachine, Quebec | | |
| VITEL ELECTRONICS | (514) | 636-5951 |
| IDAHO | | |
| INTERMOUNTAIN TECH MKTG, INC | (208) | 888-6071 |
| ILLINOIS | | |
| HEARTLAND TECH MKTG, INC | (312) | 577-9222 |
| INDIANA | | |
| Huntington - ELECTRONIC MARKETING CONSULTANTS, INC | (317) | 921-3450 |
| Indianapolis - ELECTRONIC MARKETING CONSULTANTS, INC | (317) | 921-3450 |
| IOWA | | |
| LORENZ SALES | (319) | 377-4666 |
| KANSAS | | |
| Merriam – LORENZ SALES | (913) | 469-1312 |
| Wichita – LORENZ SALES | (316) | 721-0500 |
| KENTUCKY | | |
| ELECTRONIC MARKETING CONSULTANTS, INC | (317) | 921-3452 |
| MICHIGAN | | |
| Birmingham - MIKE RAICK ASSOCIATES | (313) | 644-5040 |
| Holland – COM-TEK SALES, INC | (616) | 392-7100 |
| Novi – COM-TEK SALES, INC | (313) | 344-1409 |
| MINNESOTA | | |
| Mel Foster Tech. Sales, Inc. | (612) | 941-9790 |
| MISSOURI | | |
| LORENZ SALES | (314) | 997-4558 |
| NEBRASKA | | |
| LORENZ SALES | (402) | 475-4660 |
| NEW MEXICO | | |
| THORSON DESERT STATES | (505) | 293-8555 |
| NEW YORK | | |
| East Syracuse – NYCOM, INC | (315) | 437-8343 |
| Woodbury – COMPONENT CONSULTANTS, INC | (516) | 364-8020 |
| OHIO | | |
| Centerville – DOLFUSS ROOT & CO | (513) | 433-6776 |
| Columbus – DOLFUSS ROOT & CO | (614) | 885-4844 |
| Strongsville – DOLFUSS ROOT & CO | (216) | 238-0300 |
| PENNSYLVANIA | | |
| DOLFUSS ROOT & CO | (412) | 221-4420 |
| PUERTO RICO | | |
| COMP. REP ASSOC, INC | (809) | 746-6550 |
| UTAH, $R^2$ MARKETING | (801) | 595-0631 |
| WASHINGTON | | |
| ELECTRA TECHNICAL SALES | | |
| WISCONSIN | | |
| HEARTLAND TECH MKTG, INC | | |

026711 ✓ R



**Advanced Micro Devices, Inc.** 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
***APPLICATIONS HOTLINE & LITERATURE ORDERING*** • TOLL FREE: (800) 222-9323 • (408) 749-5703


4/20/90
WCP-11M-6/90-0 Printed in USA