HM66AQB36102/HM66AQB18202 HM66AQB9402

36-Mbit QDR™II SRAM 2-word Burst

REJ03C0049-0100
Rev.1.00
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Description

The HM66AQB36102 is a 1,048,576-word by 36-bit, the HM66AQB18202 is a 2,097,152-word by 18-bit, and the HM66AQB9402 is a 4,194,304-word by 9-bit synchronous quad data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell. It integrates unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and $\overline{K}$) and are latched on the positive edge of K and $\overline{K}$. These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin plastic FBGA package.

Features

- 1.8 V ± 0.1 V power supply for core (V_{DD})
- 1.4 V to V_{DD} power supply for I/O (V_{DDQ})
- DLL circuitry for wide output data valid window and future frequency scaling
- Separate independent read and write data ports with concurrent transactions
- 100% bus utilization DDR read and write operation
- Two-tick burst for low DDR transaction size
- Two input clocks (K and $\overline{K}$) for precise DDR timing at clock rising edges only
- Two output clocks (C and $\overline{C}$) for precise flight time and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability with µs restart
- User programmable impedance output
- Fast clock cycle time: 4.0 ns (250 MHz)/5.0 ns (200 MHz)/6.0 ns (167 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

Part No. Information

Catalogue Part No.	Ordering Part No.	Organi-zation	Cycle time	Clock frequency	Package
HM66AQB36102BP-40	HM6AQB36102BP40	1-M word × 36-bit	4.0 ns	250 MHz	Plastic FBGA 165-pin PLBG0165FB-A (BP-165A)
HM66AQB36102BP-50	HM6AQB36102BPL50		5.0 ns	200 MHz	
HM66AQB36102BP-60	HM6AQB36102BPL60		6.0 ns	167 MHz	
HM66AQB18202BP-40	HM6AQB18202BP40	2-M word × 18-bit	4.0 ns	250 MHz	
HM66AQB18202BP-50	HM6AQB18202BPL50		5.0 ns	200 MHz	
HM66AQB18202BP-60	HM6AQB18202BPL60		6.0 ns	167 MHz	
HM66AQB9402BP-40	HM6AQB9402BP40	4-M word × 9-bit	4.0 ns	250 MHz	
HM66AQB9402BP-50	HM6AQB9402BPL50		5.0 ns	200 MHz	
HM66AQB9402BP-60	HM6AQB9402BPL60		6.0 ns	167 MHz	

Note: QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress Semiconductor, IDT, NEC, Samsung, and Renesas Technology Corp.

Pin Arrangement (165PIN-BGA)

HM66AQB36102

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}	NC	$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{R}$	SA	NC	CQ
B	Q27	Q18	D18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

(Top view)

HM66AQB18202

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}	SA	$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NC	$\overline{R}$	SA	NC	CQ
B	NC	Q9	D9	SA	NC	K	$\overline{BW0}$	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

(Top view)

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	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}	SA	$\overline{W}$	NC	$\overline{K}$	NC	$\overline{R}$	SA	SA	CQ
B	NC	NC	NC	SA	NC	K	$\overline{BW}$	SA	NC	NC	Q4
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D4
D	NC	D5	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	Q5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D3	Q3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	D6	Q6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q2	D2
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	Q7	D7	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D1
N	NC	D8	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	Q8	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

(Top view)

Notes on Usage

- Power-on initialization cycles are required for all operations, including JTAG functions, to become normal.
- Clock recovery initialization cycles are required for read/write operations to become normal.
- Output buffer impedance can be programmed by terminating the ZQ ball to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 10% is 250 Ω typical. The total external capacitance of ZQ ball must be less than 7.5 pF.

Pin Descriptions

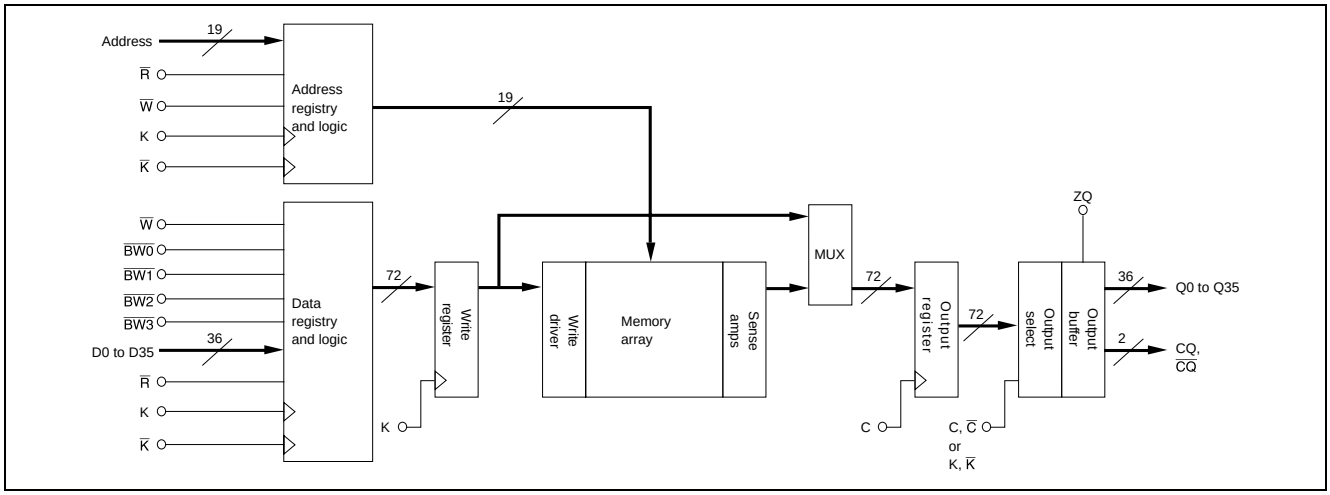
Name	I/O type	Descriptions
SA	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K for READ cycles and must meet the setup and hold times around the rising edge of $\overline{K}$ for WRITE cycles. All transactions operate on a burst-of-two words (one clock period of bus activity). These inputs are ignored when device is deselected.
$\overline{R}$	Input	Synchronous read: When low, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
$\overline{W}$	Input	Synchronous write: When low, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
$\overline{BW}$ $\overline{BWn}$	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and $\overline{K}$ for each of the two rising edges comprising the WRITE cycle. See Byte Write Truth Table for signal to data relationship.
K, $\overline{K}$	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of $\overline{K}$. $\overline{K}$ is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain V_{REF} level.
C, $\overline{C}$	Input	Output clock: This clock pair provides a user-controlled means of tuning device output data. The rising edge of $\overline{C}$ is used as the output timing reference for first output data. The rising edge of C is used as the output timing reference for second output data. Ideally, $\overline{C}$ is 180 degrees out of phase with C. C and $\overline{C}$ may be tied high to force the use of K and $\overline{K}$ as the output reference clocks instead of having to provide C and $\overline{C}$ clocks. If tied high, C and $\overline{C}$ must remain high and not to be toggled during device operation. These balls cannot remain V_{REF} level.
$\overline{DOFF}$	Input	DLL disable: When low, this input causes the DLL to be bypassed for stable, low frequency operation.
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. Q and CQ output impedance are set to 0.2 × RQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This ball cannot be connected directly to V_{SS} or left unconnected.
TMS TDI	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.
TCK	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.
D0 to Dn	Input	Synchronous data inputs: Input data must meet setup and hold times around the rising edges of K and $\overline{K}$ during WRITE operations. See Pin Arrangement figures for ball site location of individual signals. The ×9 device uses D0 to D8. Remaining signals are NC. The ×18 device uses D0 to D17. Remaining signals are NC. The ×36 device uses D0 to D35.
CQ, $\overline{CQ}$	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tri-states.
TDO	Output	IEEE 1149.1 test output: 1.8 V I/O level.
Q0 to Qn	Output	Synchronous data outputs: Output data is synchronized to the respective C and $\overline{C}$, or to the respective K and $\overline{K}$ if C and $\overline{C}$ are tied high. This bus operates in response to $\overline{R}$ commands. See Pin Arrangement figures for ball site location of individual signals. The ×9 device uses Q0 to Q8. Remaining signals are NC. The ×18 device uses Q0 to Q17. Remaining signals are NC. The ×36 device uses Q0 to Q35.
V_{DD}	Supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.
V_{DDQ}	Supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. 1.8 V is also permissible. See DC Characteristics and Operating Conditions for range.

Name	I/O type	Descriptions
V_{SS}	Supply	Power supply: Ground
V_{REF}	—	HSTL input reference voltage: Nominally $V_{DDQ}/2$, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.
NC	—	No connect: These signals are internally connected. These signals may be connected to ground to improve package heat dissipation.

Note: 1. All power supply and ground balls must be connected for proper operation of the device.

Block Diagram

HM66AQB36102



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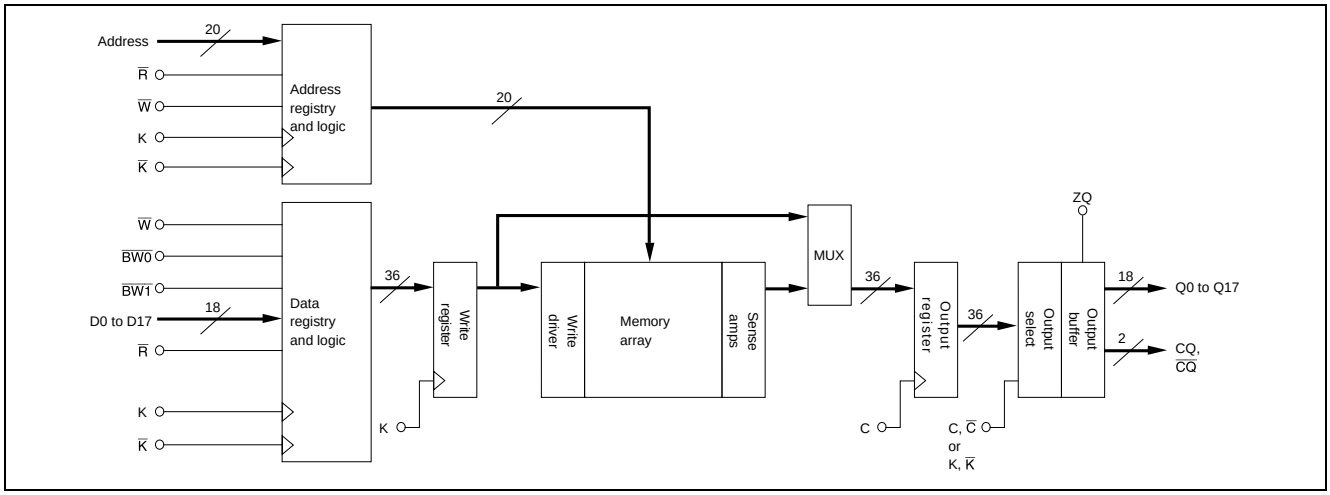

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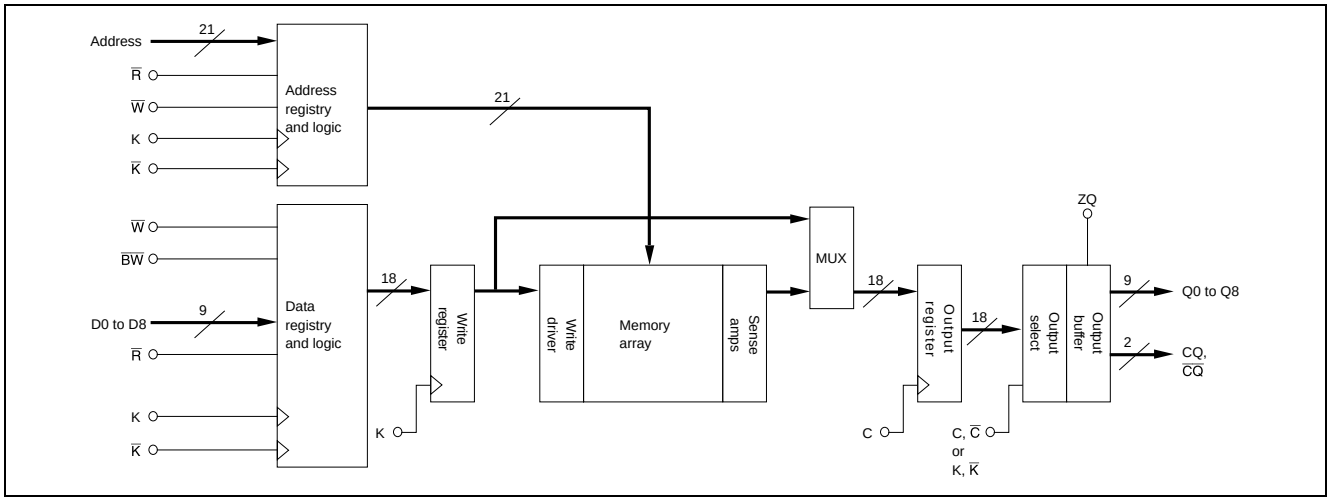

Truth Table

Operation	K	R	W	D or Q		
WRITE cycle Load address, input write data on consecutive K and K rising edges	L→H	×	L	Data in		
				Input data	D(A+0)	D(A+1)
				Input clock	K(t)↑	K(t)↑
READ cycle Load address, output data on consecutive C and C rising edges	L→H	L	×	Data out		
				Output data	Q(A+0)	Q(A+1)
				Output clock	C(t+1)↑	C(t+2)↑
NOP (No operation)	L→H	H	H	D = × or Q = High-Z		
STANDBY (Clock stopped)	Stopped	×	×	Previous state		

Notes: 1. H: high level, L: low level, ×: don't care, ↑: rising edge.

2. Data inputs are registered at K and K rising edges. Data outputs are delivered at C and C rising edges, except if C and C are high, then data outputs are delivered at K and K rising edges.
3. R and W must meet setup/hold times around the rising edges (low to high) of K and are registered at the rising edge of K.
4. This device contains circuitry that will ensure the outputs will be in high-Z during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. When clocks are stopped, the following cases are recommended; the case of K = low, K = high, C = low and C = high, or the case of K = high, K = low, C = high and C = low. This condition is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

Byte Write Truth Table

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Operation	K	$\overline{K}$	$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$
Write D0 to D35	L→H	—	L	L	L	L
	—	L→H	L	L	L	L
Write D0 to D8	L→H	—	L	H	H	H
	—	L→H	L	H	H	H
Write D9 to D17	L→H	—	H	L	H	H
	—	L→H	H	L	H	H
Write D18 to D26	L→H	—	H	H	L	H
	—	L→H	H	H	L	H
Write D27 to D35	L→H	—	H	H	H	L
	—	L→H	H	H	H	L
Write nothing	L→H	—	H	H	H	H
	—	L→H	H	H	H	H

Notes: 1. H: high level, L: low level, →: rising edge.
2. Assumes a WRITE cycle was initiated. $\overline{BW0}$ to $\overline{BW3}$ can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

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Operation	K	$\overline{K}$	$\overline{BW0}$	$\overline{BW1}$
Write D0 to D17	L→H	—	L	L
	—	L→H	L	L
Write D0 to D8	L→H	—	L	H
	—	L→H	L	H
Write D9 to D17	L→H	—	H	L
	—	L→H	H	L
Write nothing	L→H	—	H	H
	—	L→H	H	H

Notes: 1. H: high level, L: low level, →: rising edge.
2. Assumes a WRITE cycle was initiated. $\overline{BW0}$ and $\overline{BW1}$ can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

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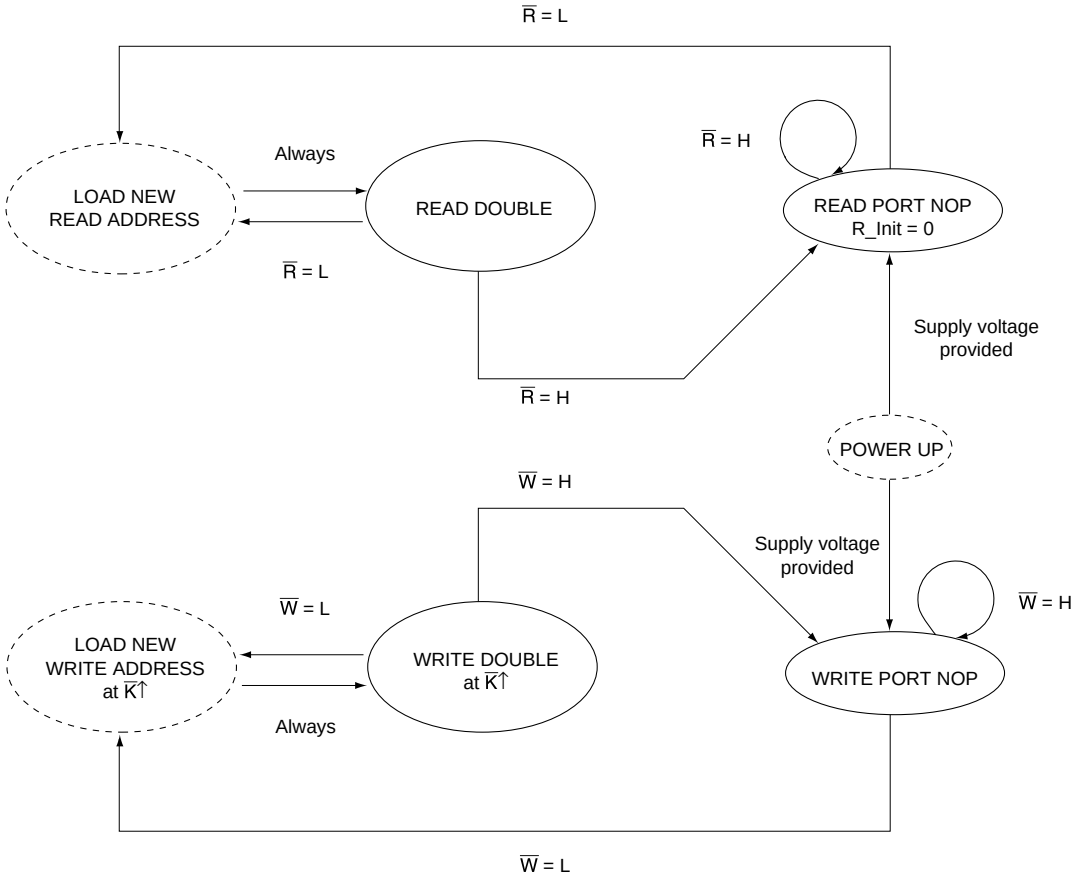
Operation	K	$\overline{K}$	$\overline{BW}$
Write D0 to D8	L→H	—	L
	—	L→H	L
Write nothing	L→H	—	H
	—	L→H	H

Notes: 1. H: high level, L: low level, →: rising edge.
2. Assumes a WRITE cycle was initiated. $\overline{BW}$ can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Notes:
1. The address is concatenated with one additional internal LSB to facilitate burst operation. The address order is always fixed as: xxx…xxx+0, xxx…xxx+1.
   Bus cycle is terminated at the end of this sequence (burst count = 2).
2. Read and write state machines can be active simultaneously.
3. State machine control timing sequence is controlled by K.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any ball	V_{IN}	–0.5 to V_{DD} + 0.5 (2.5 V max.)	V	1, 4
Input/output voltage	$V_{I/O}$	–0.5 to V_{DDQ} + 0.5 (2.5 V max.)	V	1, 4
Core supply voltage	V_{DD}	–0.5 to 2.5	V	1, 4
Output supply voltage	V_{DDQ}	–0.5 to V_{DD}	V	1, 4
Junction temperature	Tj	+125 (max)	°C	
Storage temperature	T_{STG}	–55 to +125	°C	

Notes:
1. All voltage is referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 2.5 V, whatever the instantaneous value of V_{DDQ}.

Recommended DC Operating Conditions

(Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage -- core	V_{DD}	1.7	1.8	1.9	V	
Power supply voltage -- I/O	V_{DDQ}	1.4	1.5	V_{DD}	V	
Input reference voltage -- I/O	V_{REF}	0.68	0.75	0.95	V	1
Input high voltage	$V_{IH\ (DC)}$	V_{REF} + 0.1	—	V_{DDQ} + 0.3	V	2, 3
Input low voltage	$V_{IL\ (DC)}$	–0.3	—	V_{REF} – 0.1	V	2, 3

Notes: 1. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

2. Overshoot: $V_{IH\ (AC)} \leq V_{DDQ} + 0.5$ V for $t \leq t_{KHKH}/2$
   Undershoot: $V_{IL\ (AC)} \geq -0.5$ V for $t \leq t_{KHKH}/2$
   Power-up: $V_{IH} \leq V_{DDQ} + 0.3$ V and $V_{DD} \leq 1.7$ V and $V_{DDQ} \leq 1.4$ V for $t \leq 200$ ms
   During normal operation, V_{DDQ} must not exceed V_{DD}.
   Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).

3. These are DC test criteria. The AC V_{IH} / V_{IL} levels are defined separately to measure timing parameters.

DC Characteristics

(Ta = 0 to +70°C, V_{DD} = 1.8 V ± 0.1 V)

Parameter		Symbol	HM66AQB36102/HM66AQB18202 HM66AQB9402			Unit	Notes
			-40	-50	-60		
			Max				
Operating supply current (READ / WRITE)	(×9 / ×18)	I_{DD}	740	620	550	mA	1, 2, 3
	(×36)	I_{DD}	800	670	590	mA	1, 2, 3
Standby supply current (NOP)	(×9 / ×18 / ×36)	I_{SB1}	300	280	260	mA	2, 4, 5

Parameter	Symbol	Min	Max	Unit	Test conditions	Notes
Input leakage current	I_{LI}	–2	2	µA		10
Output leakage current	I_{LO}	–2	2	µA		11
Output high voltage	V_{OH} (Low)	V_{DDQ} – 0.2	V_{DDQ}	V	$\|I_{OH}\| \leq 0.1$ mA	8, 9
	V_{OH}	$V_{DDQ}/2$ – 0.08	$V_{DDQ}/2$ + 0.08	V	Notes6	8, 9
Output low voltage	V_{OL} (Low)	V_{SS}	0.2	V	$I_{OL} \leq 0.1$ mA	8, 9
	V_{OL}	$V_{DDQ}/2$ – 0.08	$V_{DDQ}/2$ + 0.08	V	Notes7	8, 9

Notes: 1. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.

2. I_{OUT} = 0 mA. $V_{DD} = V_{DD}$ max, $t_{KHKH} = t_{KHKH}$ min.
3. Operating supply currents are measured at 100% bus utilization.
4. All address / data inputs are static at either $V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$.
5. NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.
6. Outputs are impedance-controlled. $|I_{OH}| = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
7. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of 175 Ω ≤ RQ ≤ 350 Ω.
8. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
9. HSTL outputs meet JEDEC HSTL Class I and Class II standards.
10. $0 \leq V_{IN} \leq V_{DDQ}$ for all input balls (except V_{REF}, ZQ, TCK, TMS, TDI ball).
11. $0 \leq V_{OUT} \leq V_{DDQ}$ (except TDO ball), output disabled.

Capacitance

($Ta = +25°C$, $f = 1.0$ MHz, $V_{DD} = 1.8$ V, $V_{DDQ} = 1.5$ V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	C_{IN}	—	4	5	pF	V_{IN} = 0 V
Clock input capacitance	C_{CLK}	—	5	6	pF	V_{CLK} = 0 V
Input/output capacitance (D, Q, ZQ)	$C_{I/O}$	—	6	7	pF	$V_{I/O}$ = 0 V

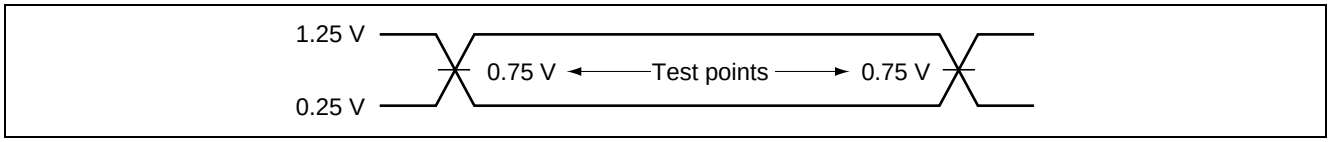
Notes: 1. These parameters are sampled and not 100% tested.
2. Except JTAG (TCK, TMS, TDI, TDO) pins.

AC Characteristics

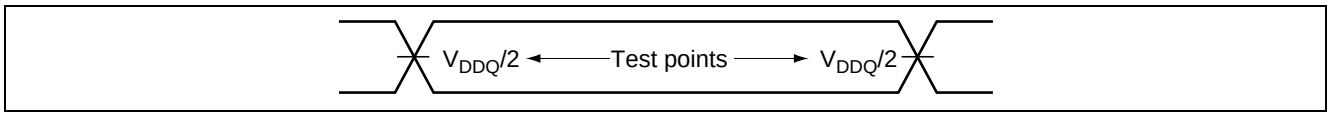
($Ta = 0$ to $+70°C$, $V_{DD} = 1.8$ V ± 0.1 V)

Test Conditions

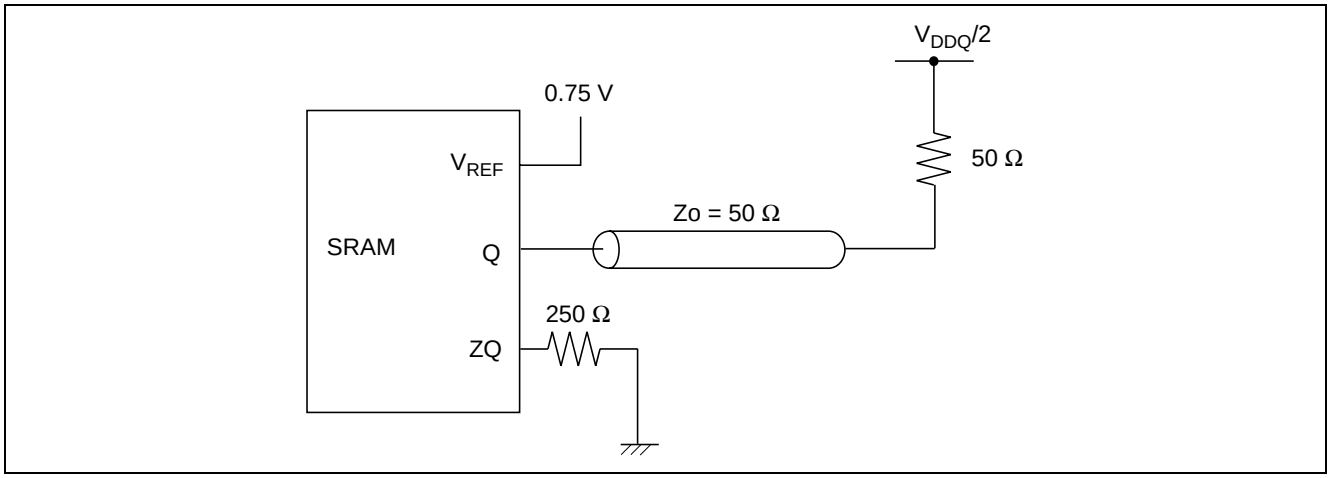
Input waveform (Rise/fall time ≤ 0.3 ns)



Output waveform



Output load condition



Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH\ (AC)}$	V_{REF} + 0.2	—	—	V	1, 2, 3, 4
Input low voltage	$V_{IL\ (AC)}$	—	—	V_{REF} – 0.2	V	1, 2, 3, 4

Notes: 1. All voltages referenced to V_{SS} (GND).

2. These conditions are for AC functions only, not for AC parameter test.
3. Overshoot: $V_{IH\ (AC)} \leq V_{DDQ}$ + 0.5 V for $t \leq t_{KHKH}/2$
   Undershoot: $V_{IL\ (AC)} \geq$ –0.5 V for $t \leq t_{KHKH}/2$
   Power-up: $V_{IH} \leq V_{DDQ}$ + 0.3 V and $V_{DD} \leq$ 1.7 V and $V_{DDQ} \leq$ 1.4 V for $t \leq$ 200 ms
   During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals may not have pulse widths less than t_{KHKL} (min) or operate at cycle rates less than t_{KHKH} (min).
4. To maintain a valid level, the transitioning edge of the input must:
   a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL\ (AC)}$ or $V_{IH\ (AC)}$.
   b. Reach at least the target AC level.
   c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL\ (DC)}$ or $V_{IH\ (DC)}$.

Parameter	Symbol	HM66AQB36102/HM66AQB18202 HM66AQB9402						Unit	Notes
		-40		-50		-60			
		Min	Max	Min	Max	Min	Max		
Average clock cycle time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKH}	4.00	5.25	5.00	6.30	6.00	7.88	ns	
Clock phase jitter (K, $\overline{K}$, C, $\overline{C}$)	t_{KC} var	—	0.20	—	0.20	—	0.20	ns	3
Clock high time (K, $\overline{K}$, C, $\overline{C}$)	t_{KHKL}	1.60	—	2.00	—	2.40	—	ns	
Clock low time (K, $\overline{K}$, C, $\overline{C}$)	t_{KLKH}	1.60	—	2.00	—	2.40	—	ns	
Clock to $\overline{\text{clock}}$ (K to $\overline{K}$, C to $\overline{C}$)	$t_{KH/KH}$	1.80	—	2.20	—	2.70	—	ns	
$\overline{\text{Clock}}$ to clock ($\overline{K}$ to K, $\overline{C}$ to C)	$t_{/KHKH}$	1.80	—	2.20	—	2.70	—	ns	
Clock to data clock (K to C, $\overline{K}$ to $\overline{C}$)	t_{KHCH}	0	1.80	0	2.30	0	2.80	ns	
DLL lock time (K, C)	t_{KC} lock	1,024	—	1,024	—	1,024	—	Cycle	2
K static to DLL reset	t_{KC} reset	30	—	30	—	30	—	ns	7
C, $\overline{C}$ high to output valid	t_{CHQV}	—	0.45	—	0.45	—	0.50	ns	
C, $\overline{C}$ high to output hold	t_{CHQX}	–0.45	—	–0.45	—	–0.50	—	ns	
C, $\overline{C}$ high to echo clock valid	t_{CHCQV}	—	0.45	—	0.45	—	0.50	ns	
C, $\overline{C}$ high to echo clock hold	t_{CHCQX}	–0.45	—	–0.45	—	–0.50	—	ns	

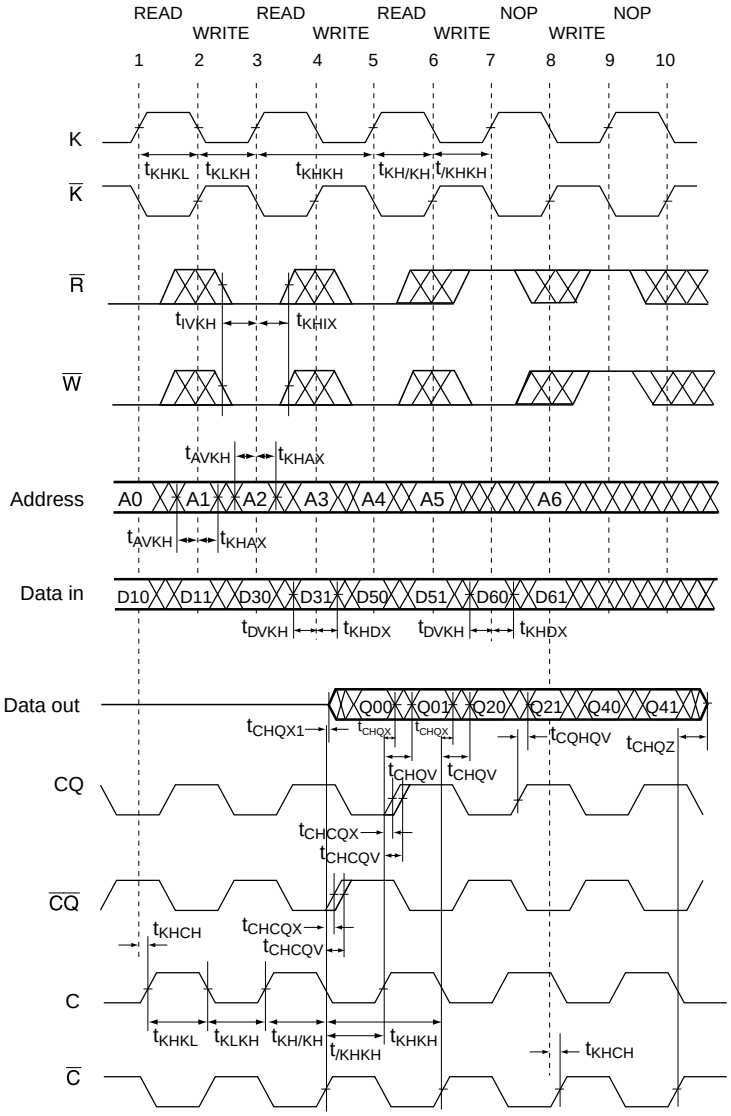
Parameter	Symbol	HM66AQB36102/HM66AQB18202 HM66AQB9402						Unit	Notes
		-40		-50		-60			
		Min	Max	Min	Max	Min	Max		
CQ, $\overline{CQ}$ high to output valid	t_{CQHQV}	—	0.30	—	0.35	—	0.40	ns	4, 7
CQ, $\overline{CQ}$ high to output hold	t_{CQHQX}	–0.30	—	–0.35	—	–0.40	—	ns	4, 7
C, $\overline{C}$ high to output high-Z	t_{CHQZ}	—	0.45	—	0.45	—	0.50	ns	5
C, $\overline{C}$ high to output low-Z	t_{CHQX1}	–0.45	—	–0.45	—	–0.50	—	ns	5
Address valid to K rising edge	t_{AVKH}	0.35	—	0.40	—	0.50	—	ns	1
Control inputs valid to K rising edge	t_{IVKH}	0.35	—	0.40	—	0.50	—	ns	1
Data-in valid to K, $\overline{K}$ rising edge	t_{DVKH}	0.35	—	0.40	—	0.50	—	ns	1
K rising edge to address hold	t_{KHAX}	0.35	—	0.40	—	0.50	—	ns	1
K rising edge to control inputs hold	t_{KHIX}	0.35	—	0.40	—	0.50	—	ns	1
K, $\overline{K}$ rising edge to data-in hold	t_{KHDX}	0.35	—	0.40	—	0.50	—	ns	1

Notes: 1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.
2. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
It is recommended that the device is kept inactive during these cycles.
3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
4. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guardbands and test setup variations.
5. Transitions are measured ±100 mV from steady-state voltage.
6. At any given voltage and temperature t_{CHQZ} is less than t_{CHQX1} and t_{CHQZ} less than t_{CHQV}.
7. These parameters are sampled.

Remarks: 1. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
2. Control input signals may not be operated with pulse widths less than t_{KHKL} (min).
3. If C, $\overline{C}$ are tied high, K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters.
4. V_{DDQ} is +1.5 V DC.
5. Control signals are $\overline{R}$, $\overline{W}$, $\overline{BW}$, $\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$ and $\overline{BW3}$.

Timing Waveforms

Read and Write Timing



Notes:
1. Q00 refers to output from address A0+0. Q01 refers to output from the next internal burst address following A0, i.e., A0+1.
2. Outputs are disable (high-Z) one clock cycle after a NOP.
3. In this example, if address A0 = A1, then data Q00 = D10, Q01 = D11. Write data is forwarded immediately as read results.
4. To control read and write operations, $\overline{BW}$ signals must operate at the same timing as Data in.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.
TDI and TMS are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a 1kΩ resistor.
TDO should be left unconnected.

Test Access Port (TAP) Pins

Symbol I/O	Pin assignments	Description
TCK	2R	Test clock input. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test mode select. This is the command input for the TAP controller state machine.
TDI	11R	Test data input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test data output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note: The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on SRAM POWER-UP.

TAP DC Operating Characteristics

($Ta = 0$ to $+70°C$, $V_{DD} = 1.8\ V \pm 0.1\ V$)

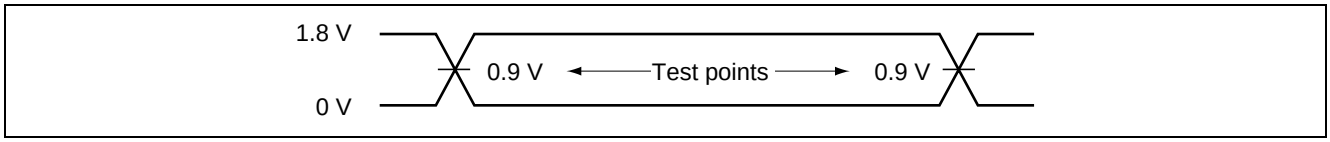
Parameter	Symbol	Min	Max	Unit	Conditions
Input high voltage	V_{IH}	+1.3	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	–0.3	+0.5	V	
Input leakage current	I_{LI}	–5.0	+5.0	µA	$0\ V \le V_{IN} \le V_{DD}$
Output leakage current	I_{LO}	–5.0	+5.0	µA	$0\ V \le V_{IN} \le V_{DD}$, output disabled
Output low voltage	V_{OL1}	—	0.2	V	I_{OLC} = 100 µA
	V_{OL2}	—	0.4	V	I_{OLT} = 2 mA
Output high voltage	V_{OH1}	1.6	—	V	$\|I_{OHC}\|$ = 100 µA
	V_{OH2}	1.4	—	V	$\|I_{OHT}\|$ = 2 mA

Notes: 1. All voltages referenced to V_{SS} (GND).
2. Power-up: $V_{IH} \le V_{DDQ} + 0.3\ V$ and $V_{DD} \le +1.7\ V$ and $V_{DDQ} \le +1.4\ V$ for $t \le 200$ ms.
3. In “EXTEST” mode and “SAMPLE” mode, V_{DDQ} is nominally 1.5 V.
4. ZQ: $V_{IH} = V_{DDQ}$.

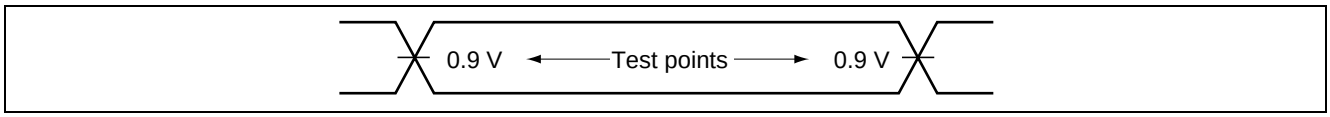
TAP AC Test Condition

- Temperature — 0°C ≤ Ta ≤ +70°C
- Input timing measurement reference levels — 0.9 V
- Input pulse levels — 0 V to 1.8 V
- Input rise/fall time — ≤ 1.0 ns
- Output timing measurement reference levels — 0.9 V
- Test load termination supply voltage (V_{TT}) — 0.9 V
- Output load — See figures

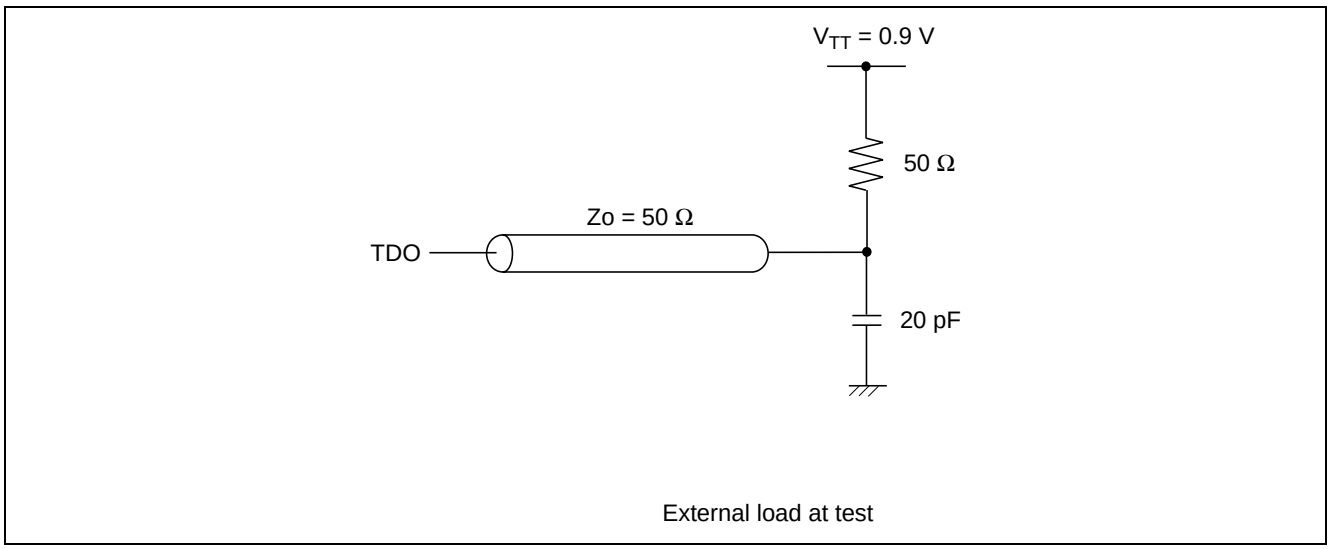
Input waveform



Output waveform



Output load



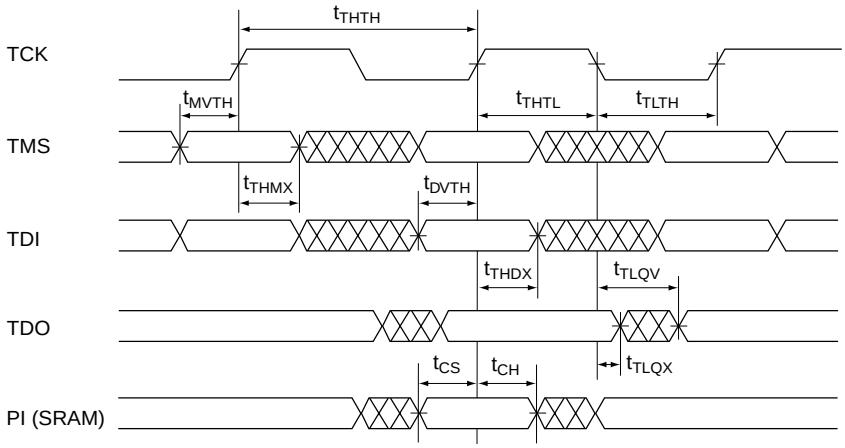
TAP AC Operating Characteristics

($Ta = 0$ to $+70°C$, $V_{DD} = 1.8\ V \pm 0.1\ V$)

Parameter	Symbol	Min	Max	Unit	Note
Test clock cycle time	t_{THTH}	100	—	ns	
Test clock high pulse width	t_{THTL}	40	—	ns	
Test clock low pulse width	t_{TLTH}	40	—	ns	
Test mode select setup	t_{MVTH}	10	—	ns	
Test mode select hold	t_{THMX}	10	—	ns	
Capture setup	t_{CS}	10	—	ns	1
Capture hold	t_{CH}	10	—	ns	1
TDI valid to TCK high	t_{DVTH}	10	—	ns	
TCK high to TDI invalid	t_{THDX}	10	—	ns	
TCK low to TDO unknown	t_{TLQX}	0	—	ns	
TCK low to TDO valid	t_{TLQV}	—	20	ns	

Note: 1. $t_{CS} + t_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol
Instruction register	3 bits	IR [2:0]
Bypass register	1 bit	BP
ID register	32 bits	ID [31:0]
Boundary scan register	109 bits	BS [109:1]

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Description	Notes
0	0	0	EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.	1, 2, 3
0	0	1	IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO balls in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.	
0	1	0	SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the RAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.	3, 4
0	1	1	RESERVED	The RESERVED instructions are not implemented but are reserved for future use. Do not use these instructions.	
1	0	0	SAMPLE (/PRELOAD)	When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO balls.	3
1	0	1	RESERVED		
1	1	0	RESERVED		
1	1	1	BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.	

Notes: 1. Data in output register is not guaranteed if EXTEST instruction is loaded.
2. After performing EXTEST, power-up conditions are required in order to return part to normal operation.
3. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.
4. Clock recovery initialization cycles are required to return from the SAMPLE-Z instruction.

ID Register

Part	Revision number (31:29)	Type number (28:12)	Vendor JEDEC code (11:1)	Start bit (0)
HM66AQB36102	000	00010011010100010	01000100011	1
HM66AQB18202	000	00010010010100010	01000100011	1
HM66AQB9402	000	00010000010100010	01000100011	1

Boundary Scan Order

Bit #	Ball ID	Signal names		
		×9	×18	×36
1	6R	$\overline{C}$	$\overline{C}$	$\overline{C}$
2	6P	C	C	C
3	6N	SA	SA	SA
4	7P	SA	SA	SA
5	7N	SA	SA	SA
6	7R	SA	SA	SA
7	8R	SA	SA	SA
8	8P	SA	SA	SA
9	9R	SA	SA	SA
10	11P	Q0	Q0	Q0
11	10P	D0	D0	D0
12	10N	NC	NC	D9
13	9P	NC	NC	Q9
14	10M	NC	Q1	Q1
15	11N	NC	D1	D1
16	9M	NC	NC	D10
17	9N	NC	NC	Q10
18	11L	Q1	Q2	Q2
19	11M	D1	D2	D2
20	9L	NC	NC	D11
21	10L	NC	NC	Q11
22	11K	NC	Q3	Q3
23	10K	NC	D3	D3
24	9J	NC	NC	D12
25	9K	NC	NC	Q12
26	10J	Q2	Q4	Q4
27	11J	D2	D4	D4
28	11H	ZQ	ZQ	ZQ
29	10G	NC	NC	D13
30	9G	NC	NC	Q13
31	11F	NC	Q5	Q5
32	11G	NC	D5	D5
33	9F	NC	NC	D14
34	10F	NC	NC	Q14
35	11E	Q3	Q6	Q6
36	10E	D3	D6	D6
37	10D	NC	NC	D15
38	9E	NC	NC	Q15
39	10C	NC	Q7	Q7
40	11D	NC	D7	D7
41	9C	NC	NC	D16
42	9D	NC	NC	Q16
43	11B	Q4	Q8	Q8
44	11C	D4	D8	D8
45	9B	NC	NC	D17

Bit #	Ball ID	Signal names		
		×9	×18	×36
46	10B	NC	NC	Q17
47	11A	CQ	CQ	CQ
48	10A	SA	NC	NC
49	9A	SA	SA	SA
50	8B	SA	SA	SA
51	7C	SA	SA	SA
52	6C	SA	SA	SA
53	8A	$\overline{R}$	$\overline{R}$	$\overline{R}$
54	7A	NC	NC	$\overline{BW1}$
55	7B	$\overline{BW}$	$\overline{BW0}$	$\overline{BW0}$
56	6B	K	K	K
57	6A	$\overline{K}$	$\overline{K}$	$\overline{K}$
58	5B	NC	NC	$\overline{BW3}$
59	5A	NC	$\overline{BW1}$	$\overline{BW2}$
60	4A	$\overline{W}$	$\overline{W}$	$\overline{W}$
61	5C	SA	SA	SA
62	4B	SA	SA	SA
63	3A	SA	SA	NC
64	2A	V_{SS}	V_{SS}	V_{SS}
65	1A	$\overline{CQ}$	$\overline{CQ}$	$\overline{CQ}$
66	2B	NC	Q9	Q18
67	3B	NC	D9	D18
68	1C	NC	NC	D27
69	1B	NC	NC	Q27
70	3D	NC	Q10	Q19
71	3C	NC	D10	D19
72	1D	NC	NC	D28
73	2C	NC	NC	Q28
74	3E	Q5	Q11	Q20
75	2D	D5	D11	D20
76	2E	NC	NC	D29
77	1E	NC	NC	Q29
78	2F	NC	Q12	Q21
79	3F	NC	D12	D21
80	1G	NC	NC	D30
81	1F	NC	NC	Q30
82	3G	Q6	Q13	Q22
83	2G	D6	D13	D22
84	1H	$\overline{DOFF}$	$\overline{DOFF}$	$\overline{DOFF}$
85	1J	NC	NC	D31
86	2J	NC	NC	Q31
87	3K	NC	Q14	Q23
88	3J	NC	D14	D23
89	2K	NC	NC	D32
90	1K	NC	NC	Q32

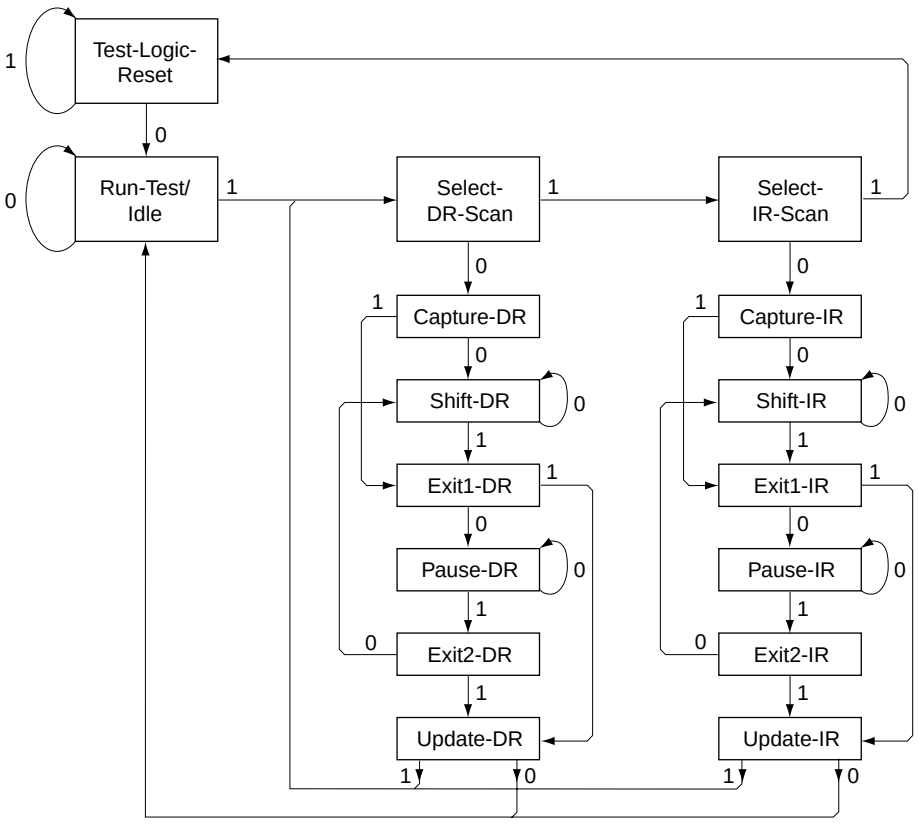
Bit #	Ball ID	Signal names		
		×9	×18	×36
91	2L	Q7	Q15	Q24
92	3L	D7	D15	D24
93	1M	NC	NC	D33
94	1L	NC	NC	Q33
95	3N	NC	Q16	Q25
96	3M	NC	D16	D25
97	1N	NC	NC	D34
98	2M	NC	NC	Q34
99	3P	Q8	Q17	Q26
100	2N	D8	D17	D26

Bit #	Ball ID	Signal names		
		×9	×18	×36
101	2P	NC	NC	D35
102	1P	NC	NC	Q35
103	3R	SA	SA	SA
104	4R	SA	SA	SA
105	4P	SA	SA	SA
106	5P	SA	SA	SA
107	5N	SA	SA	SA
108	5R	SA	SA	SA
109	—	INTER-NAL	INTER-NAL	INTER-NAL

Note: In boundary scan mode,

1. Clock balls (K / $\overline{K}$, C / $\overline{C}$) are referenced to each other and must be at opposite logic levels for reliable operation.
2. CQ and $\overline{CQ}$ data are synchronized to the respective C and $\overline{C}$ (except EXTEST, SAMPLE-Z).
3. If C and $\overline{C}$ tied high, CQ is generated with respect to K and $\overline{CQ}$ is generated with respect to $\overline{K}$ (except EXTEST, SAMPLE-Z).
4. ZQ must be driven to V_{DDQ} supply to ensure consistent results.

TAP Controller State Diagram

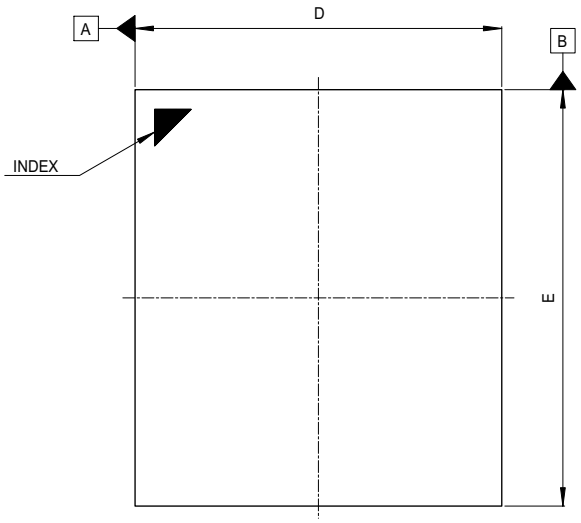


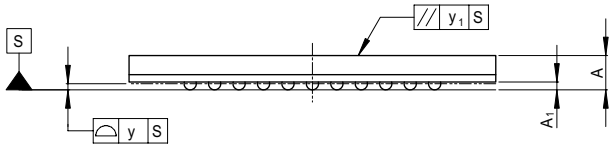
Notes: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

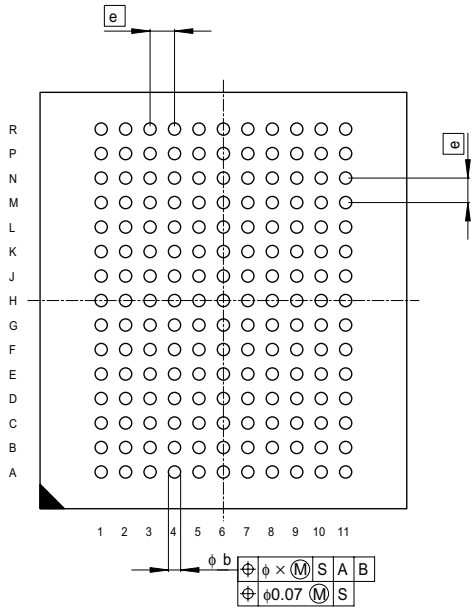
Package Dimensions

HM66AQB36102/18202/9402BP (PLBG0165FB-A / Previous Code: BP-165A)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LBGA165-15x17-1.00	PLBG0165FB-A	BP-165A	0.7g







Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	14.90	15.00	15.10
E	16.90	17.00	17.10
v	—	—	—
w	—	—	—
A	1.34	1.40	1.46
A_1	0.27	0.32	0.37
e	—	1.00	—
b	0.45	0.50	0.55
x	—	—	0.20
y	—	—	0.15
y_1	—	—	0.25
S_D	—	—	—
S_E	—	—	—
Z_D	—	—	—
Z_E	—	—	—

Revision History	HM66AQB36102/HM66AQB18202 HM66AQB9402 Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
0.0	Dec. 11, 2002	—	Initial issue
0.01	Mar.31.2004	—	Change format issued by Renesas Technology Corp.
		—	Deletion of cycle time 7.5 ns (133 MHz, BP-75)
		—	HM66AQB9402: Change of pin names D0 to D1 D1 to D2 D2 to D3 D3 to D4 D4 to D5 D5 to D6 D6 to D7 D7 to D8 D8 to D0 Q0 to Q1 Q1 to Q2 Q2 to Q3 Q3 to Q4 Q4 to Q5 Q5 to Q6 Q6 to Q7 Q7 to Q8 Q8 to Q0
		1	Change of Note
		4	Addition of Notes on Usage
		5-6	Pin Descriptions SAn to SA SA: Change of Descriptions $\overline{BW}$, $\overline{BWn}$: Change of Descriptions K, $\overline{K}$: Change of Descriptions C, $\overline{C}$: Change of Descriptions ZQ: Change of Descriptions D0 to Dn: Change of Descriptions Q0 to Qn: Change of Descriptions V_{REF}: Change of Descriptions NC: Change of Descriptions
		7-8	Block Diagram Change of the figures
		8	Truth Table D_A(A+0) to D(A+0) D_A(A+1) to D(A+1) Q_A(A+0) to Q(A+0) Q_A(A+1) to Q(A+1) Change of Notes6

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Mar.31.2004	9-10	Byte Write Truth Table 0 to L 1 to H
		11	Absolute Maximum Ratings V_{IN}, $V_{I/O}$, V_{DD}, V_{DDQ} (Notes4) Maximum value: 2.9 V to 2.5 V
		11	Recommended DC Operating Conditions Deletion of Notes2 Notes3 to Notes2 Change of Notes2 Addition of Notes3
		12	DC Characteristics (1st table) I_{DD} (Max): ×9, ×18: 600/490/415/340 mA to 740/620/550 mA ×36: 800/655/550/450 mA to 800/670/590 mA I_{SB1} (Max): ×9, ×18: 200/170/150/125 mA to 300/280/260 mA ×36: 210/180/160/135 mA to 300/280/260 mA I_{DD}, I_{SB1}: Addition of Notes Deletion of Notes3 Notes4 to Notes3 Addition of Notes4 Notes1-5 are moved to DC Characteristics (2nd table)
		12	DC Characteristics (2nd table) Deletion of I_{OH}, I_{OL} Deletion of Notes5-7, 10 Notes1-4 to Notes6-9 Notes8-9 to Notes10-11
		13	Capacitance Change of condition $C_{I/O}$: Change of Parameter Change of Notes2
		14	$V_{IH\ (AC)}$, $V_{IL\ (AC)}$: Addition of Notes4 Addition of Notes2 Notes2-3 to Notes3-4 Change of Notes3
		15	t_{KC} reset, t_{CQHQV}, t_{CQHQX}: Addition of Notes7 t_{CHQZ}, t_{CHQX1}: Change of Parameter
		16	Remarks1 to Notes7 Change of Notes7 Remarks2-5 to Remarks1-4 Addition of Remarks5
		17	Timing Waveforms Change of the figure Change of Notes3 Addition of Notes4
		19	TAP DC Operating Characteristics Addition of Notes4

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Mar.31.2004	21	TAP Controller Timing Diagram Change of the figure
		22-23	TAP Controller Instruction Set SAMPLE(-PRELOAD) to SAMPLE(/PRELOAD) EXTEST, SAMPLE-Z, RESERVED, SAMPLE(/PRELOAD): Change of Description Addition of Notes3-4
		23	ID Register Vendor JEDEC code: 00000000111 to 01000100011
		24-25	Boundary Scan Order Change of Note
		27	Package Dimensions Change of the figure of BP-165A
1.00	Jul.26.2006	—	Change format revised by Renesas Technology Corp.
		1	Ordering Information to Part No. Information
		1	Part No. Information Type No. to Catalogue Part No. Addition of Ordering Part No. Addition of the Renesas package code
		20	Package Dimensions Addition of the Renesas package code Changed to the Renesas format

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