100VG-AnyLAN Category 3/5 4-UTP Transceiver

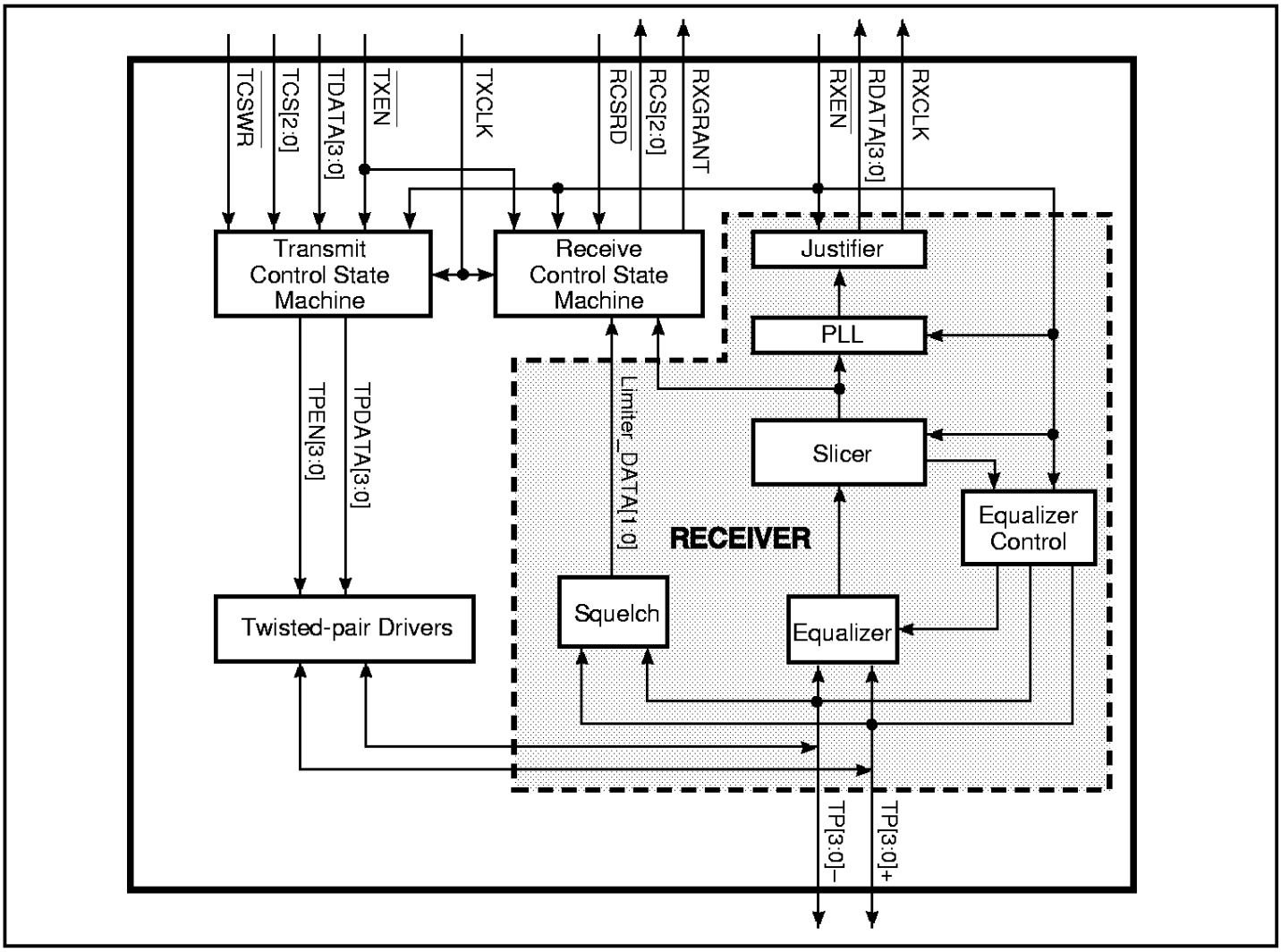
Product Features

- Complete PMD interface for 100VG-AnyLAN
- Supports Category 3/5 UTP cables
- 100 Mbps Transmission through 4 channels
- Adaptive equalization
- Digital PLLs
- Low Power
- IEEE 802.12 Standard compliant MII Interface
- Packages available:
  - 44-pin plastic PLCC (J44)

Product Description

The 100VG-AnyLAN Category 3/5 4-UTP Transceiver integrated circuit provides the complete physical layer (PMD) functions for 4-pair Category-3 or -5 unshielded twisted pair links as specified by the IEEE 802.12 standard. The device enables 100VG-AnyLAN adapter and hub implementations by providing a standard Media Independent Interface (MII) that can connect to either hub or MAC implementations with no additional glue logic. The four differential twisted pair drivers connect directly to commonly available 802.12 4-UTP filter-transformer modules. The device supports 100Mbps transmission over twisted-pair lengths from 0 to 100 meters on Category-3 cable, and longer lengths on Category-5 cable.

Figure 1. Logic Block Diagram



During packet reception, the device provides all timing and data recovery functions for the four incoming data streams and justifies the received data streams from the four independent twisted-pairs to a common received clock. Control signals received on twisted pairs 0 and 1 are decoded by the receive control machine to provide line state information at the MII interface. The receive data path includes a first order linear equalizer and timing recovery circuits for each of the four twisted pairs.

Transmit control signals are generated by the device on twisted pairs 2 and 3 based on the requested transmit control state presented at the MII. During packet transmission all four twisted pairs are driven with the transmit data received from the MII.

Figure 2. Pin Configuration

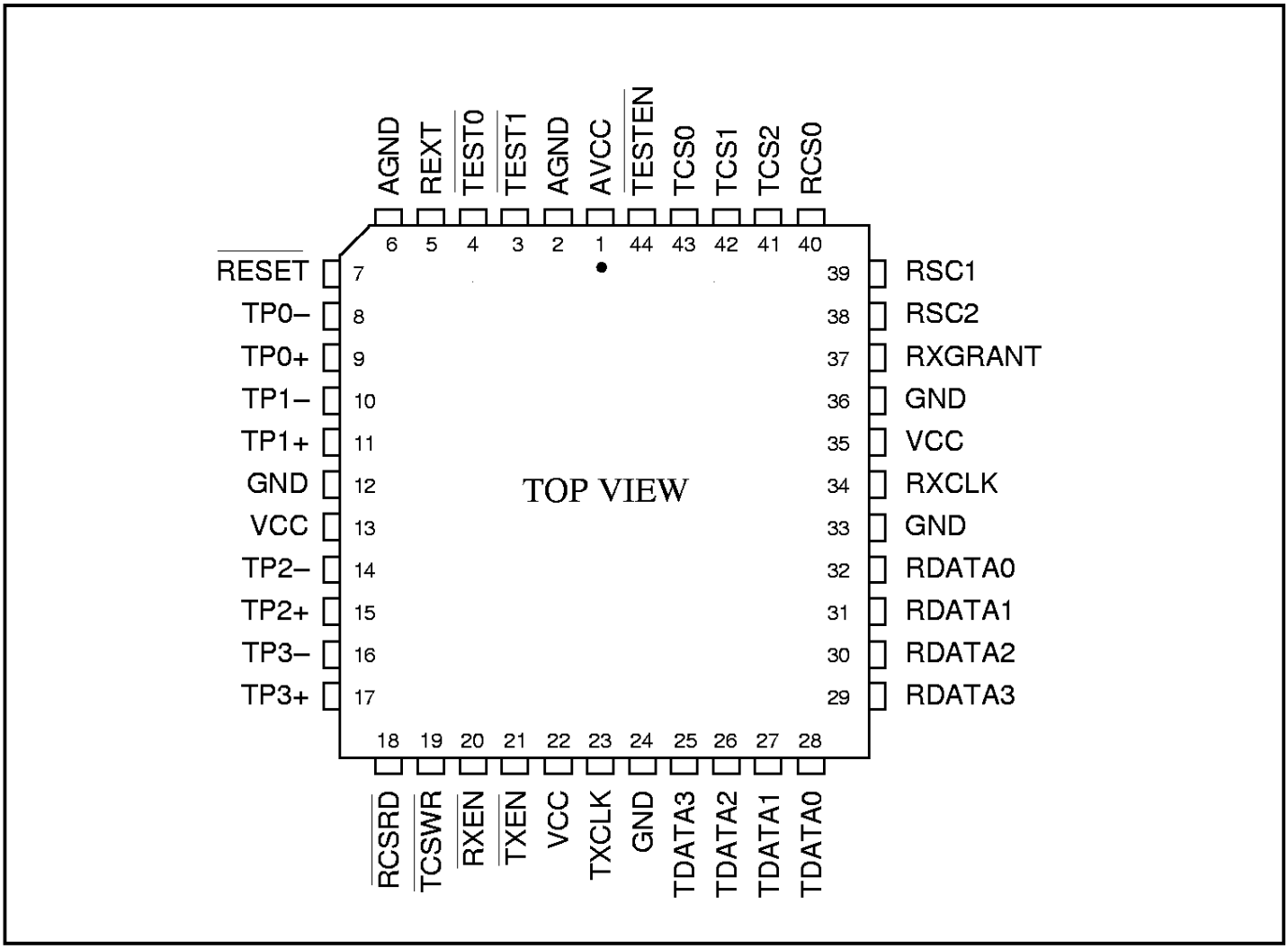


Table 1. Pin Description

Pin No.	Signal	I/O	Description
1	AVCC	—	Analog Vcc.
2	AGND	—	Analog Ground.
3	$\overline{\text{TEST1}}$	I	Test pin (Active LOW). Reserved
4	$\overline{\text{TEST0}}$	I	Test pin (Active LOW). Reserved
5	REXT	—	**R External**. (24.9KΩ ±1%).This pin is used to attach an external precision resistor used as a current reference.
6	AGND	—	Analog Ground.
7	$\overline{\text{RESET}}$	I	**Reset.** (Active LOW) When asserted causes a reset of all internal state machines, counters and logic. $\overline{\text{RESET}}$ must be asserted for a minimum of 20 microseconds.
8, 9	TP0–, TP0+	I/O	**Twisted Pair Zero Input/Output ±.** TP0+, TP0– is a differential pair of twisted-pair drivers.
10, 11	TP1–, TP1+	I/O	**Twisted Pair One Input/Output ±.** TP1+, TP1– is a differential pair of twisted-pair drivers.
12	GND	—	Twisted Pair I/O Ground
13	VCC	—	Twisted Pair I/O Vcc
14, 15	TP2–, TP2+	I/O	**Twisted Pair Two Input/Output ±.** TP2+, TP2– is a differential pair of twisted-pair drivers.
16, 17	TP3–, TP3+	I/O	**Twisted Pair Three Input/Output ±.** TP3+, TP3– is a differential pair of twisted-pair drivers.
18	$\overline{\text{RCSRD}}$	I	**Receive Control Read Enable.** (Active LOW) When $\overline{\text{RCSRD}}$ is asserted LOW, the device drives the RXGRANT and RCS[2:0] outputs. When $\overline{\text{RCSRD}}$ is deasserted, RXGRANT and RCS[2:0] are tri-stated.
19	$\overline{\text{TCSWR}}$	I	**Transmit Control Code Write Enable.** (Active LOW) This signal must be asserted LOW to enable the Transmit Control Machine to sample TCS[2:0]. $\overline{\text{TCSWR}}$ is synchronous with TXCLK.
20	$\overline{\text{RXEN}}$	I	**Receive Enable.** (Active LOW) When $\overline{\text{RXEN}}$ is asserted, the device is enabled to receive packet data from the TP[3:0] inputs. When $\overline{\text{RXEN}}$ is deasserted, RXCLK and RDATA[3:0] are tri-stated. When $\overline{\text{RXEN}}$ is asserted and preamble is detected, RXCLK begins to transition, at which time the RDATA[3:0] outputs are active and valid. When $\overline{\text{RXEN}}$ is asserted, the four twisted pair drivers are disabled. (The transmitters on TP2 and TP3 are disabled after DC balance has been achieved.)
21	$\overline{\text{TXEN}}$	I	**Transmit Enable.** (Active LOW) When $\overline{\text{TXEN}}$ is asserted, the device transmits data on the TDATA[3:0] inputs to the TP[3:0] outputs once a DC balance point has been reached on the twisted pairs. When $\overline{\text{TXEN}}$ is deasserted, control codes encoded by TCS[2:0] are transmitted. $\overline{\text{TXEN}}$ is synchronous to TXCLK.
22	VCC	—	Digital Vcc.
23	TXCLK	I	**Transmit Clock.** 30 MHz ±100ppm with 45%-55% duty cycle. TCS[2:0], $\overline{\text{TCSWR}}$, $\overline{\text{TXEN}}$, TDATA[3:0], RCS[2:0], $\overline{\text{RCSRD}}$, RXEN, and RXGRANT are synchronous to TXCLK.
24	GND	—	Digital Ground.

Note: I = Input, O = Output, Z = Tristate, — = N/A

Table 1: Pin Description *(continued)*

Pin No.	Signal	Type	Description
25-28	TDATA[3:0]	I	**Transmit Data.** A 4-bit unidirectional serial transmit bus. Data presented on these inputs are transmitted onto TP[3:0] when $\overline{\text{TXEN}}$ is asserted LOW. TDATA[3:0] inputs are synchronized to the rising edge of TXCLK. Data on TDATA3 is transmitted on TP0. Data on TDATA2 is transmitted on TP1. Data on TDATA1 is transmitted on TP2. Data on TDATA0 is transmitted on TP3.
29-32	RDATA[3:0]	O/Z	**Receive Data.** A 4-bit unidirectional serial receive bus that contains valid receive data when $\overline{\text{RXEN}}$ is asserted and a packet is being received from the medium. RDATA3 contains data present on TP3, RDATA2 contains data present on TP2, RDATA1 contains data present on TP1 and RDATA0 contains data present on TP0. RDATA[3:0] are synchronous to RXCLK. Upon $\overline{\text{RXEN}}$ deassertion, RDATA[3:0] is immediately tristated. When $\overline{\text{RXEN}}$ is asserted, RDATA[3:0] is driven low until RXCLK is active, at which point valid preamble is on RDATA[3:0].
33	GND	—	CMOS Output Ground.
34	RXCLK	O/Z	**Receive Clock.** Recovered 30 MHz clock from the data on the twisted pairs. RXCLK is synchronous with the RDATA[3:0] outputs. It is active only when $\overline{\text{RXEN}}$ has been asserted LOW and the device has acquired phase and frequency lock from the incoming data. At the time RXCLK becomes active, valid preamble is presented on the RDATA[3:0] outputs. RXCLK will continue to be active as long as $\overline{\text{RXEN}}$ is asserted.
35	VCC	—	CMOS Output Vcc.
36	GND	—	Digital Ground.
37	RXGRANT	O/Z	**Receive Grant.** When RXGRANT is asserted, the device has determined that the GRANT code has been transmitted by the upstream node. When RXGRANT is deasserted, another control code is being received. RXGRANT is synchronous with TXCLK. It is tri-stated if $\overline{\text{RCSRD}}$ is deasserted.
38-40	RCS[2:0]	O/Z	**Receive Control Code.** RCS[2:0] are the encoded values of the control codes received from the medium on TP[1:0]. The signals are valid when $\overline{\text{RCSRD}}$ is asserted and are synchronous to TXCLK. When $\overline{\text{RCSRD}}$ is deasserted, these signals are tri-stated.
41-43	TCS[2:0]	I	**Transmit Control Code.** The 3-bit encoded value of the transmit control code. The TCS is processed and transmitted onto pairs TP[3:2] by the device. The values on these three inputs will be sampled only when $\overline{\text{TCSWR}}$ is asserted. TCS[2:0] may be changed when $\overline{\text{TXEN}}$ is asserted, but will not take effect until $\overline{\text{TXEN}}$ has been deasserted.
44	$\overline{\text{TESTEN}}$	I	**Test Enable Pin.** (Active LOW) When $\overline{\text{RESET}}$ is deasserted and $\overline{\text{TESTEN}}$ is asserted, the chip-to-board contact test is enabled. See Table 2 for detailed pin mapping during the contact test.

Table 2: Pin Mapping for Chip-to-Board Contact Test ($\overline{RESET}$ = 1, TESTEN = 0)

INPUT`	$\overline{TEST1}$	$\overline{TEST0}$	TCS[2:0]	TDATA[3:0]	$\overline{RCSRD}$	$\overline{TCSWR}$	$\overline{RXEN}$	$\overline{TXEN}$	TXCLK
OUTPUT	REXT	RXGRANT	RCS[2:0]	RDATA[3:0]	TP0+/TP0–	TP1+/TP1–	TP2+/TP2–	TP3+/TP3–	RXCLK

Note: When $\overline{RESET}$ is asserted, the contact test is disabled. This is used to check the contact for the $\overline{RESET}$ pin.

Functional Description

Twisted-Pair Drivers

The four twisted-pair drivers provide a differential output impedance of 50 Ohms from their respective twisted-pair pins. These drivers are tristated during reception and driven during transmission. The twisted-pair drivers transmit NRZ data, i.e., a value of 1 is indicated by a positive differential voltage and a value of 0 is indicated by a negative differential voltage.

Receiver

The receiver consists of four sets of switchable first order linear equalizers followed by slicers, which determine the voltage level (1 or 0) on each of the twisted pair differential signals. Following the assertion of $\overline{RXEN}$, the timing recovery circuits are engaged to detect packet preamble and create a receive clock for each of the four data channels. Each channel's receive clock and sampled data is provided to the justifier circuit, which retimes the received data to the output RXCLK. During periods of packet reception, data on all four twisted-pairs is passed through the equalizer circuits, if they are enabled. The decision to enable an equalizer will be based on the amplitude of the preamble sequence of the previous packet.

When packet data is expected, the receiver will also perform a signal detect function, which is an indication that TP[3:0] may have incoming preamble. (This is distinguished from control codes). Timing and data recovery is performed on all four twisted pairs independently and the resulting four clocks are justified to a single RXCLK recovered from TP0. Data and timing recovery continues until $\overline{RXEN}$ is deasserted at the MII interface. If valid data bits are not incoming while $\overline{RXEN}$ is asserted, RXCLK may drift.

Control State Machine

Two control tone signals, CS1 and CS2, are generated and transmitted on twisted pair wires for Receive Control State Machine (RCSM) and Transmit Control State Machine (TCSM) interpretation. CS1 is a continuous repetition of 16 "1's" followed by 16 "0's" transmitted at 30 Mbaud, and CS2 is continuous repetition of 8 "1's" followed by 8 "0's" transmitted at 30 MBaud. The fundamental frequency of CS1 is 0.9375 MHz, and that of CS2 is 1.875 MHz.

Transmit Control State Machine

The TCSM has two major functions: the generation of control signals and their subsequent transmission, and the transmission of data present on the TDATA[3:0] inputs. The transmit control machine encodes the 3-bit value of TCS[2:0] for transmission onto TP[3:2] when $\overline{TXEN}$ is deasserted and provides the proper termination control codes prior to transmitting serial data on TP[3:0] when $\overline{TXEN}$ is asserted. NRZ coding is used to transmit both data and control codes. The transmit control machine must also monitor $\overline{RXEN}$ in order to disable control signal transmissions on TP[1:0] during packet reception.

Data on TDATA[3:0] shall be transmitted synchronously with TXCLK onto TP[3:0] when $\overline{TXEN}$ is asserted and a DC balance point has been reached. A DC balance point is defined as an equal number of 1's and 0's having been transmitted on both TP3 and TP2. When both $\overline{TXEN}$ and $\overline{RXEN}$ are deasserted, TCS disables the transmitters on channels 0 and 1, and generates the following control signals on channels 2 and 3 based on the values of TCS[2:0] as shown in table 3.

Table 3. TCS - TP Mapping

TCS[2:0]	TP2	TP3
000	Disable	Disable
001	CS1	CS1
010	CS1	CS2
011	CS2	CS1
100	CS2	CS2
101	—	—
110	—	—
111	Disable	Disable

When $\overline{\text{TXEN}}$ is asserted, the TCS continues to transmit control signals on TP2 and TP3 until an equal number of 0's and 1's (DC balance) on both channels have been transmitted. At that point, the TCS then begins to transmit data from TDATA[3:0] onto all four twisted pairs according to Table 4.

Table 4. TDATA to TP Mapping

Input	Output
TDATA0	TP3
TDATA1	TP2
TDATA2	TP1
TDATA3	TP0

Receive Control State Machine

The Receive Control State Machine (RCSM) is responsible for recovering received control signals from TP1 and TP0 via LIMITER_DATA[1:0], and determining the receive control state for indication on RCS[2:0] and RXGRANT. Control signals are interpreted mainly during periods when packets are not being received. During times of packet reception and transmission, the RCSM is mainly inactive, though signal monitoring functions are performed during packet reception. Table 5 illustrates the mapping from the twisted pair signals to the RDATA signals during packet reception.

Table 5. TP to RDATA Mapping

Input	Output
TP0	RDATA0
TP1	RDATA1
TP2	RDATA2
TP3	RDATA3

RXGRANT is asserted by the RCSM when the lack of energy or SILENCE is detected on TP0 and TP1. It is deasserted otherwise. The signal level measurement function is performed by the squelch circuits on TP0 and TP1. The relationship between TP0 and TP1 with the received control state is given in Table 6.

Table 6. TP0/1 Mapping TO RCS

TP0	TP1	RCS[2:0]
Mode Transition	Mode Transition	000
CS1	CS1	001
CS2	CS1	010
CS1	CS2	011
CS2	CS2	100
Data	Data	101
—	—	110
Link Warning	Link Warning	111

MAXIMUM RATINGS

(Above which the useful life may be impaired. For user guidelines, not tested.)

Maximum Supply Voltage (Vcc)	7.0V
Storage Temperature (Ts)	–55°C to +125°C
Ambient Temperature with Power Applied (TA)	0°C to +70°C
Signal Pin Voltage	–0.5 to Vcc+0.5V

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7. DC Electrical Characteristics (Over the Operating Range)

Description		Min.	Typ.	Max.	Units
Supply Voltage		4.75	5.0	5.25	V
Supply Current	Idle	—	46	—	mA
	Transmit Tone	—	130	—	mA
	Transmit Data	—	198	—	mA
	Receive Data	—	132	—	mA

Table 8. Twisted Pair Output Specifications (See Figure 6)

Description	Min.	Typ.	Max.	Units
Differential Source Resistance	40	50	60	Ω
Rise/Fall Time with 150Ω/20pF Load, 10% to 90%	6.0	—	12.0	ns
Output Voltage with 150Ω Load	3.4	3.8	4.2	V
Differential Pair Skew	—	—	1.0	ns

Table 9. Twisted Pair Input Specifications

Description	Min.	Typ.	Max.	Units
Differential Input Resistance	35	50	65	Ω
Differential Input Capacitance	—	15	20	pF

Table 10. CMOS Input

Description	Condition	Min.	Typ.	Max.	Units
V_{IH}		Vcc – 1	—	—	V
V_{IL}		—	—	1.0	V
Input Leakage		—	—	10	µA
Input Capacitance		—	—	6	pF
Input Rise/Fall Time	20%-80%	—	—	5	ns

Table 11. CMOS Output

Description	Condition	Min.	Typ.	Max.	Units
V_{OH}	Sourcing 2 mA	V_{CC} – 0.5	—	—	V
V_{OL}	Sinking 2 mA	—	—	0.5	V
Ouput Leakage Current	High-Impedance State	—	—	10	µA
Output Rise/Fall Time	See Figure 3	1	—	6	ns

Figure 3. MII Output Driver Test Condition

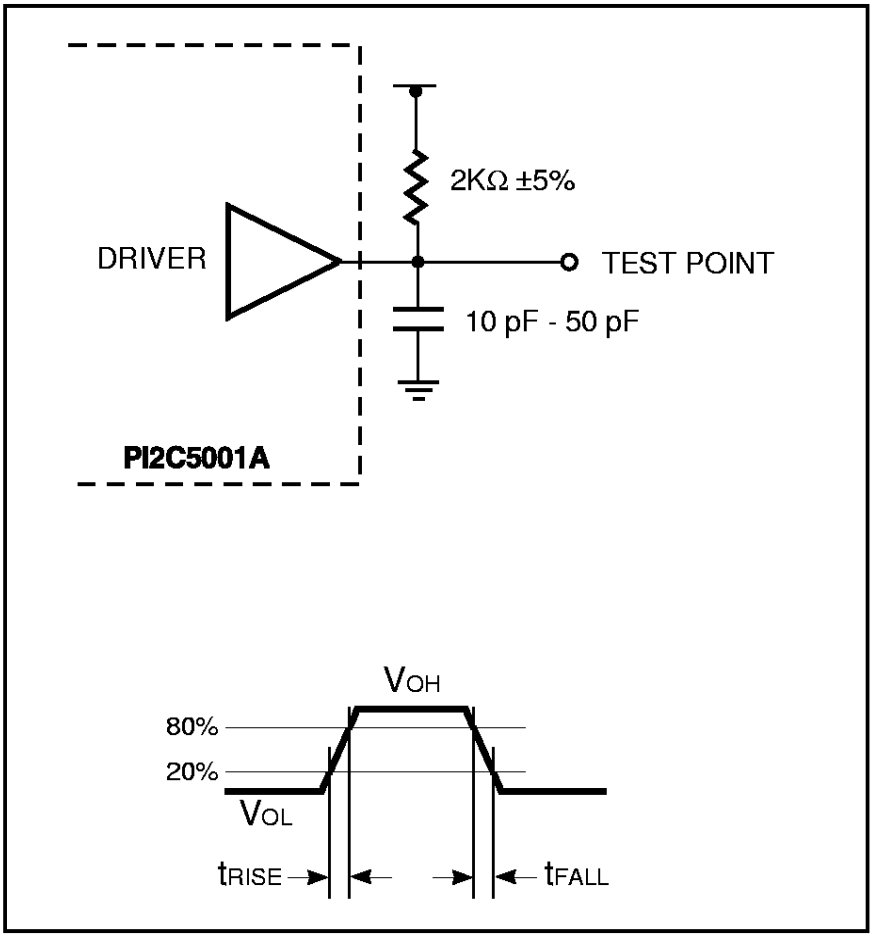
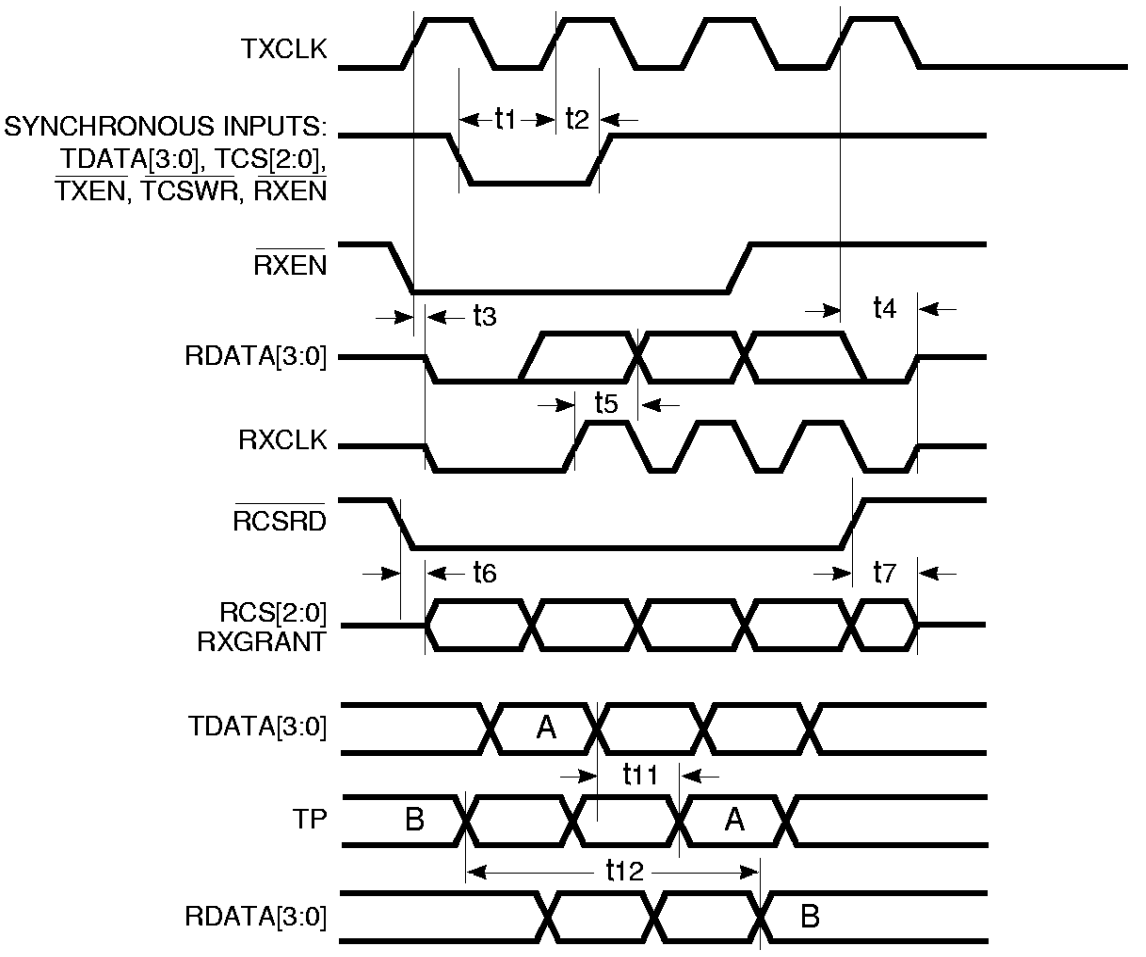


Table 12. Timing Specifications (BT = Bit Times) (See Figure 4)

Symbol	Parameter	Description	Min.	Typ.	Max.	Units
t1	t_{SETUP}	Synchronous Input Setup Time to Rising Edge of TXCLK for TDATA[3:0], TCS[2:0], $\overline{TXEN}$, $\overline{TCSWR}$, $\overline{RXEN}$	7	—	—	ns
t2	t_{HOLD}	Synchronous Input Hold Time to Rising Edge of TXCLK for TDATA[3:0]. TCS[2:0], $\overline{TXEN}$, $\overline{TCSWR}$, $\overline{RXEN}$	2	—	—	ns
t3	t_{RXEN}	Time from TXCLK ($\overline{RXEN}$ Asserted) to RXCLK and RDATA[3:0] Driven	—	—	15	ns
t4	t_{RXDIS}	Time from TXCLK ($\overline{RXEN}$ Deasserted) to RXCLK and RDATA[3:0] Tri-stated	—	—	15	ns
t5	t_{RDV}	RDATA Valid after RXCLK Rising Edge	3	—	20	ns
t6	t_{RCSEN}	$\overline{RCSRD}$ Asserted to RCS[2:0] and RXGRANT Valid	—	—	15	ns
t7	t_{RCSDIS}	$\overline{RCSRD}$ Deasserted to RCS[2:0] and RXGRANT Tri-stated	—	—	15	ns
t8	t_{RXPRE}	$\overline{RXEN}$ Asserted to Start of Preamble for Valid Packet Reception	6	—	—	BT
t9	t_{PRERD}	Time from Preamble to RDATA, RXCLK Valid	—	—	20	BT
t10	t_{RXMIN}	Minimum Time for $\overline{RXEN}$ must be deasserted so that DC balance can be achieved for TCS requirement	16	—	—	BT
t11	t_{DTP}	TDATA to TP	33	—	167	ns
t12	t_{PRD}	TP to RDATA	65	—	235	ns
—	t_{SKEW}	Timing Skew Between TP Inputs During Start of Preamble	—	—	2	BT
—	—	RXCLK Duty Cycle	40	—	60	%
—	t_{RXJ}	RXCLK Cycle-to-cycle Jitter	—	—	±2.0	ns
—	t_{TXPJ}	TXCLK Peak-to-peak Jitter	—	—	1.0	ns

Figure 4. Timing Characteristics



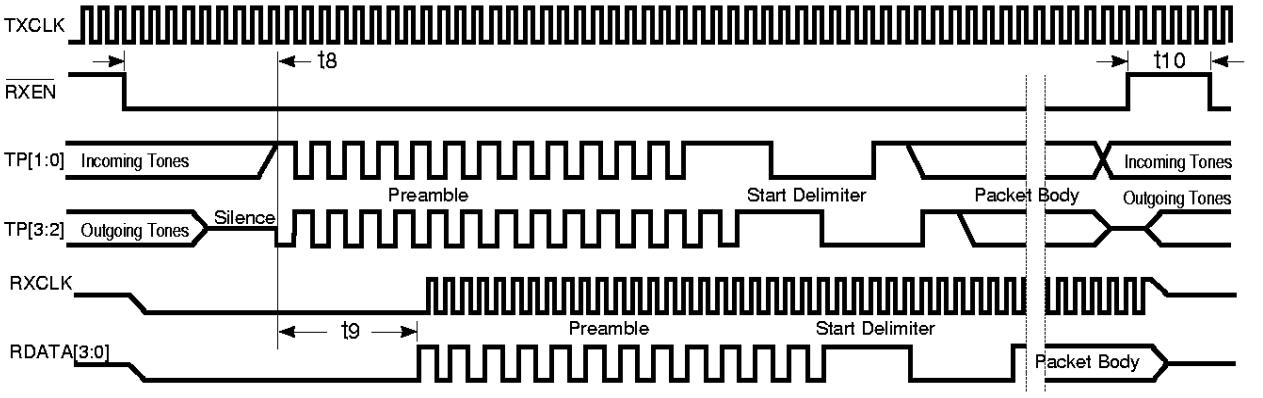


Figure 5. Silence Thresholds

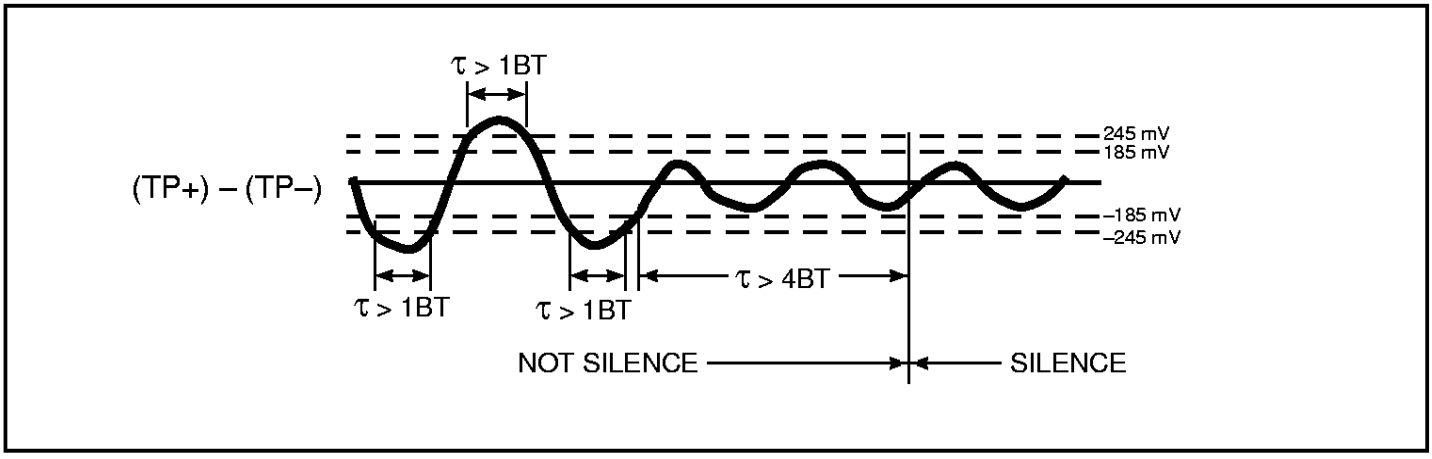


Figure 6. TP Output Data Test Load

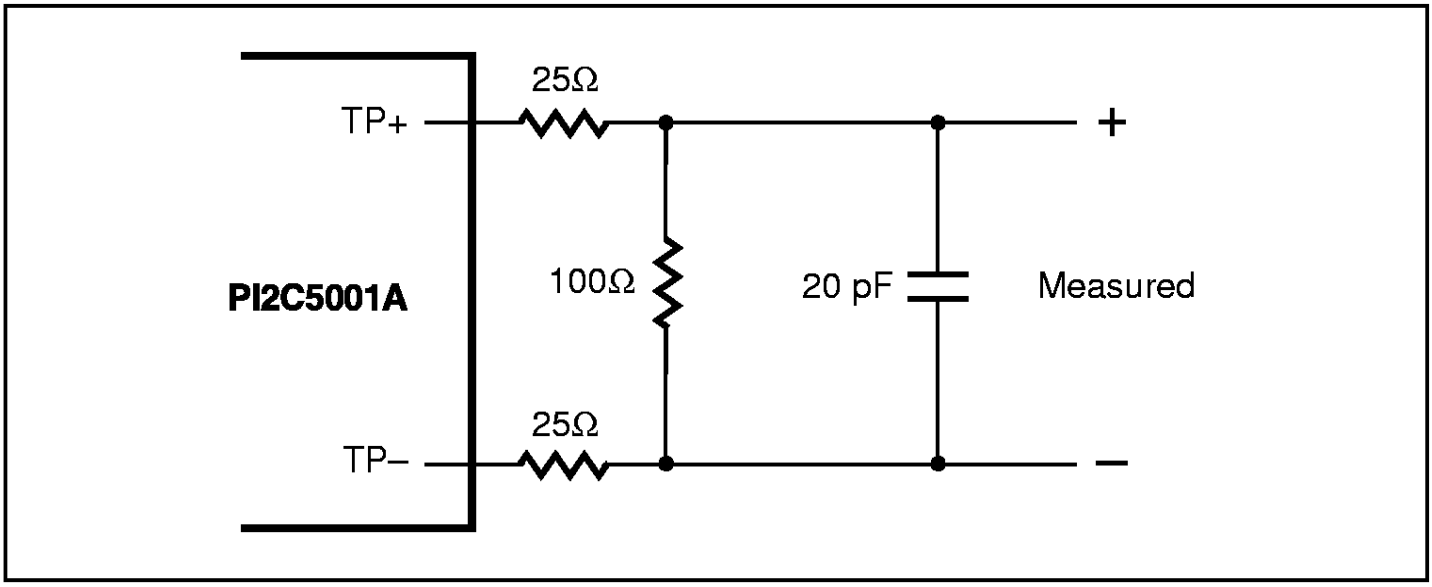


Figure 7. Typical Application Configuration

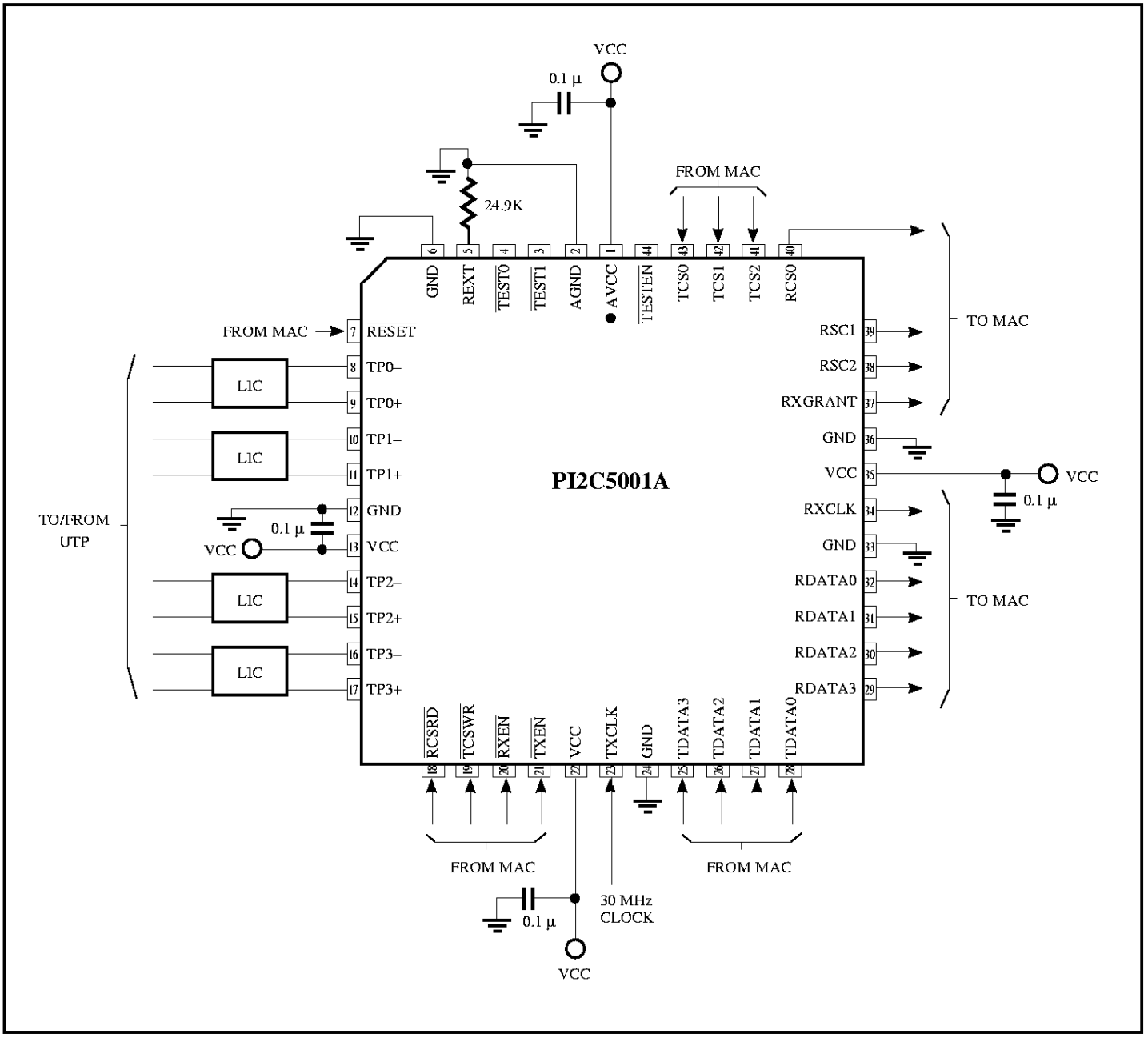
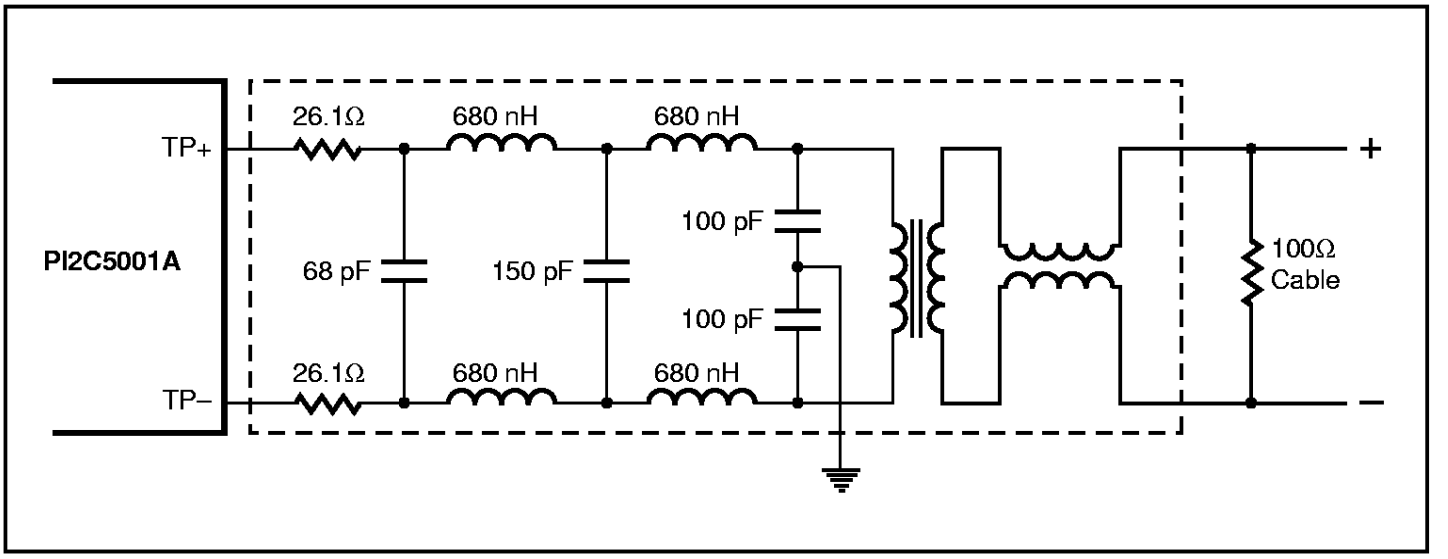


Figure 8. Line Interface Circuit (LIC)



Package Information

J-44 — 44-Pin PLCC (680 x 680)