Am93L28

Low-Power Dual 8-Bit Shift Register

Distinctive Characteristics

- 80 mW typical power dissipation
- 16 MHz typical shift frequency
- 100% reliability assurance testing in compliance with MIL STD 883
- Guaranteed fan-out of three with standard TTL circuits

FUNCTIONAL DESCRIPTION

The Am93L28 low-power dual 8-bit shift register provides 16 bits of high-speed serial storage in two identical shift registers, each consisting of 8 master slave RS flip-flops.

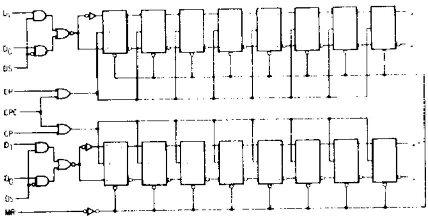
Data to each register is selected from one of two sources, D_0 and D_1, by a two input multiplexer controlled by DS (data select). When DS is HIGH, data is entered from the D_1 input; when DS is LOW data is entered from the D_0 input.

The two shift registers have separate clock inputs and a common clock input. The common clock is OR'ed with the separate clock inputs, so that for each register one clock input can be used as a clock line and the other as an active LOW shift enable. The registers can then be operated with a common clock and independent shift enables or with independent clocks and a common shift enable.

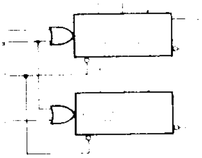
Data is entered into the masters of the flip-flops while the clock is LOW. During the clock pulse LOW-to-HIGH transition the masters are inhibited from further change, and the data is transferred to the slaves. As long as the clock is HIGH, the masters cannot change and the slaves are connected to the masters. When the clock goes from HIGH to LOW, the slaves are inhibited from changing and new data is entered into the masters.

An asynchronous active LOW master reset ($\overline{MR}$) resets all 16 bits of shift register to the "0" state independent of any other inputs to the device.

LOGIC DIAGRAM



LOGIC SYMBOL



LOADING RULES

In Unit Loads (Notes)

Input Load Factor	TTL LOADS HIGH	TTL LOADS LOW	93L LOADS HIGH	93L LOADS LOW
$\overline{MR}$, D_0, D_1	0.5	0.25	1.0	1.0
Separate CP (Pin 7 & 10)	0.75	0.375	1.5	1.5
D_S	1.0	0.5	2.0	2.0
Common CP (Pin 2)	1.5	0.75	3.0	3.0
Output Drive	**HIGH**	**LOW**	**HIGH**	**LOW**
Q_7, $\overline{Q}_7$	8	3	16	12

NOTES:
1) A TTL unit load is specified as 0.4 V at −1.6 mA LOW, 2.4 V at 40 μA HIGH.
2) A 93L unit load is specified as 0.3 V at −400 μA LOW, 2.4 V at 20 μA HIGH.
3) Enough output LOW current is available to mix TTL and 93L loads and still meet the 93L requirement of a V_{OL} of 0.3 V.

Am93L28 ORDERING INFORMATION

Package Type	Temperature Range	Order Number
16-pin Molded DIP	0°C to +75°C	U6M93L2859X
16-pin Hermetic DIP	0°C to +75°C	U7B93L2859X
16-pin Hermetic DIP	−55°C to +125°C	U7B93L2851X
16-pin Hermetic Flat Pak	−55°C to +125°C	U4L93L2851X
Dice	Note	UXX93L28XXD

Note: The dice supplied will contain units which meet both 0°C to +75°C and −55°C to +125°C temperature ranges.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V max
DC Input Voltage	−0.5 V to +5.5 V
Output Current, Into Outputs	30 mA
DC Input Current (Note 1)	−30 mA to +5.0 mA

Note 1. Maximum current defined by DC input voltage

ELECTRICA[illegible]RACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am93L2859X T_A [illegible] 0 +75°C V_{CC} = 4.75 V to 5.25 V
Am93L2851X T_A = −55°C to +125°C V_{CC} = 4.50 V to 5.50 V

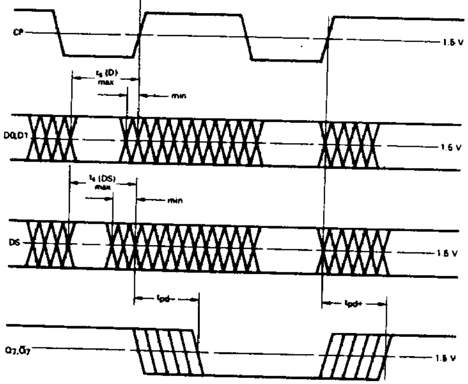
Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL}	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 4.92 mA V_{IN} = V_{IH} or V_{IL}		0.15	0.3	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.7	Volts
I_{IL} (Note 2)	93L Unit Load, Input LOW Current	V_{CC} = MAX., V_{IN} = 0.3 V		−0.25	−0.4	mA
I_{IH} (Note 2)	93L Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4 V		2.0	20	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5 V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−2.5	−16	−25	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		16	25.3	mA

Notes: 1) Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
2) Actual input currents are obtained by multiplying unit load current by the 93L input load factor. (see loading rules)

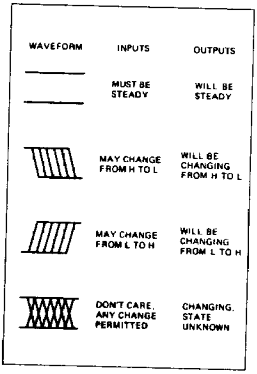
SWITCHING CHARACTERISTICS (T_A = 25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{pd+} t_{pd-}	Turn Off Delay (Q_7, $\overline{Q}_7$) Turn On Delay (Q_7, $\overline{Q}_7$)	V_{CC} = 5.0 V C_L = 15 pF		20 43	45 80	ns ns
$t_{pd-}(\overline{MR})$	Turn On Delay ($\overline{MR}$ to Q_7)			50	110	ns
CP_{pw}	Min. Clock LOW Pulse Width			30	55	ns
$\overline{MR}_{pw}$(CPH)	Min. Reset Pulse Width with CP HIGH			28	60	ns
$\overline{MR}_{pw}$(CPL)	Min. Reset Pulse Width with CP LOW			38	70	ns
t_s (D_0, D_1)	Data Set-up Time		0		30	ns
t_s (DS)	Set-up Time, Select Input		−1		30	ns
f_s	Shift Frequency		10	16		MHz

SWITCHING TIME WAVEFORMS



KEY TO TIMING DIAGRAM



Note: The "set-up Time" is defined as the time required, relative to the clock, for a LOW to HIGH edge (tsH) or a HIGH to LOW edge (tsL) to propagate through internal delays. Logic transitions occurring before ts max are guaranteed to be detected; those occurring after ts min are guaranteed not to be detected. Transitions between ts max and ts min may or may not be detected. The minimum set up time for a LOW is sometimes called the "release time" for a HIGH.

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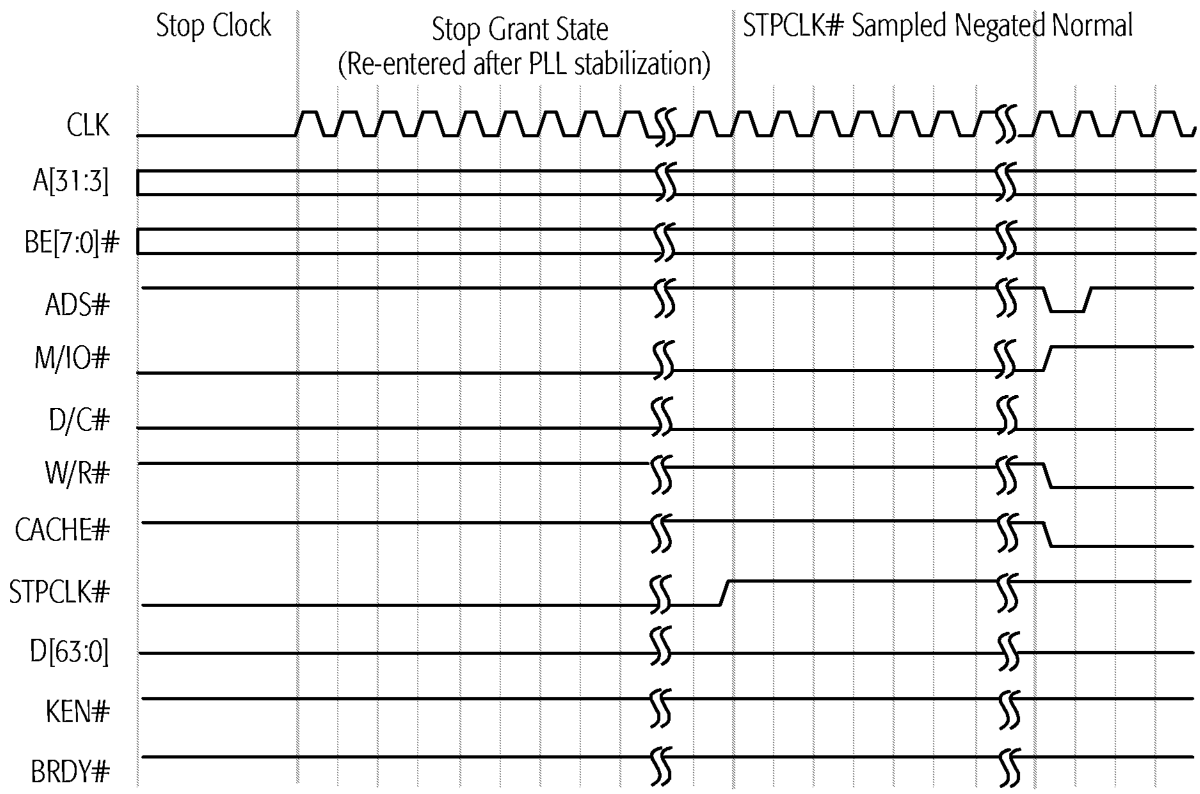

Figure 75. Stop Grant and Stop Clock Modes, Part 2

INIT-Initiated Transition from Protected Mode to Real Mode

INIT is typically asserted in response to a BIOS interrupt that writes to an I/O port. This interrupt is often in response to a Ctrl-Alt-Del keyboard input. The BIOS writes to a port (similar to port 64h in the keyboard controller) that asserts INIT. INIT is also used to support 80286 software that must return to Real mode after accessing extended memory in Protected mode.

The assertion of INIT causes the processor to empty its pipelines, initialize most of its internal state, and branch to address FFFF_FFF0h—the same instruction execution starting point used after RESET. Unlike RESET, the processor preserves the contents of its caches, the floating-point state, the MMX state, Model-Specific Registers (MSRs), the CD and NW bits of the CR0 register, the time stamp counter, and other specific internal resources.

Figure 76 shows an example in which the operating system writes to an I/O port, causing the system logic to assert INIT. The sampling of INIT asserted starts an extended microcode sequence that terminates with a code fetch from FFFF_FFF0h, the reset location. INIT is sampled on every clock edge but is not recognized until the next instruction boundary. During an I/O write cycle, it must be sampled asserted a minimum of three clock edges before BRDY# is sampled asserted if it is to be recognized on the boundary between the I/O write instruction and the following instruction. If INIT is asserted synchronously, it can be asserted for a minimum of one clock. If it is asserted asynchronously, it must have been negated for a minimum of two clocks, followed by an assertion of a minimum of two clocks.

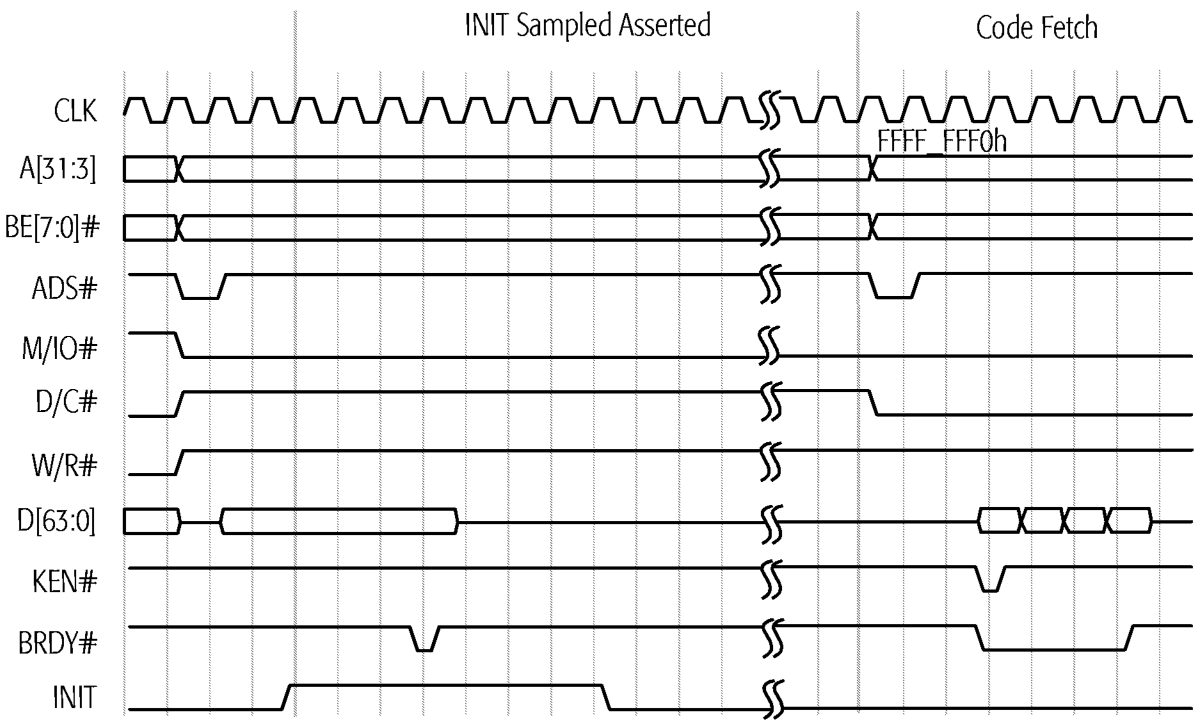

Figure 76. INIT-Initiated Transition from Protected Mode to Real Mode

6 Power-on Configuration and Initialization

On power-on the system logic must reset the AMD-K6-2 processor by asserting the RESET signal. When the processor samples RESET asserted, it immediately flushes and initializes all internal resources and its internal state, including its pipelines and caches, the floating-point state, the MMX and 3DNow! states, and all registers. Then the processor jumps to address FFFF_FFF0h to start instruction execution.

6.1 Signals Sampled During the Falling Transition of RESET

FLUSH# FLUSH# is sampled on the falling transition of RESET to determine if the processor begins normal instruction execution or enters Tri-State Test mode. If FLUSH# is High during the falling transition of RESET, the processor unconditionally runs its Built-In Self Test (BIST), performs the normal reset functions, then jumps to address FFFF_FFF0h to start instruction execution. (See "Built-In Self-Test (BIST)" on page 217 for more details.) If FLUSH# is Low during the falling transition of RESET, the processor enters Tri-State Test mode. (See "Tri-State Test Mode" on page 218 and "FLUSH# (Cache Flush)" on page 103 for more details.)

BF[2:0] The internal operating frequency of the processor is determined by the state of the bus frequency signals BF[2:0] when they are sampled during the falling transition of RESET. The frequency of the CLK input signal is multiplied internally by a ratio defined by BF[2:0]. (See "BF[2:0] (Bus Frequency)" on page 92 for the processor-clock to bus-clock ratios.)

BRDYC# BRDYC# is sampled on the falling transition of RESET to configure the drive strength of A[20:3], ADS#, HITM#, and W/R#. If BRDYC# is Low during the fall of RESET, these outputs are configured using higher drive strengths than the standard strength. If BRDYC# is High during the fall of RESET, the standard strength is selected. (See "BRDYC# (Burst Ready Copy)" on page 95 for more details.)

6.2 RESET Requirements

During the initial power-on reset of the processor, RESET must remain asserted for a minimum of 1.0 ms after CLK and V_{CC} reach specification. (See “CLK Switching Characteristics” on page 255 for clock specifications. See “Electrical Data” on page 247 for V_{CC} specifications.)

During a warm reset while CLK and V_{CC} are within specification, RESET must remain asserted for a minimum of 15 clocks prior to its negation.

6.3 State of Processor After RESET

Output Signals

Table 31 shows the state of all processor outputs and bidirectional signals immediately after RESET is sampled asserted.

Table 31. Output Signal State After RESET

Signal	State	Signal	State
A[31:3], AP	Floating	LOCK#	High
ADS#, ADSC#	High	M/IO#	Low
APCHK#	High	PCD	Low
BE[7:0]#	Floating	PCHK#	High
BREQ	Low	PWT	Low
CACHE#	High	SCYC	Low
D/C#	Low	SMIACT#	High
D[63:0], DP[7:0]	Floating	TDO	Floating
FERR#	High	VCC2DET	Low
HIT#	High	VCC2H/L#	Low
HITM#	High	W/R#	Low
HLDA	Low	–	–

Registers

Table 32 on page 175 shows the state of all architecture registers and Model-Specific Registers (MSRs) after the processor has completed its initialization due to the recognition of the assertion of RESET.