- –55°C to 125°C Operating Temperature Range, QML Processing
- Processed to MIL-PRF-38535 (QML)
- Two 1K-Word × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks
- Validated Ada Compiler
- 64-Word × 32-Bit Instruction Cache
- 32-Bit Instruction and Data Words, 24-Bit Addresses
- 40 / 32-Bit Floating-Point /Integer Multiplier and Arithmetic Logic Unit (ALU)
- Parallel ALU and Multiplier Execution in a Single Cycle
- On-Chip Direct Memory Access (DMA) Controller for Concurrent I / O and CPU Operation
- Integer, Floating-Point, and Logical Operations
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Zero-Overhead Loops With Single-Cycle Branches
- Interlocked Instructions for Multiprocessing Support
- 32-Bit Barrel Shifter
- Eight Extended-Precision Registers (Accumulators)
- Two- and Three-Operand Instructions
- Conditional Calls and Returns
- Block Repeat Capability
- Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) by Texas Instruments (TI™)
- Two 32-Bit Timers

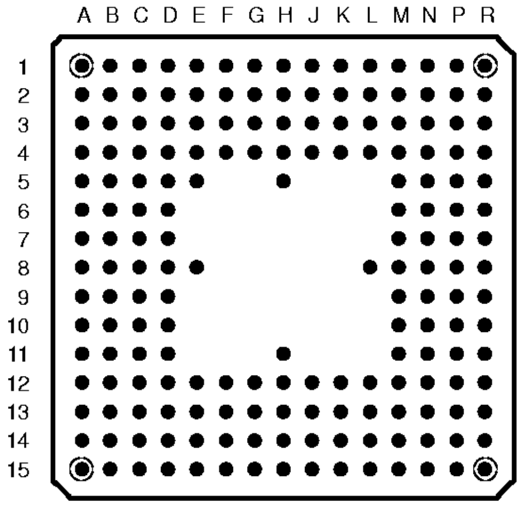
SMJ320C30 Key Features

- Performance
  - SMJ320C30-33 (60-ns Cycle)
    33 MFLOPS
    16.7 MIPS
  - SMJ320C30-40 (50-ns Cycle)
    40 MFLOPS
    20 MIPS
- One 4K-Word × 32-Bit Single-Cycle Dual-Access On-Chip ROM Block
- Two 32-Bit External Ports (24- and 13-Bit Address)
- Two Serial Ports With Support for 8- / 16- /24- /32-Bit Transfers
- Packaging
  - 181-Pin Grid Array Ceramic Package (GB Suffix)
  - 196-Pin Ceramic Quad Flatpack With Nonconductive Tie-Bar (HFG Suffix)
  - 244-Pad JEDEC Standard TAB Frame
- SMD Approval for 33- and 40-MHz Versions

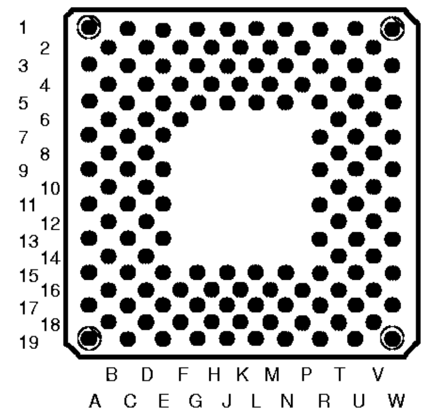
SMJ320C31 Key Features

- Performance
  - SMJ320C31-33 (60-ns Cycle)
    33.3 MFLOPS
    16.7 MIPS
  - SMJ320C31-40 (50-ns Cycle)
    40 MFLOPS
    20 MIPS
  - SMJ320C31-50 (40-ns Cycle)
    50 MFLOPS
    25 MIPS
- Flexible Boot-Program Loader
- One Serial Port to Support 8- / 16- /24- /32-Bit Transfers
- One 32-Bit Data Bus (24-Bit Address)
- Packaging
  - 132-Pin Ceramic Quad Flatpack With Nonconductive Tie-Bar (HFG Suffix)
  - 141-Pin Staggered Grid Array Ceramic Package (GFA Suffix)
  - 244-Pad JEDEC-Standard TAB Frame
- SMD Approval for 33-, 40-, and 50-MHz Versions

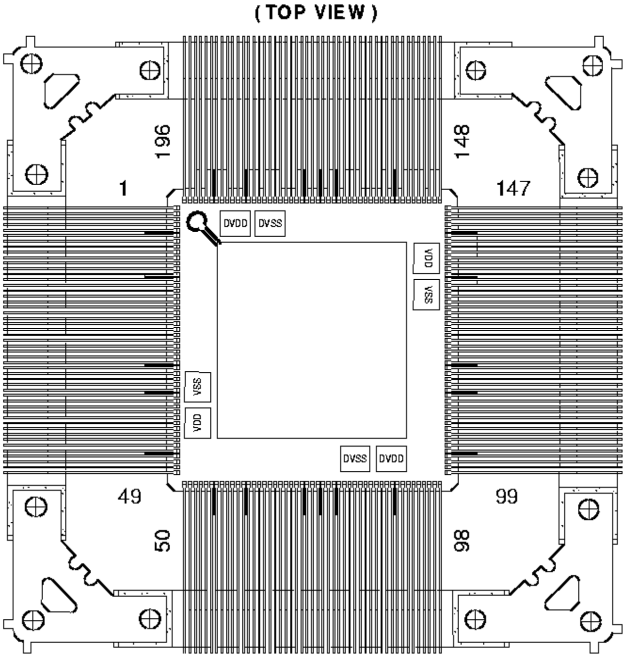
SMJ320C30
181-Pin GB Grid Array Package
(BOTTOM VIEW)



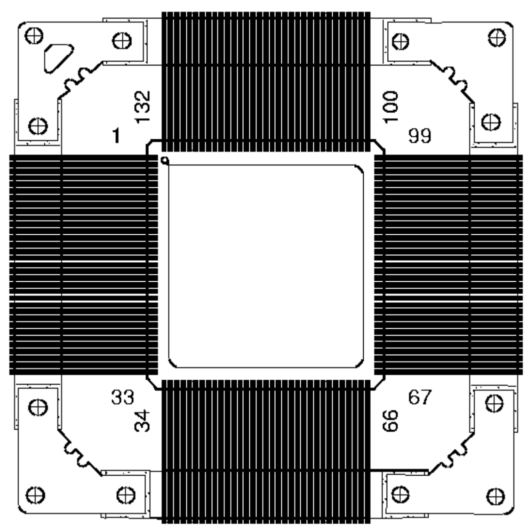
SMJ320C31
141-Pin GFA Staggered Grid Array Package
(BOTTOM VIEW)



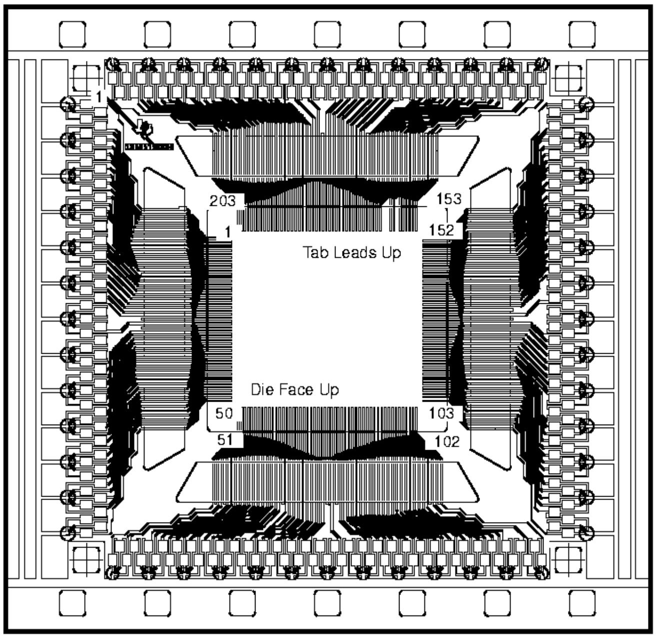
SMJ320C30
196-Pin HFG Quad Flatpack
(TOP VIEW)



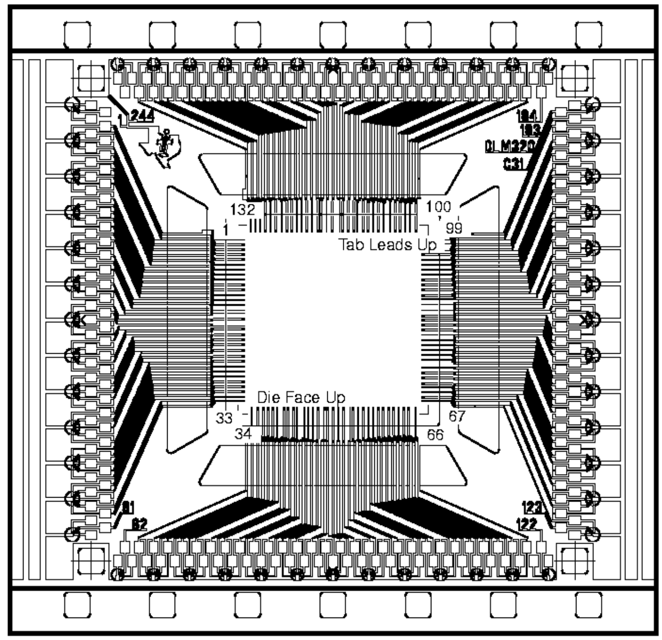
SMJ320C31
132-Pin HFG Quad Flatpack
(TOP VIEW)



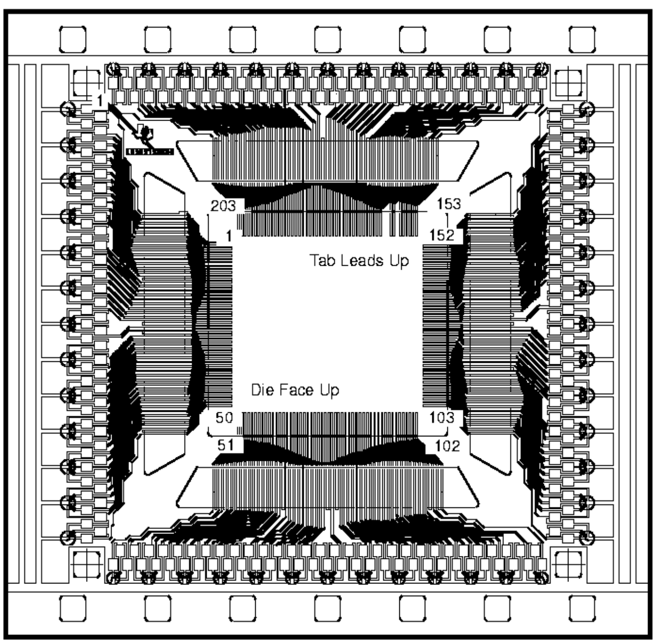
SMJ320C30 TA PACKAGE
(TOP VIEW)



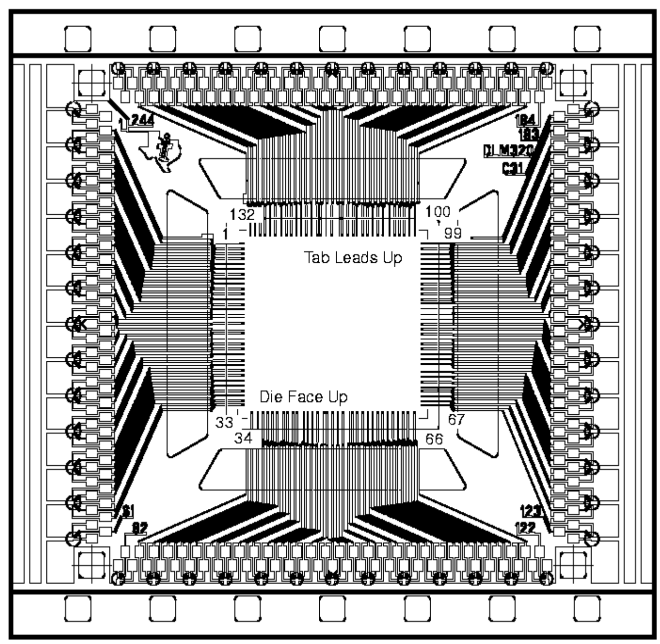
SMJ320C31 TA PACKAGE
(TOP VIEW)



SMJ320C30 TB PACKAGE
(TOP VIEW)



SMJ320C31 TB PACKAGE
(TOP VIEW)



description

The SMJ320C3x's internal busing and special digital signal processing (DSP) instruction set have the speed and flexibility to execute up to 50 MFLOPS (million floating-point operations per second). The SMJ320C3x devices optimize speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The emphasis on total system cost has resulted in a less expensive processor that can be designed into systems currently using costly bit-slice processors. Also, appropriate selection based on cost and performance is enhanced by the different processors in the SMJ320C3x line:

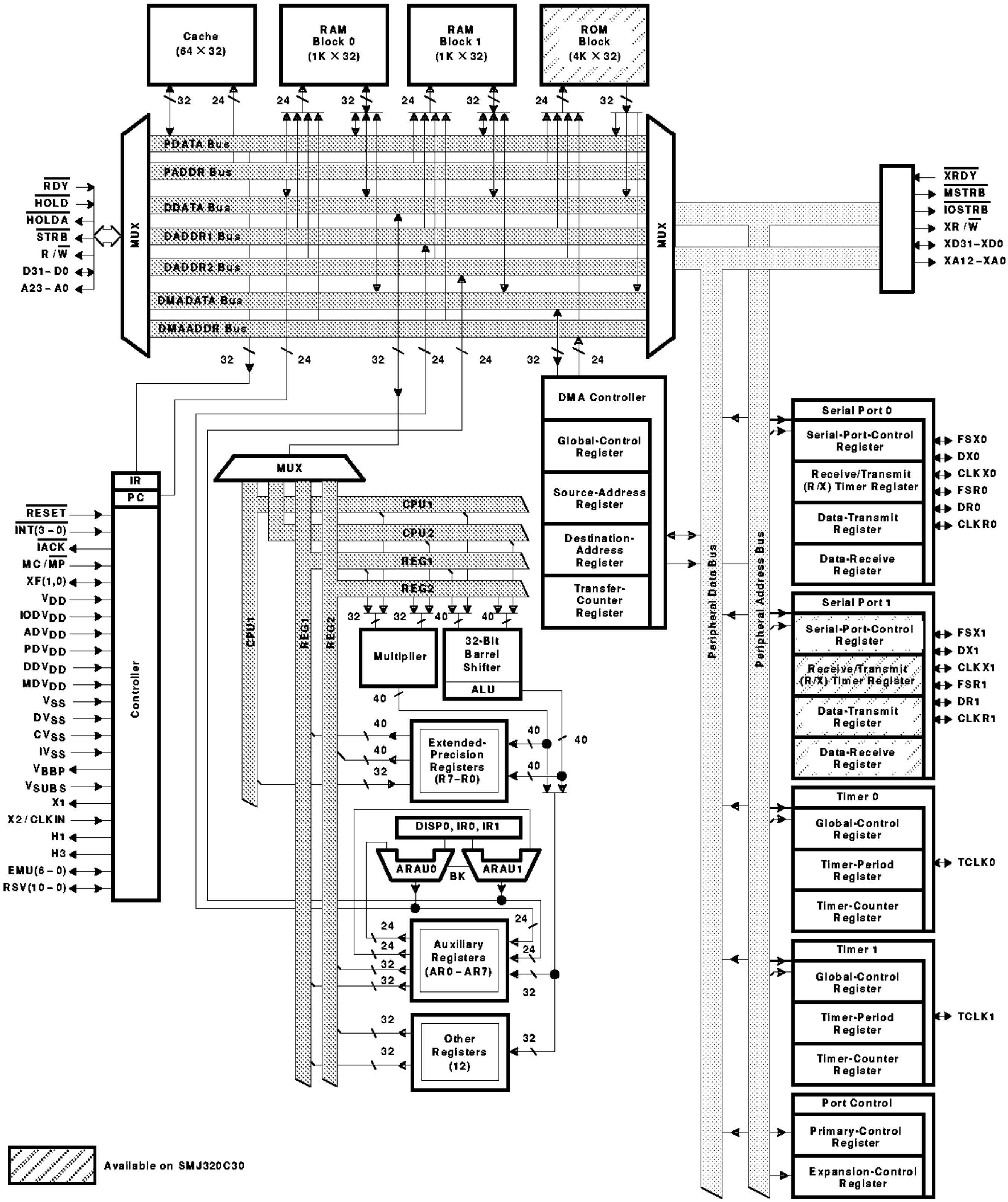
- SMJ320C30-33: 60-ns single-cycle execution time, 10% supply
- SMJ320C30-40: 50-ns single-cycle execution time, 5% supply
- SMJ320C31-33: Low cost, reduced overall size, 60-ns single-cycle execution time, 10% supply
- SMJ320C31-40: Low cost, reduced overall size, 50-ns single-cycle execution time, 5% supply
- SMJ320C31-50: Low cost, reduced overall size, 40-ns single-cycle execution time, 5% supply

The SMJ320C30 and SMJ320C31 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

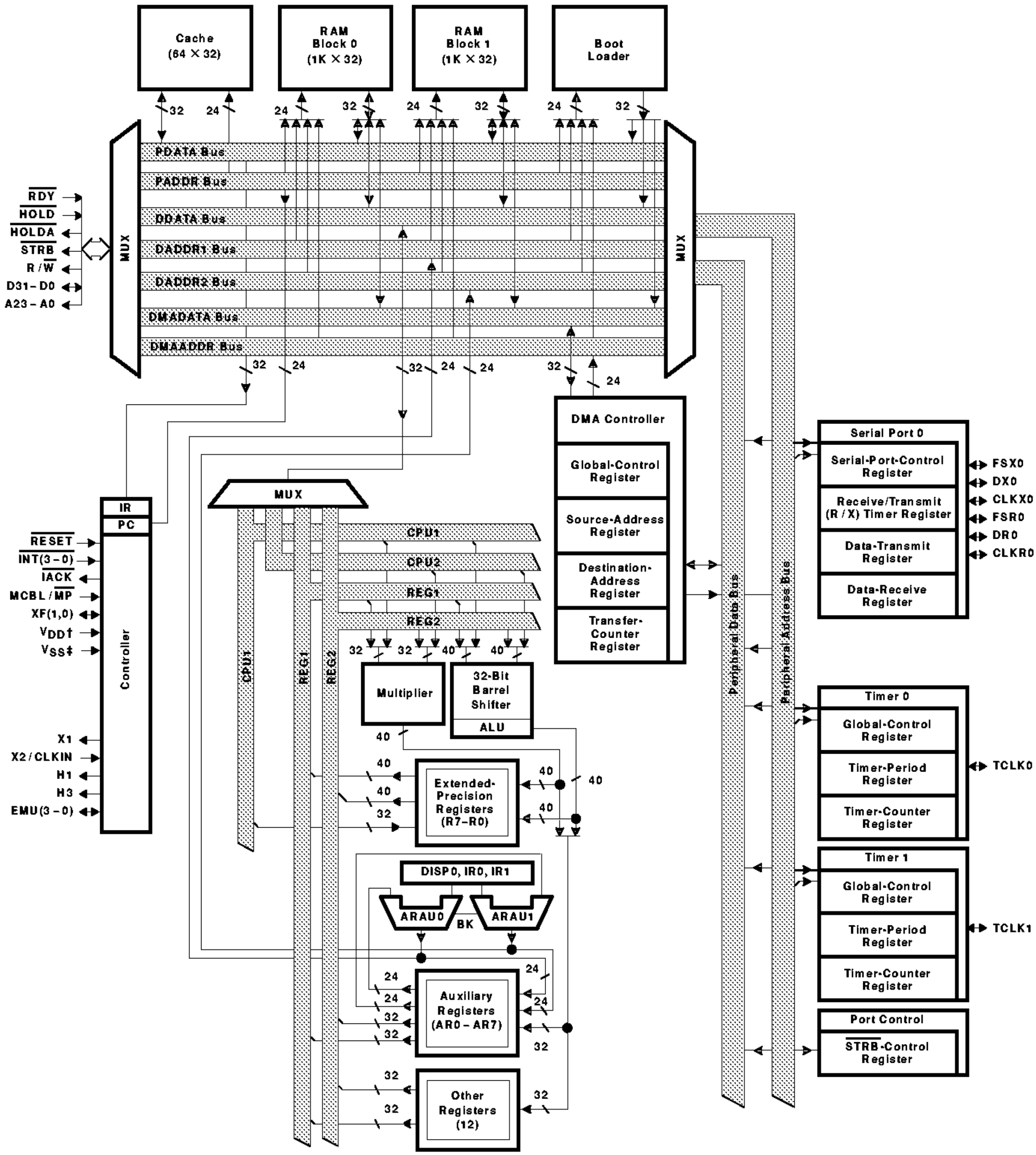
General-purpose applications are enhanced greatly by the large address space, multiprocessor interface, internally and externally generated wait states, external interface ports (two on the SMJ320C30, one on the SMJ320C31), two timers, serial ports (two on the SMJ320C30, one on the SMJ320C31), and multiple interrupt structure. The SMJ320C3x supports a wide variety of system applications from host processor to dedicated coprocessor.

High-level language support is implemented easily through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

functional block diagram for SMJ320C30



functional block diagram for SMJ320C31



† V_{DD} includes AV_{DD}, V_{DDL}, DV_{DD}, CV_{DD}, and PV_{DD}.
‡ V_{SS} includes DV_{SS}, CV_{SS}, V_{SSL}, and IV_{SS}.

memory map

Figure 1 depicts the memory map for the SMJ320C30 and SMJ320C31. Refer to the TMS320C3x User's Guide (literature number SPRU031) for a detailed description of this memory mapping.

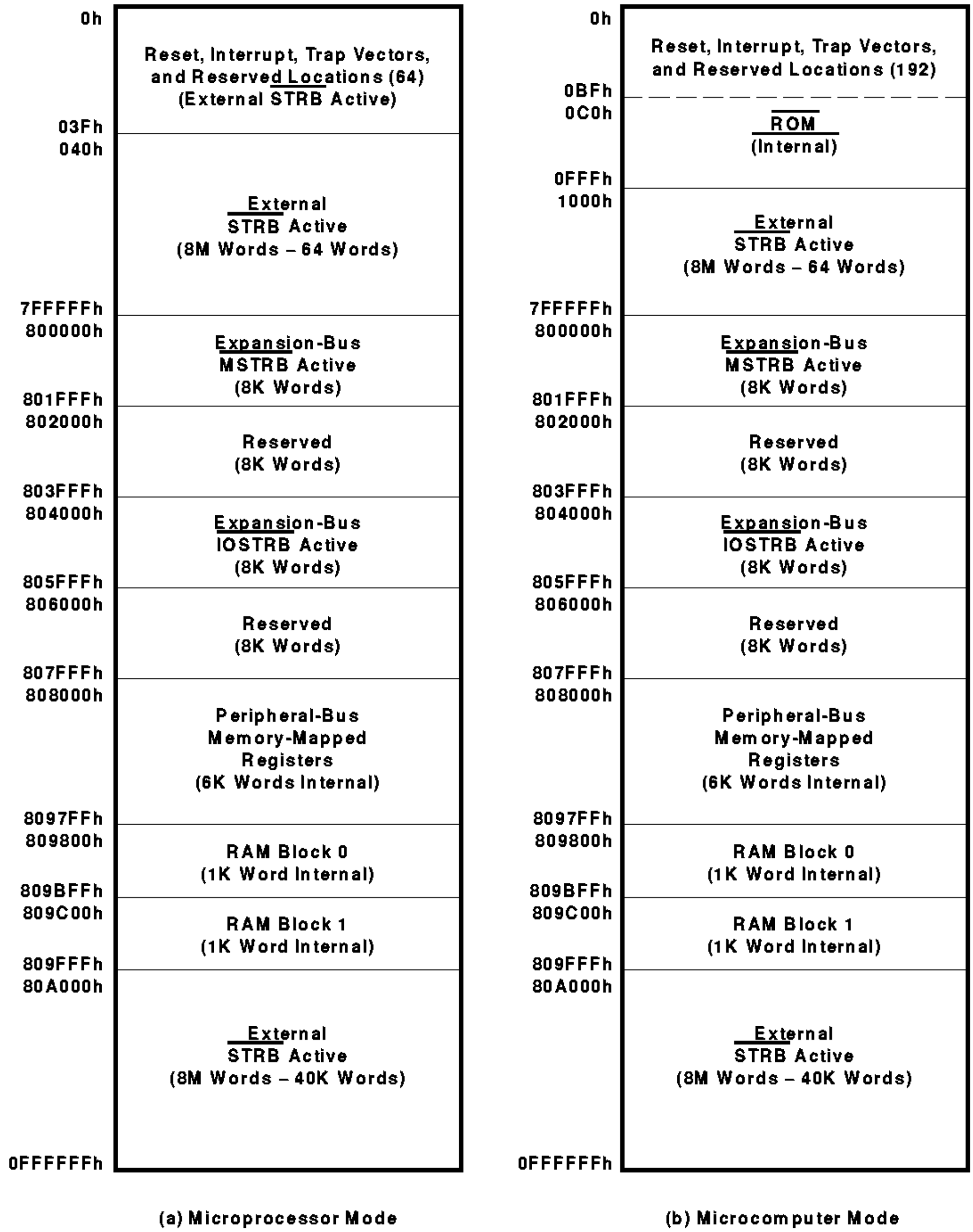


Figure 1. SMJ320C30 and SMJ320C31 Memory Map

pin functions

This section gives signal descriptions for the SMJ320C3x devices in the microprocessor mode. The following tables list each signal, the number of pins, type of operating mode(s) (that is, input, output, or high-impedance state as indicated by I, O, or Z, respectively), and a brief function description. All pins labeled NC have special functions and should not be connected by the user. A line over a signal name (for example, $\overline{\text{RESET}}$) indicates that the signal is active low (true at logic-0 level). The signals are grouped according to functions.

SMJ320C30 Pin Functions

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§		
PRIMARY BUS INTERFACE						
D31–D0	32	I/O/Z	32-bit data port of the primary bus interface	S	H	
A23–A0	24	O/Z	24-bit address port of the primary bus interface	S	H	R
R/$\overline{\text{W}}$	1	O/Z	Read/write for primary bus interface. R/$\overline{\text{W}}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{\text{STRB}}$	1	O/Z	External access strobe for the primary bus interface	S	H	
$\overline{\text{RDY}}$	1	I	Ready. $\overline{\text{RDY}}$ indicates that the external device is prepared for a primary bus interface transaction to complete.			
$\overline{\text{HOLD}}$	1	I	Hold for primary bus interface. When $\overline{\text{HOLD}}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and all transactions over the primary bus interface are held until $\overline{\text{HOLD}}$ becomes a logic high or the NOHOLD bit of the primary bus control register is set.			
$\overline{\text{HOLDA}}$	1	O/Z	Hold acknowledge for primary bus interface. $\overline{\text{HOLDA}}$ is generated in response to a logic low on $\overline{\text{HOLD}}$. $\overline{\text{HOLDA}}$ indicates that A23–A0, D31–D0, $\overline{\text{STRB}}$, and R/$\overline{\text{W}}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{\text{HOLDA}}$ is high in response to a logic high of $\overline{\text{HOLD}}$ or when the NOHOLD bit of the primary bus control register is set.	S		
EXPANSION BUS INTERFACE						
XD31–XD0	32	I/O/Z	32-bit data port of the expansion bus interface	S		R
XA12–XA0	13	O/Z	13-bit address port of the expansion bus interface	S		R
XR/$\overline{\text{W}}$	1	O/Z	Read/write signal for expansion bus interface. When a read is performed, XR/$\overline{\text{W}}$ is held high; when a write is performed, XR/$\overline{\text{W}}$ is low.	S		R
$\overline{\text{MSTRB}}$	1	O/Z	External memory access strobe for the expansion bus interface	S		
$\overline{\text{IOSTRB}}$	1	O/Z	External I/O access strobe for the expansion bus interface	S		
$\overline{\text{XRDY}}$	1	I	Ready signal. $\overline{\text{XRDY}}$ indicates that the external device is prepared for an expansion bus interface transaction to complete.			
CONTROL SIGNALS						
$\overline{\text{RESET}}$	1	I	Reset. When $\overline{\text{RESET}}$ is a logic low, the device is in the reset condition. When $\overline{\text{RESET}}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{\text{INT3}}$–$\overline{\text{INT0}}$	4	I	External interrupts			
$\overline{\text{IACK}}$	1	O/Z	Interrupt acknowledge. $\overline{\text{IACK}}$ is set to a logic high by the IACK instruction. $\overline{\text{IACK}}$ can be used to indicate the beginning or end of an interrupt-service routine.	S		
MC/$\overline{\text{MP}}$	1	I	Microcomputer/microprocessor mode			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instructions.	S		R

† I = input, O = output, Z = high-impedance state
‡ For GB package
§ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active

SMJ320C30 Pin Functions (Continued)

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§	
SERIAL PORT 0 SIGNALS					
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial-shift clock for the serial port 0 transmitter.	S	R
DX0	1	I/O/Z	Data transmit output. Serial port 0 transmits serial data on DX0.	S	R
FSX0	1	I/O/Z	Frame synchronization pulse for transmit. The FSX0 pulse initiates the transmit-data process over DX0.	S	R
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial-shift clock for the serial port 0 receiver.	S	R
DR0	1	I/O/Z	Data receive. Serial port 0 receives serial data on DR0.	S	R
FSR0	1	I/O/Z	Frame synchronization pulse for receive. The FSR0 pulse initiates the receive-data process over DR0.	S	R
SERIAL PORT 1 SIGNALS					
CLKX1	1	I/O/Z	Serial port 1 transmit clock. CLKX1 is the serial-shift clock for the serial port 1 transmitter.	S	R
DX1	1	I/O/Z	Data transmit output. Serial port 1 transmits serial data on DX1.	S	R
FSX1	1	I/O/Z	Frame synchronization pulse for transmit. The FSX1 pulse initiates the transmit-data process over DX1.	S	R
CLKR1	1	I/O/Z	Serial port 1 receive clock. CLKR1 is the serial-shift clock for the serial port 1 receiver.	S	R
DR1	1	I/O/Z	Data receive. Serial port 1 receives serial data on DR1.	S	R
FSR1	1	I/O/Z	Frame synchronization pulse for receive. The FSR1 pulse initiates the receive-data process over DR1.	S	R
TIMER 0 SIGNALS					
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TIMER 1 SIGNALS					
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS (see Note 1)					
V_{DD}	4	I	5-V supply¶		
$IODV_{DD}$	2	I	5-V supply¶		
ADV_{DD}	2	I	5-V supply¶		
PDV_{DD}	1	I	5-V supply¶		
DDV_{DD}	2	I	5-V supply¶		
MDV_{DD}	1	I	5-V supply¶		
V_{SS}	4	I	Ground		
DV_{SS}	4	I	Ground		
CV_{SS}	2	I	Ground		

† I = input, O = output, Z = high-impedance state
‡ For GB package
§ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active
¶ Recommended decoupling capacitor is 0.1 μF.
NOTE 1: CV_{SS}, V_{SS}, and IV_{SS} are on the same plane.

SMJ320C30 Pin Functions (Continued)

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§
SUPPLY AND OSCILLATOR SIGNALS (CONTINUED) (see Note 1)				
IV_{SS}	1	I	Ground	
V_{BBP}	1	NC	V_{BB} pump oscillator output	
V_{SUBS}	1	I	Substrate pin. Tie to ground	
X1	1	O	Output from the internal oscillator for the crystal. If a crystal is not used, X1 should be left unconnected.	
X2/CLKIN	1	I	Input to the internal oscillator from the crystal or a clock	
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
RESERVED¶				
EMU0–EMU2	3	I	Reserved. Use pullup resistors to 5 V	
EMU3	1	O/Z	Reserved	S
EMU4/$\overline{\text{SHZ}}$	1	I	Shutdown high impedance. When active, EMU4/$\overline{\text{SHZ}}$ shuts down the SMJ320C30 and places all pins in the high-impedance state. EMU4/$\overline{\text{SHZ}}$ is used for board-level testing to ensure that no dual drive conditions occur. **CAUTION:** A low on $\overline{\text{SHZ}}$ corrupts SMJ320C30 memory and register contents. Reset the device with $\overline{\text{SHZ}}$ high to restore it to a known operating condition.	
EMU5, EMU6	2	NC	Reserved	
RSV0–RSV4	5	I	Reserved. Tie pins directly to 5 V	
RSV5–RSV10	6	I/O	Reserved. Use pullups on each pin to 5 V	
Locator	1	NC	Reserved	

† I = input, O = output, Z = high-impedance state, NC = No Connect
‡ For GB package
§ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active
¶ Follow the connections specified for the reserved pins. Use 18-kΩ –22-kΩ pullup resistors for best results. All 5-V supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.
NOTE 1: CV_{SS}, V_{SS}, IV_{SS} are on the same plane.

SMJ320C31 Pin Functions

PIN NAME	PIN QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§		
PRIMARY BUS INTERFACE						
D31–D0	32	I/O/Z	32-bit data port of the primary bus interface	S	H	R
A23–A0	24	O/Z	24-bit address port of the primary bus interface	S	H	R
R/$\overline{W}$	1	O/Z	Read/write. R/$\overline{W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S	H	R
$\overline{STRB}$	1	O/Z	External access strobe of the primary bus interface	S	H	
$\overline{RDY}$	1	I	Ready. $\overline{RDY}$ indicates that the external device is prepared for a transaction completion.			
$\overline{HOLD}$	1	I	Hold. When $\overline{HOLD}$ is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state, and all transactions over the primary bus interface are held until $\overline{HOLD}$ becomes a logic high or the NOHOLD bit of the primary bus control register is set.			
$\overline{HOLDA}$	1	O/Z	Hold acknowledge. $\overline{HOLDA}$ is generated in response to a logic low on $\overline{HOLD}$. $\overline{HOLDA}$ indicates that A23–A0, D31–D0, $\overline{STRB}$, and R/$\overline{W}$ are in the high-impedance state and that all transactions over the bus are held. $\overline{HOLDA}$ is high in response to a logic high of $\overline{HOLD}$ or the NOHOLD bit of the primary bus control register being set.	S		
CONTROL SIGNALS						
$\overline{RESET}$	1	I	Reset. When $\overline{RESET}$ is a logic low, the device is in the reset condition. When $\overline{RESET}$ becomes a logic high, execution begins from the location specified by the reset vector.			
$\overline{INT3}$–$\overline{INT0}$	4	I	External interrupts			
$\overline{IACK}$	1	O/Z	Interrupt acknowledge. $\overline{IACK}$ is set to a logic high by the IACK instruction. $\overline{IACK}$ can be used to indicate the beginning or the end of an interrupt-service routine.	S		
MCBL/$\overline{MP}$	1	I	Microcomputer boot loader/microprocessor mode select			
$\overline{SHZ}$	1	I	Shutdown high impedance. When active, $\overline{SHZ}$ shuts down the SMJ320C31 and places all pins in the high-impedance state. $\overline{SHZ}$ is used for board-level testing to ensure that no dual drive conditions occur. **CAUTION:** A low on $\overline{SHZ}$ corrupts SMJ320C31 memory and register contents. Reset the device with $\overline{SHZ}$ high to restore it to a known operating condition.			
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S		R
SERIAL PORT 0 SIGNALS						
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial-shift clock for the serial port 0 receiver.	S		R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial-shift clock for the serial port 0 transmitter.	S		R
DR0	1	I/O/Z	Data receive. Serial port 0 receives serial data on DR0.	S		R
DX0	1	I/O/Z	Data transmit output. Serial port 0 transmits serial data on DX0.	S		R
FSR0	1	I/O/Z	Frame synchronization pulse for receive. The FSR0 pulse initiates the receive-data process over DR0.	S		R
FSX0	1	I/O/Z	Frame synchronization pulse for transmit. The FSX0 pulse initiates the transmit-data process over DX0.	S		R

† I = input, O = output, Z = high-impedance state
‡ For GFA package. F6 pin is not connected.
§ S = $\overline{SHZ}$ active, H = $\overline{HOLD}$ active, R = $\overline{RESET}$ active

SMJ320C31 Pin Functions (Continued)

PIN NAME	QTY‡	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE§	
TIMER SIGNALS					
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S	R
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S	R
SUPPLY AND OSCILLATOR SIGNALS					
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S	
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S	
V_{DD}¶	20	I	5-V supply. All must be connected to a common supply plane.#		
V_{SS}‖	32	I	Ground. All grounds must be connected to a common ground plane.		
V_{SUBS}	1	I	Substrate pin. Tie to ground		
X1	1	O/Z	Output from the internal crystal oscillator. If a crystal is not used, X1 should be left unconnected.	S	
X2/CLKIN	1	I	Internal oscillator input from a crystal or a clock		
RESERVED☆					
EMU2–EMU0	3	I	Reserved. Use pullup resistors to 5 V		
EMU3	1	O/Z	Reserved	S	

† I = input, O = output, Z = high-impedance state
‡ For GFA package. F6 pin is not connected.
§ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active
¶ V_{DD} includes AV_{DD}, V_{DDL}, DV_{DD}, CV_{DD}, and PV_{DD}.
# Recommended decoupling capacitor value is 0.1 µF.
‖ V_{SS} includes DV_{SS}, CV_{SS}, V_{SSL}, and IV_{SS}.
☆ Follow the connections specified for the reserved pins. Use 18-kΩ – 22-kΩ pullup resistors for best results. All 5-V supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

SMJ320C30 Pin Assignments

PIN			PIN			PIN			PIN			PIN		
NUMBER		NAME	NUMBER		NAME	NUMBER		NAME	NUMBER		NAME	NUMBER		NAME
GB PKG	HFG PKG		GB PKG	HFG PKG		GB PKG	HFG PKG		GB PKG	HFG PKG		GB PKG	HFG PKG	
F15	82	A0	C5	139	D5	P2	195	DX1	L2	185	RSV6	R8	29	XD11
G12	81	A1	D6	138	D6	F14	83	EMU0	K4	186	RSV7	R9	30	XD12
G13	80	A2	A4	137	D7	E15	84	EMU1	M1	187	RSV8	P9	31	XD13
G14	79	A3	B5	136	D8	F13	85	EMU2	L3	188	RSV9	N9	32	XD14
G15	78	A4	C6	135	D9	E14	86	EMU3	M2	189	RSV10	R10	33	XD15
H15	77	A5	A5	134	D10	F12	87	EMU4/$\overline{SHZ}$	D12	100	ADV_{DD}†	M9	34	XD16
H14	72	A6	B6	133	D11	C1	155	EMU5	H11	64	ADV_{DD}†	P10	35	XD17
J15	71	A7	D7	132	D12	M6	11	EMU6	D4	114	DDV_{DD}†	R11	36	XD18
J14	70	A8	A6	131	D13	B3	145	H1	E8	147	DDV_{DD}†	N10	37	XD19
J13	69	A9	C7	130	D14	A1	146	H3	L8	15	$IODV_{DD}$†	P11	38	XD20
K15	68	A10	B7	129	D15	C2	152	X1	M12	16	$IODV_{DD}$†	R12	39	XD21
J12	67	A11	A7	128	D16	B1	151	X2/CLKIN		49	$IODV_{DD}$†	M10	40	XD22
K14	66	A12	A8	127	D17	P4	9	TCLK0	H5	162	MDV_{DD}†	N11	41	XD23
L15	65	A13	B8	122	D18	N5	10	TCLK1		163	MDV_{DD}†	P12	42	XD24
K13	63	A14	A9	121	D19	G2	169	XF0	M4	1	PDV_{DD}†	R13	43	XD25
L14	62	A15	B9	120	D20	G3	168	XF1	B2	51	CV_{SS}§	R14	44	XD26
M15	61	A16	C9	119	D21	D3	154	V_{BBP}	P14	52	CV_{SS}§	M11	45	XD27
K12	60	A17	A10	118	D22	E4	153	V_{SUBS}		25	V_{DD}‡	N12	46	XD28
L13	59	A18	D9	117	D23	H4	123	V_{DD}‡		26	V_{DD}‡	P13	47	XD29
M14	58	A19	B10	116	D24	D8	73	V_{DD}‡		172	V_{DD}‡	R15	48	XD30
N15	57	A20	A11	115	D25	M8	74	V_{DD}‡		173	V_{DD}‡	P15	53	XD31
M13	56	A21	C10	113	D26	H12	124	V_{DD}‡	C8	28	V_{SS}§		2	DV_{DD}
L12	55	A22	B11	112	D27	N8	27	V_{SS}§	H3	75	V_{SS}§		101	DV_{DD}
N14	54	A23	A12	111	D28	A13	107	XA0	H13	76	V_{SS}§	C3	50	DV_{SS}¶
E5		LOCATOR/NC	D10	110	D29	A14	106	XA1		125	V_{SS}§	C13	98	DV_{SS}¶
G1	170	$\overline{IACK}$	C11	109	D30	D11	105	XA2		126	V_{SS}§	N3	148	DV_{SS}¶
H2	171	$\overline{INT0}$	B12	108	D31	C12	104	XA3		149	V_{SS}§	N13	196	DV_{SS}¶
H1	176	$\overline{INT1}$	F3	161	$\overline{HOLD}$	B13	103	XA4		150	V_{SS}§	B14	96	IV_{SS}§
J1	177	$\overline{INT2}$	E2	160	$\overline{HOLDA}$	A15	102	XA5		174	V_{SS}§		97	IV_{SS}§
J2	178	$\overline{INT3}$	D2	156	$\overline{XRDY}$	B15	95	XA6		175	V_{SS}§			
D15	88	MC/$\overline{MP}$	D1	159	XR/$\overline{W}$	C14	94	XA7		99	V_{SUBS}			
E3	157	$\overline{MSTRB}$	P3	4	FSR0	E12	93	XA8	R4	12	XD0			
E1	164	$\overline{RDY}$	R2	7	FSX0	D13	92	XA9	P5	13	XD1			
F1	167	$\overline{RESET}$	N4	5	CLKR0	C15	91	XA10	N6	14	XD2			
G4	166	R/$\overline{W}$	M5	6	CLKX0	D14	90	XA11	R5	17	XD3			
F2	165	$\overline{STRB}$	R1	3	DR0	E13	89	XA12	P6	18	XD4			
F4	158	$\overline{IOSTRB}$	R3	8	DX0	J3	179	RSV0	M7	19	XD5			
C4	144	D0	M3	191	FSR1	J4	180	RSV1	R6	20	XD6			
D5	143	D1	P1	194	FSX1	K1	181	RSV2	N7	21	XD7			
A2	142	D2	L4	192	CLKR1	K2	182	RSV3	P7	22	XD8			
A3	141	D3	N2	193	CLKX1	L1	183	RSV4	R7	23	XD9			
B4	140	D4	N1	190	DR1	K3	184	RSV5	P8	24	XD10			

† ADV_{DD}, DDV_{DD}, $IODV_{DD}$, MDV_{DD}, and PDV_{DD} are on a common plane internal to the device.
‡ V_{DD} is on a common plane internal to the device.
§ V_{SS}, CV_{SS}, and IV_{SS} are on a common plane internal to the device.
¶ DV_{SS} is on a common plane internal to the device.

SMJ320C31 Pin Assignments

PIN			PIN			PIN			PIN		
NUMBER		NAME	NUMBER		NAME	NUMBER		NAME	NUMBER		NAME
HFG PKG	GFA PKG		HFG PKG	GFA PKG		HFG PKG	GFA PKG		HFG PKG	GFA PKG	
12	L1	A0	47	W9	D10	86	E19	$\overline{INT1}$	18	P4	V_{SSL}†
11	K2	A1	46	U9	D11	89	F18	$\overline{INT2}$	19	T10	V_{SSL}†
10	J1	A2	45	V8	D12	90	G17	$\overline{INT3}$	20	K4	DV_{SS}
9	J3	A3	43	W7	D13	110	C11	MCBL/$\overline{MP}$	25	T4	IV_{SS}†
8	G1	A4	41	U7	D14	77	L19	R/$\overline{W}$	34	G3	DV_{SS}
6	F2	A5	39	V6	D15	75	N17	$\overline{RDY}$	40	K16	CV_{SS}†
5	E1	A6	38	W5	D16	78	K18	$\overline{RESET}$	44	T8	IV_{SS}†
4	E3	A7	37	U5	D17	101	A17	$\overline{SHZ}$	52	T12	DV_{SS}
3	D2	A8	36	V4	D18	76	M18	$\overline{STRB}$	53	R11	V_{SSL}†
1	C1	A9	35	W3	D19	103	B16	TCLK0	54	J15	V_{SSL}†
131	C3	A10	33	U3	D20	105	C15	TCLK1	67	W13	DV_{SS}
129	B2	A11	31	V2	D21	121	G5	AV_{DD}‡	68	D10	CV_{SS}†
128	A1	A12	30	W1	D22	130	E7	AV_{DD}‡	69	D16	IV_{SS}†
127	C5	A13	29	R3	D23	7	E5	AV_{DD}‡	84	T16	DV_{SS}
126	B4	A14	28	T2	D24	15	N5	V_{DDL}	85	D12	V_{SSL}†
125	A3	A15	27	U1	D25	16	R5	V_{DDL}	92	F16	CV_{SS}†
124	C7	A16	26	N3	D26	23	H4	DV_{DD}‡	96	H16	IV_{SS}†
123	B6	A17	24	P2	D27	32	J5	DV_{DD}‡	100	D14	V_{SUBS}§
122	C9	A18	22	R1	D28	42	T14	DV_{DD}‡	102	U15	DV_{SS}
120	B8	A19	21	L3	D29	48	R7	V_{DDL}	111	C13	CV_{SS}†
117	A7	A20	17	M2	D30	49	R9	V_{DDL}	71	T18	X1
116	A9	A21	14	N1	D31	57	R13	DV_{DD}‡	70	U19	X2/CLKIN
113	B10	A22	91	C19	DR0	66	R15	DV_{DD}‡	79	J19	XF0
112	A11	A23	99	C17	DX0	74	P16	CV_{DD}‡	81	G19	XF1
94	E17	CLKR0	107	B14	EMU0	80	N15	CV_{DD}‡		F6	No Connect
95	A19	CLKX0	108	A13	EMU1	87	G15	V_{DDL}		D4	DV_{SS}
63	W19	D0	109	B12	EMU2	88	E15	V_{DDL}		N19	DV_{SS}
62	V16	D1	106	A15	EMU3	98	L15	PV_{DD}‡		R17	DV_{SS}
61	W17	D2	93	D18	FSR0	104	E9	PV_{DD}‡		L17	DV_{SS}
60	U13	D3	97	B18	FSX0	114	E13	V_{DDL}		M16	DV_{SS}
59	V14	D4	73	P18	$\overline{HOLD}$	115	E11	V_{DDL}		D6	DV_{SS}
58	W15	D5	72	R19	$\overline{HOLDA}$	118	L5	V_{SSL}†		A5	DV_{SS}
56	U11	D6	64	V18	H1	119	H2	DV_{SS}		D8	DV_{SS}
55	V12	D7	65	U17	H3	132	M4	CV_{SS}†			
51	W11	D8	82	H18	$\overline{IACK}$	2	F4	DV_{SS}			
50	V10	D9	83	J17	$\overline{INT0}$	13	T6	CV_{SS}†			

† CV_{SS}, V_{SSL}, and IV_{SS} are on the same plane.
‡ AV_{DD}, DV_{DD}, CV_{DD}, and PV_{DD} are on the same plane.
§ V_{SUBS} connects to die metallization. Tie this pin to clean ground.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 2) . . . . –0.3 V to 7 V
Input voltage range, V_I . . . . – 0.3 V to 7 V
Output voltage range, V_O . . . . –0.3 V to 7 V
Continuous power dissipation (see Note 3) . . . . 3.15 W
Operating free-air temperature range, T_A . . . . – 55°C to 125°C
Storage temperature range, T_{stg} . . . . – 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. All voltage values are with respect to V_{SS}.
3. Actual operating power is less. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 4)

			MIN	NOM‡	MAX	UNIT
V_{DD}	Supply voltage (AV_{DD}, etc.)	'320C30-40 '320C31-40 '320C31-50	4.75	5	5.25	V
		'320C30-33 '320C31-33	4.5	5	5.5	
V_{SS}	Supply voltage (CV_{SS}, etc.)			0		V
V_{IH}	High-level input voltage		2.1		V_{DD} + 0.3§	V
V_{TH}	High-level input voltage for CLKIN		3		V_{DD} + 0.3§	V
V_{IL}	Low-level input voltage		– 0.3§		0.8	V
I_{OH}	High-level output current				– 300	μA
I_{OL}	Low-level output current				2	mA
T_A	Operating free-air temperature		– 55		125	°C

‡ All nominal values are at V_{DD} = 5 V, T_A = 25°C.
§ These values are derived from characterization and not tested.
NOTE 4: All input and output voltage levels are TTL compatible.

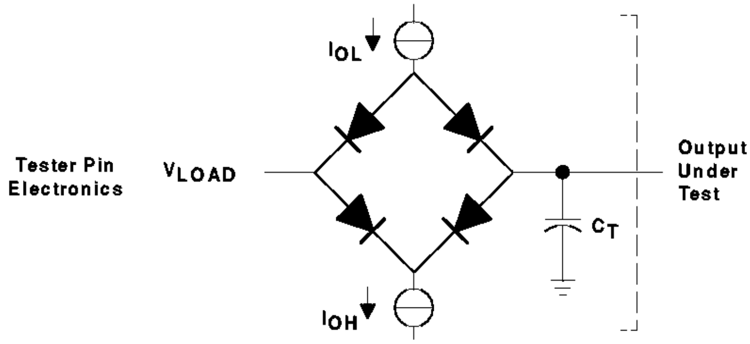
electrical characteristics over recommended ranges of supply voltage (unless otherwise noted) (see Note 4)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = MIN, I_{OH} = MAX		2.4	3		V
V_{OL}	Low-level output voltage	For XA12–XA0	V_{DD} = MIN, I_{OL} = MAX				0.6§	V
		All others	V_{DD} = MIN, I_{OL} = MAX			0.3	0.6	V
I_Z	High-impedance current		V_{DD} = MAX				± 20	µA
I_I	Input current		$V_I = V_{SS}$ to V_{DD}				± 10	µA
I_{IP}	Input current		Inputs with internal pullups (see Note 5)		– 400		20	µA
I_{IC}	Input current (X2/CLKIN)		$V_I = V_{SS}$ to V_{DD}				± 50	µA
I_{CC}	Supply current		V_{DD} = MAX, T_A = 25°C, $t_{c(CI)}$ = MIN, See Note 6	'320C30-33		200	600	mA
				'320C31-33		150	325	
				'320C30-40		200	600	
				'320C31-40		250	400	
				'320C31-50		350	500	
I_{DD}	Supply current, standby; IDLE2, clock shut off		V_{DD} = 5 V, T_A = 25°C			50		mA
C_i	Input capacitance						15¶	pF
C_o	Output capacitance						20¶	pF
C_x	X2/CLKIN capacitance						25¶	pF

† For conditions shown as MIN/MAX, use the appropriate value specified in recommended operating conditions.
‡ All typical values are at V_{DD} = 5 V, T_A = 25°C.
§ These values are derived from characterization but not tested.
¶ These values are derived by design but not tested.

NOTES: 4. All input and output voltage levels are TTL compatible.
5. Pins with internal pullup devices: $\overline{\text{INT0}}$–$\overline{\text{INT3}}$, MC/$\overline{\text{MP}}$, RSV0–RSV10. Although RSV0–RSV10 have internal pullup devices, external pullups should be used on each pin as identified in the Pin Functions tables.
6. Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 2 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{LOAD} = Selected to emulate 50 Ω termination (typical value = 1.54 V).
C_T = 80-pF typical load-circuit capacitance

Figure 2. Test Load Circuit

signal transition levels

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

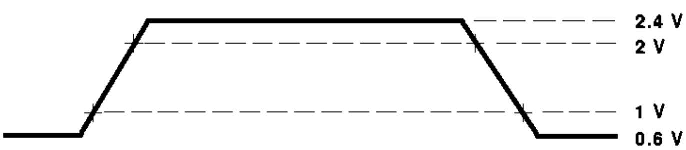


Figure 3. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2.1 V and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2.1 V.

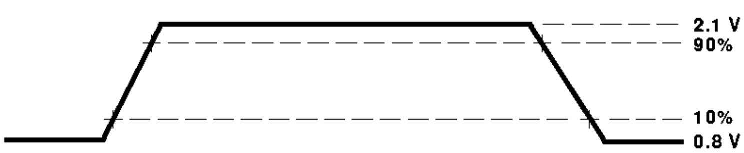


Figure 4. TTL-Level Inputs

PARAMETER MEASUREMENT INFORMATION

SMJ320C30, SMJ320C31 timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the terminal names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23–A0	IACK	$\overline{\text{IACK}}$
ASYNCH	Asynchronous reset signals, include XF0, XF1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1	INT	$\overline{\text{INT3}}$–$\overline{\text{INT0}}$
CH	CLKX, includes CLKX0 and CLKX1	IOS	$\overline{\text{IOSTRB}}$
CI	CLKIN	(M)S	$\overline{\text{(M)STRB}}$, includes $\overline{\text{MSTRB}}$ and $\overline{\text{STRB}}$
CONTROL	Control signals, include $\overline{\text{STRB}}$, $\overline{\text{MSTRB}}$, and $\overline{\text{IOSTRB}}$	RDY	$\overline{\text{RDY}}$
D	D31–D0	RESET	$\overline{\text{RESET}}$
DR	Includes DR0, DR1	RW	R/$\overline{\text{W}}$
DX	Includes DX0, DX1	S	$\overline{\text{STRB}}$
FS	FSX/R, includes FSX0, FSX1, FSR0, and FSR1	SCK	CLKX/R, includes CLKX0, CLKX1, CLKR0, and CLKR1
FSR	Includes FSR0, FSR1	TCLK	TCLK0, TCLK1
FSX	Includes FSX0, FSX1	(X)A	Includes A23–A0 and XA12–XA0
GPIO	General-purpose input/output; peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1	(X)D	Includes D31–D0 and XD31–XD0
H	Includes H1, H3	XF	XFx, includes XF0 and XF1
H1	H1	XF0	XF0
H3	H3	XF1	XF1
HOLD	$\overline{\text{HOLD}}$	(X)RDY	Includes $\overline{\text{RDY}}$ and $\overline{\text{XRDY}}$
HOLDA	$\overline{\text{HOLDA}}$	(X)RW	(X)R/$\overline{\text{W}}$, includes R/$\overline{\text{W}}$ and XR/$\overline{\text{W}}$

timing parameters for X2/CLKIN, H1, H3 (see Note 4, Figure 5, Figure 6, Figure 7 and Figure 8)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_{f(CI)}$	Fall time, CLKIN		5†		5†		5†	ns
2	$t_{w(CIL)}$	Pulse duration, CLKIN low, $t_{c(CI)}$ = MIN (see Note 7)	10.5		9		7		ns
3	$t_{w(CIH)}$	Pulse duration, CLKIN high, $t_{c(CI)}$ = MIN (see Note 7)	10.5		9		7		ns
4	$t_{r(CI)}$	Rise time, CLKIN		5†		5†		5†	ns
5	$t_{c(CI)}$	Cycle time, CLKIN	30	303	25	303	20	303	ns
6	$t_{f(H)}$	Fall time, H1/H3		3		3		3	ns
7	$t_{w(HL)}$	Pulse duration, H1/H3 low (see Note 8)	P – 6		P – 5		P – 5		ns
8	$t_{w(HH)}$	Pulse duration, H1/H3 high (see Note 8)	P – 7		P – 6		P – 6		ns
9	$t_{r(H)}$	Rise time, H1/H3		4		3		3	ns
9.1	$t_{d(HL-HH)}$	Delay time, from H1 low to H3 high or from H3 low to H1 high	0‡	5	0‡	4	0†	4	ns
10	$t_{c(H)}$	Cycle time, H1/H3	60	606	50	606	40	606	ns

† These values are derived by design but not tested.
‡ These values are derived from characterization but not tested.

NOTES: 4. All input and output voltage levels are TTL compatible.
7. Rise and fall times, assuming a 35 – 65% duty cycle, are incorporated within this specification (see NO TAG).
8. P = $t_{c(CI)}$

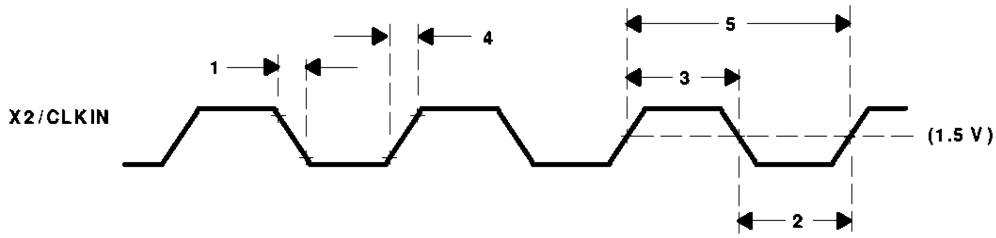


Figure 5. X2/CLKIN Timing

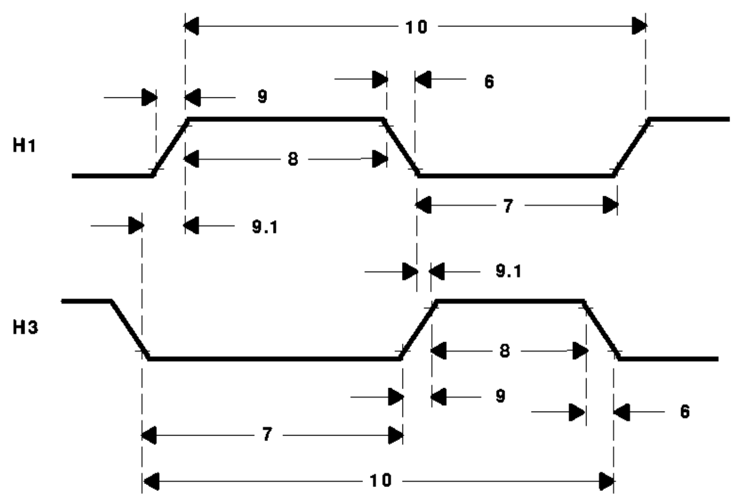


Figure 6. H1/H3 Timings

timing parameters for X2/CLKIN, H1, H3 (see Note 4, Figure 5, Figure 6, Figure 7 and Figure 8) (continued)

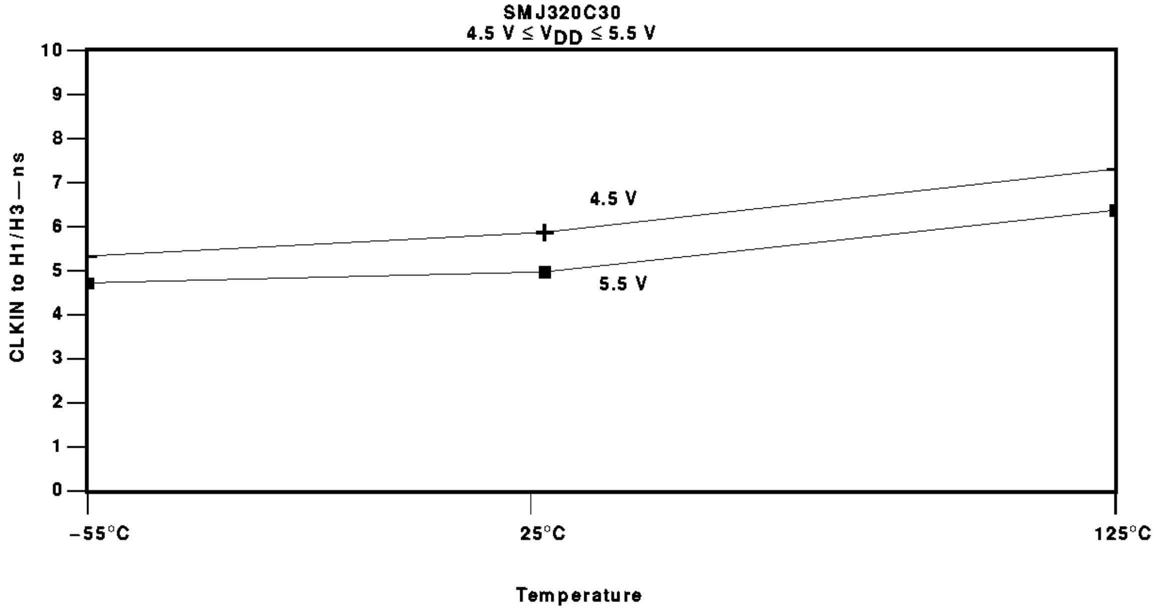


Figure 7. CLKIN to H1/H3 as a Function of Temperature
(Typical but not Guaranteed)

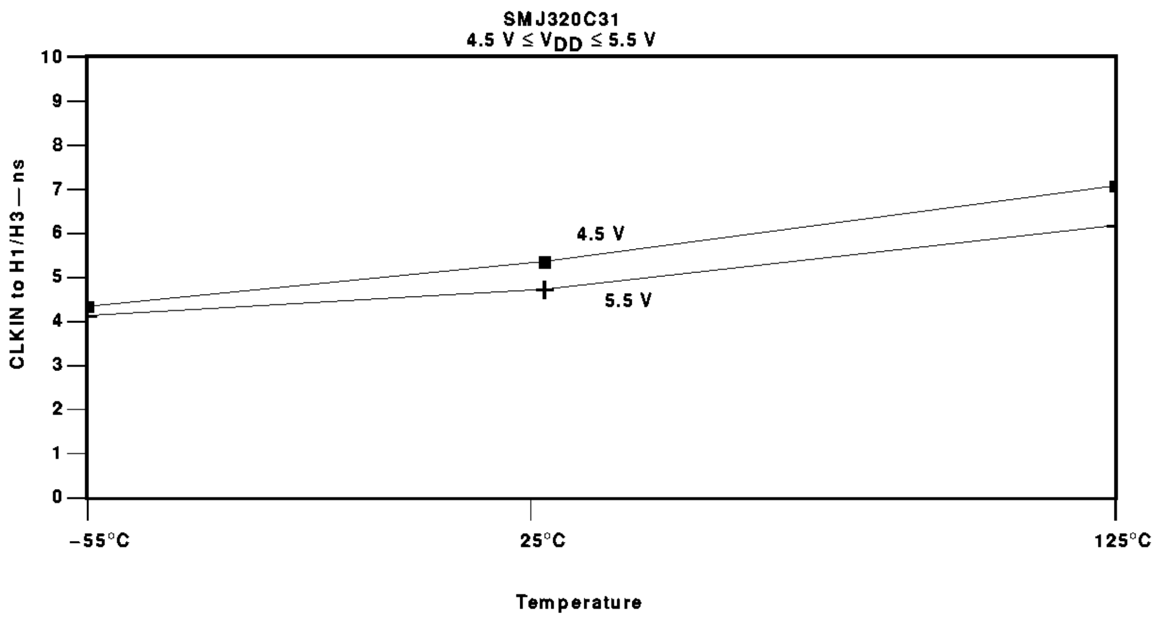


Figure 8. CLKIN to H1/H3 as a Function of Temperature
(Typical but not Guaranteed)

memory-read-cycle and memory-write-cycle timing [(M)STRB = 0] (see Figure 9 and Figure 10)

NO.			'320C30-33 '320C31-33		'320C30-40		'320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
11	$t_{d[H1L-(M)SL]}$	Delay time, H1 low to (M)STRB low	0†	10	0†	10	0†	6	0†	4	ns
12	$t_{d[H1L-(M)SH]}$	Delay time, H1 low to (M)STRB high	0†	10	0†	6	0†	6	0†	4	ns
13.1	$t_{d(H1H-RWL)}$	Delay time, H1 high to R/W low	0†	10	0†	9	0†	9	0†	7	ns
13.2	$t_{d[H1H-(X)RWL]}$	Delay time, H1 high to (X)R/W low	0†	15	0†	13	—		—		ns
14.1	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0†	14	0†	14	0†	10	0†	10	ns
14.2	$t_{d[H1L-(X)A]}$	Delay time, H1 low to (X)A valid	0†	10	0†	9	—		—		ns
15.1	$t_{su(D-H1L)R}$	Setup time, D valid before H1 low (read)	16		14		14		10		ns
15.2	$t_{su[(X)DR-H1L]R}$	Setup time, (X)D before H1 low (read)	18		16		—		—		ns
16	$t_{h[H1L-(X)D]R}$	Hold time, (X)D after H1 low (read)	0†		0†		0†		0†		ns
17.1	$t_{su(RDY-H1H)}$	Setup time, RDY before H1 high	8		8		8		6		ns
17.2	$t_{su[(X)RDY-H1H]}$	Setup time, (X)RDY before H1 high	9		9		—		—		ns
18	$t_{h[H1H-(X)RDY]}$	Hold time, (X)RDY after H1 high	0		0		0		0		ns
19	$t_{d[H1H-(X)RWH]W}$	Delay time, H1 high to (X)R/W high (write)		10		9		9		7	ns
20	$t_{v[H1L(X)D]W}$	Valid time, (X)D after H1 low (write)		20		17		17		14	ns
21	$t_{h[H1H-(X)D]W}$	Hold time, (X)D after H1 high (write)	0†		0†		0†		0†		ns
22.1	$t_{d(H1H-A)}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		18		15		15		14	ns
22.2	$t_{d[H1H-(X)A]}$	Delay time, H1 high to (X)A valid on back-to-back write cycles (write)		25		21	—		—		ns
26	$t_{d[A-(X)RDY]}$	Delay time, (X)RDY from A valid		8‡		7‡		7‡	§		ns

† These values are derived by design but not tested.
‡ These values are derived from characterization but not tested.
§ This value is frequency-dependent and can be calculated by: (delay, H1 low to H1 high) – (parameter 14.x) – (parameter 17.x)

memory-read-cycle and memory-write-cycle timing [($\overline{\text{(M)STRB}}$ = 0] (see Figure 9 and Figure 10) (continued)

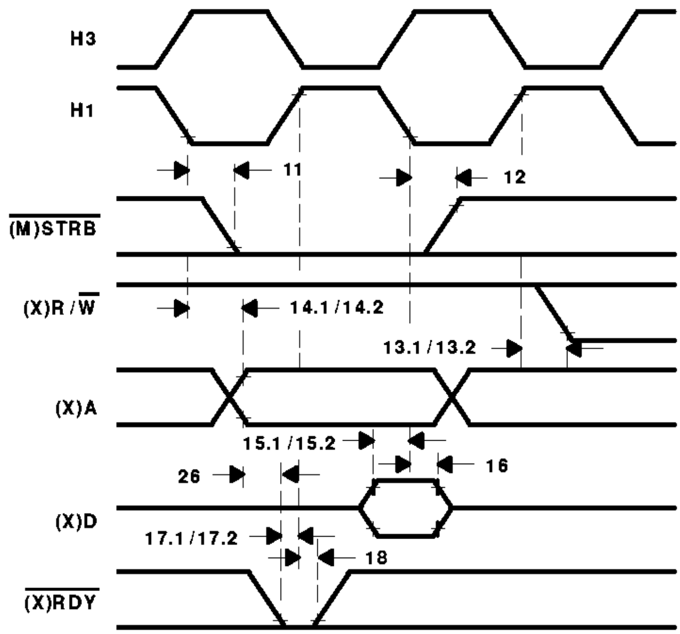


Figure 9. Memory-Read-Cycle Timing [$\overline{\text{(M)STRB}}$ = 0]

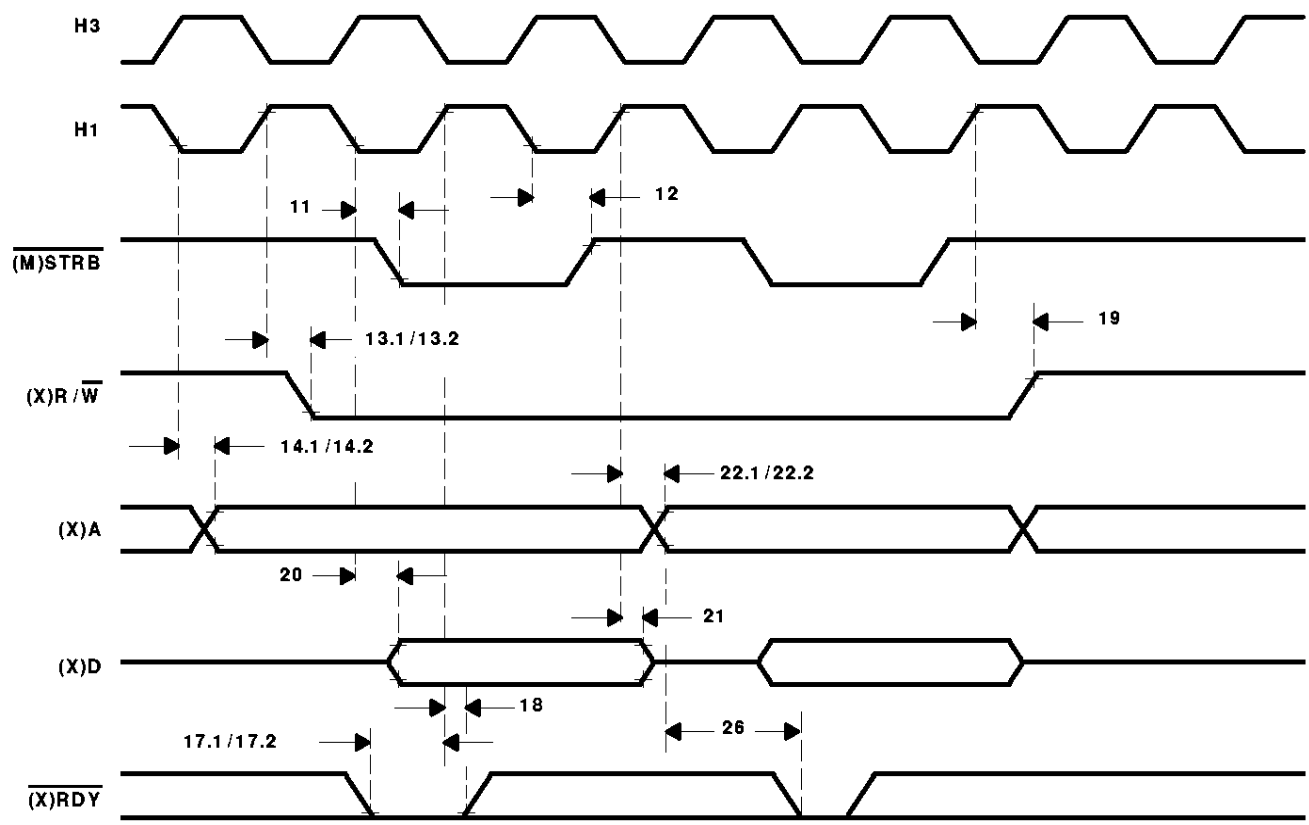


Figure 10. Memory-Write-Cycle Timing [$\overline{\text{(M)STRB}}$ = 0]

memory-read-cycle timing ($\overline{IOSTRB}$ = 0, SMJ320C30 only) (see Figure 11)

NO.			'320C30-33		'320C30-40		UNIT
			MIN	MAX	MIN	MAX	
27	$t_{d(H1H\text{-}IOSL)}$	Delay time, H1 high to $\overline{IOSTRB}$ low	0†	10	0†	9	ns
28	$t_{d(H1H\text{-}IOSH)}$	Delay time, H1 high to $\overline{IOSTRB}$ high	0†	10	0†	9	ns
29	$t_{d[H1L\text{-}(X)RWH]}$	Delay time, H1 low to (X)R/$\overline{W}$ high	0†	10	0†	9	ns
30	$t_{d[H1L\text{-}(X)A]}$	Delay time, H1 low to (X)A valid	0†	10	0†	9	ns
31	$t_{su[(X)D\text{-}H1H]R}$	Setup time, (X)D before H1 high	15		13		ns
32	$t_{h[H1H\text{-}(X)D]R}$	Hold time, (X)D after H1 high	0‡		0‡		ns
33	$t_{su[(X)RDY\text{-}H1H]}$	Setup time, $\overline{(X)RDY}$ before H1 high	9		9		ns
34	$t_{h[H1H\text{-}(X)RDY]}$	Hold time, $\overline{(X)RDY}$ after H1 high	0		0		ns

† These values are derived by design but not tested.
‡ These values are derived from characterization but not tested.

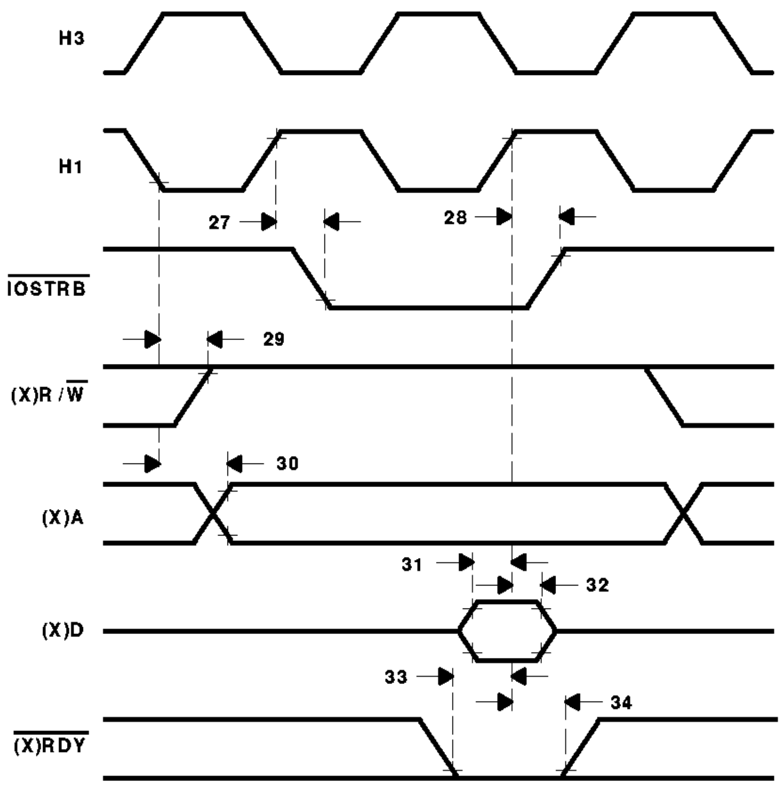


Figure 11. SMJ320C30 Memory-Read-Cycle Timing ($\overline{IOSTRB}$ = 0)

memory-write-cycle timing ($\overline{\text{IOSTRB}}$ = 0, SMJ320C30 only) (see Figure 12)

NO.			'320C30-33		'320C30-40		UNIT
			MIN	MAX	MIN	MAX	
27	$t_{d(H1H\text{-}IOSL)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ low	0†	10	0†	9	ns
28	$t_{d(H1H\text{-}IOSH)}$	Delay time, H1 high to $\overline{\text{IOSTRB}}$ high	0†	10	0†	9	ns
29	$t_{d[H1L\text{-}(X)RWH]}$	Delay time, H1 low to (X)R/$\overline{\text{W}}$ high	0†	10	0†	9	ns
30	$t_{d[H1L\text{-}(X)A]}$	Delay time, H1 low to (X)A valid	0†	10	0†	9	ns
33	$t_{su[(X)RDY\text{-}H1H]}$	Setup time, $\overline{\text{(X)RDY}}$ before H1 high	9		9		ns
34	$t_{h[H1H\text{-}(X)RDY]}$	Hold time, $\overline{\text{(X)RDY}}$ after H1 high	0		0		ns
35	$t_{d(H1L\text{-}XRWL)}$	Delay time, H1 low to XR/$\overline{\text{W}}$ low	0†	15	0†	13	ns
36	$t_{v[H1H(X)D]W}$	Valid time, (X)D after H1 high		30		25	ns
37	$t_{h[H1L\text{-}(X)D]W}$	Hold time, (X)D after H1 low	0		0		ns

† These values are derived by design but not tested.

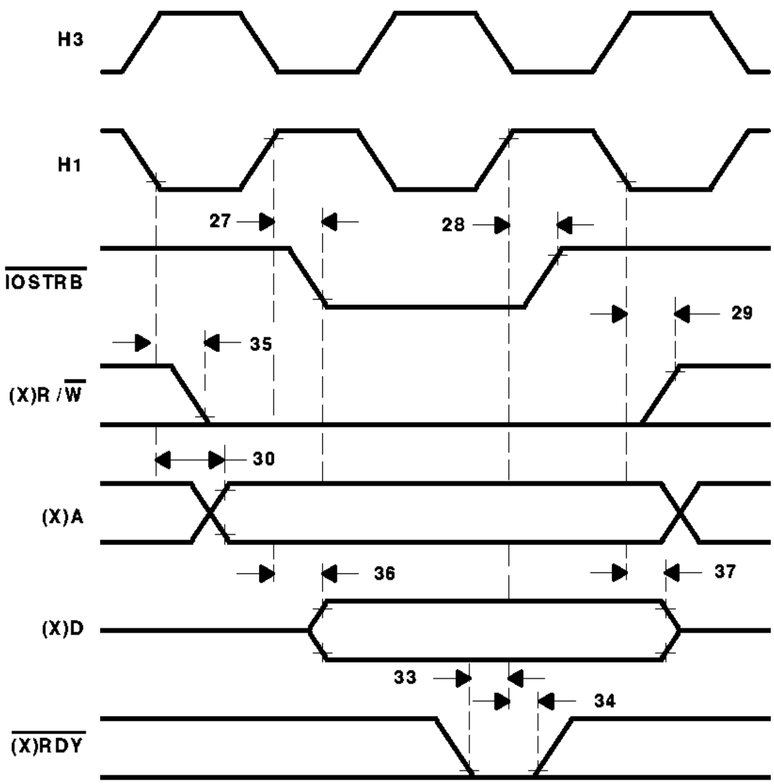


Figure 12. SMJ320C30 Memory-Write-Cycle Timing ($\overline{\text{IOSTRB}}$ = 0)

timing for XF0 and XF1 when executing LDFI or LDII (see Figure 13)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
38	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		15		13		12	ns
39	$t_{su(XF1-H1L)}$	Setup time, XF1 valid before H1 low	12		9		8		ns
40	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		ns

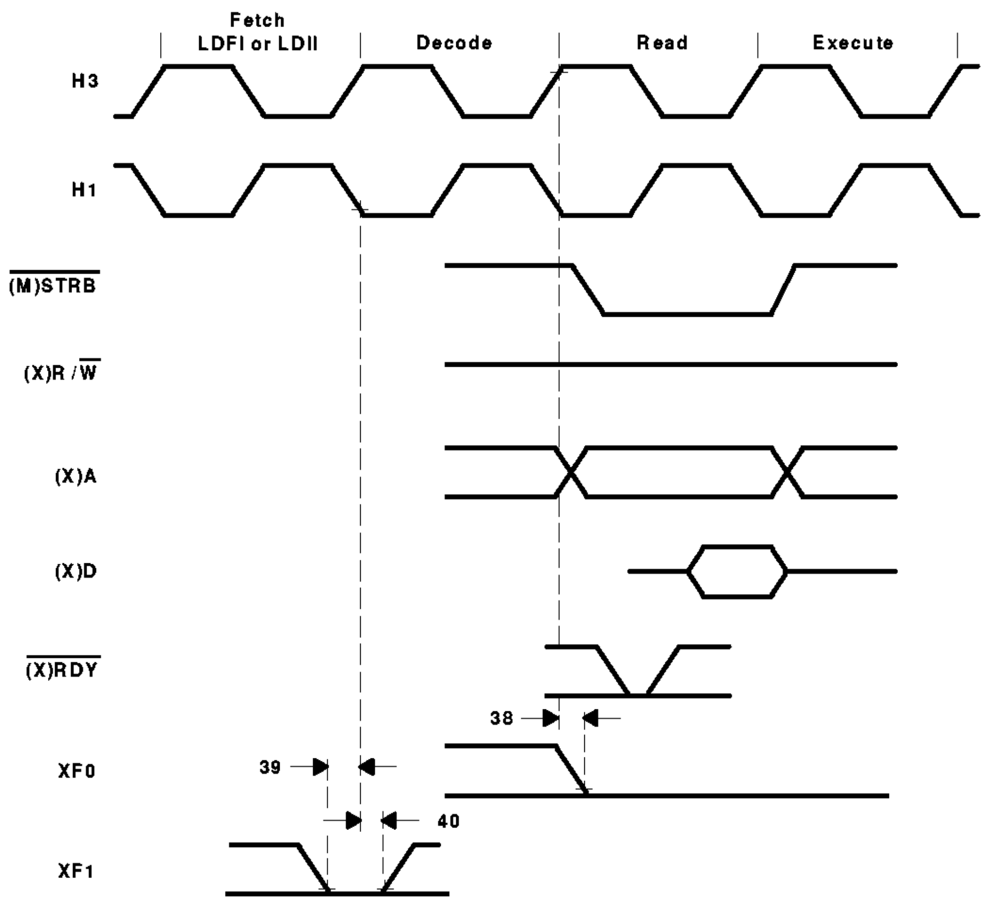


Figure 13. Timing for XF0 and XF1 When Executing LDFI or LDI

timing for XF0 when executing a STFI or STII (see Figure 14)

NO.		’320C30-33 ’320C31-33		’320C30-40 ’320C31-40		’320C31-50		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
41	$t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high		18		13		12	ns

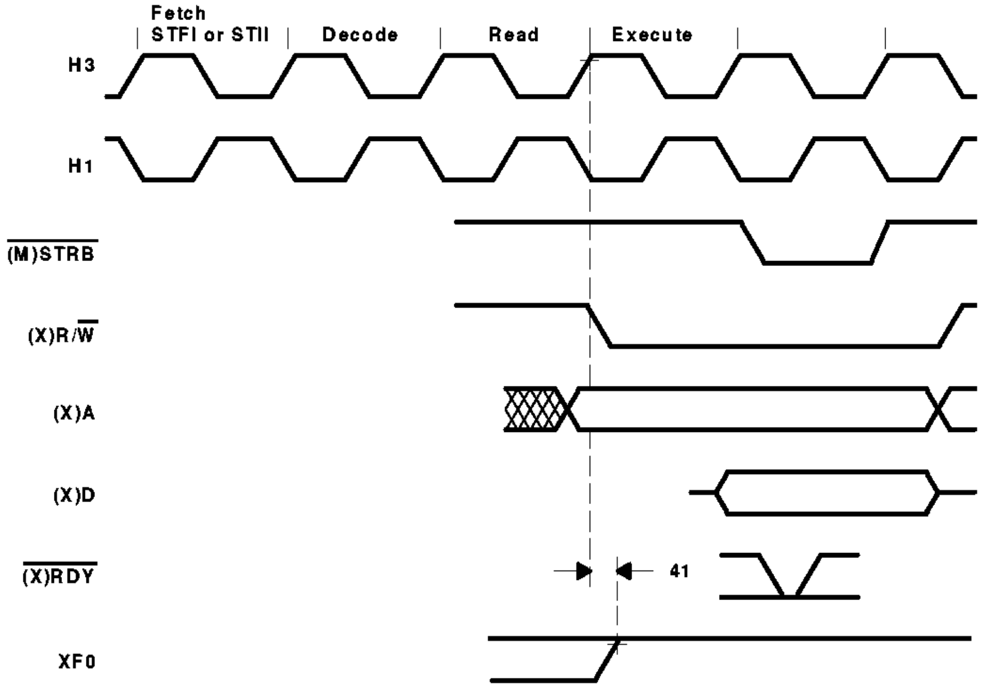


Figure 14. Timing for XF0 When Executing a STFI or STII

timing for XF0 and XF1 when executing SIGI (see Figure 15)

NO.			’320C30-33 ’320C31-33		’320C30-40 ’320C31-40		’320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
41.1	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		15		13		12	ns
42	$t_{d(H3H-XF0H)}$	Delay time, H3 high to XF0 high		18		13		12	ns
43	$t_{su(XF1-H1L)}$	Setup time, XF1 valid before H1 low	12		9		8		ns
44	$t_{h(H1L-XF1)}$	Hold time, XF1 after H1 low	0		0		0		ns

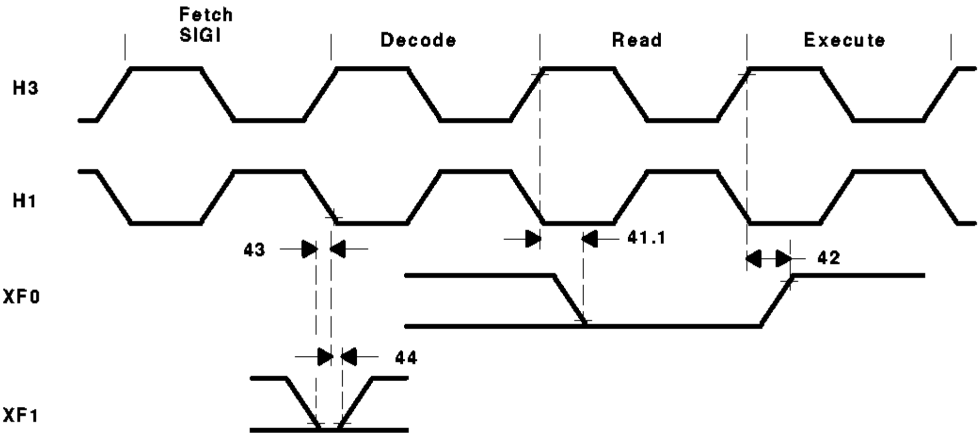


Figure 15. Timing for XF0 and XF1 When Executing SIGI

timing for loading XF register when configured as an output (see Figure 16)

NO.			’320C30-33 ’320C31-33		’320C30-40 ’320C31-40		’320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
45	$t_{v(H3H-XF)}$	Valid time, H3 high to XF valid		15		13		12	ns

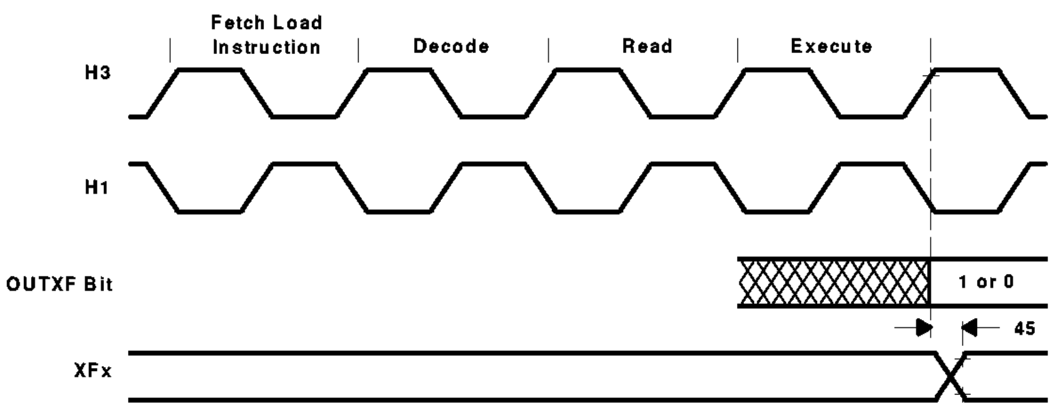
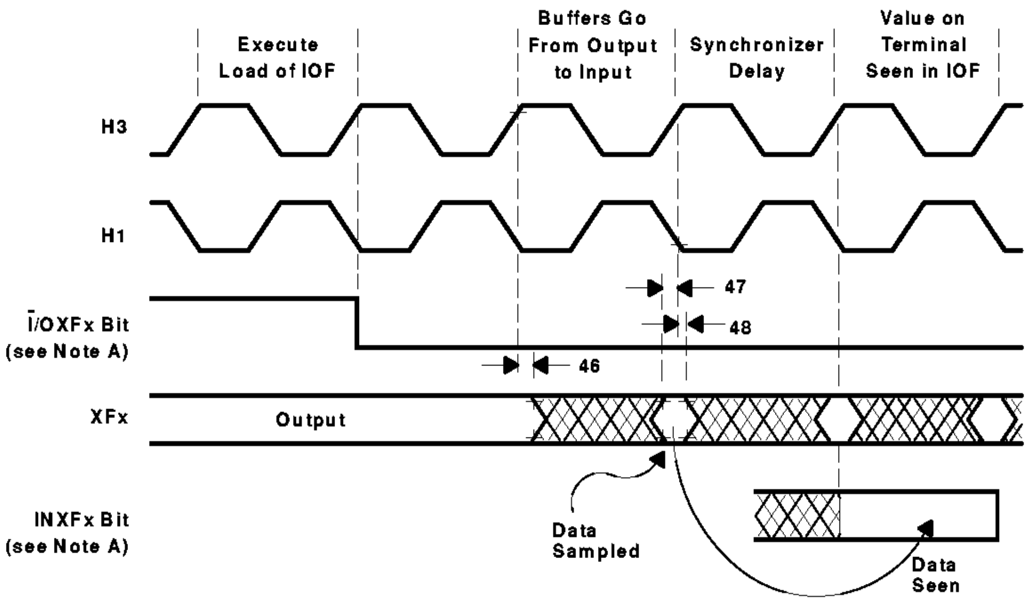


Figure 16. Timing for Loading XF Register When Configured as an Output

change of XFx from output to input mode (see Figure 17)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
46	$t_{d(H3H-XFx)}$	Delay time, XFx after H3 high		15†		13†		12†	ns
47	$t_{su(XFx-H1L)}$	Setup time, XFx before H1 low	12		9		8		ns
48	$t_{h(H1L-XFx)}$	Hold time, XFx after H1 low	0		0		0		ns

† These values are derived from characterization but not tested.

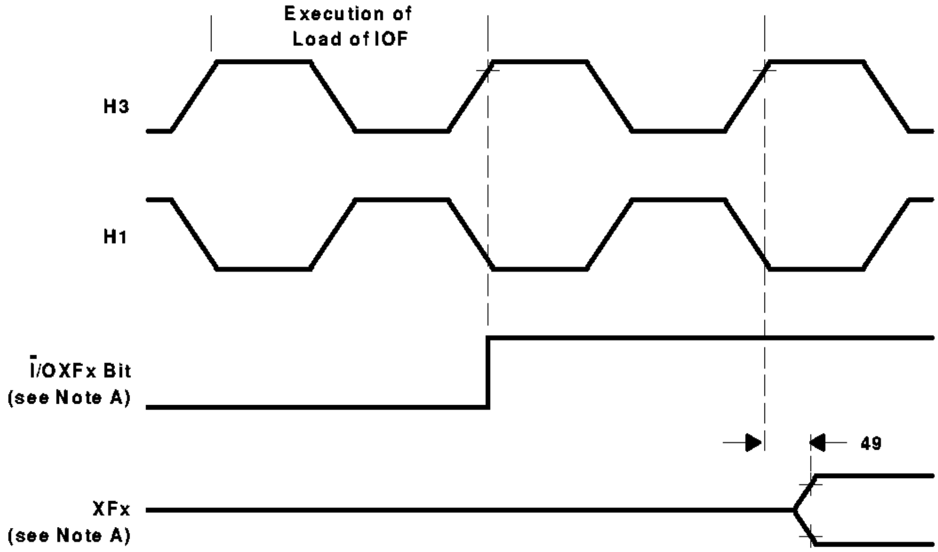


NOTE A: Ī/OXFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register depending on whether XF0 or XF1, respectively, is being affected.

Figure 17. Change of XFx From Output to Input Mode

change of XFx from input to output mode (see Figure 18)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
49	$t_{d(H3H-XFIO)}$	Delay time, H3 high to XF switching from input to output		20		17		15	ns



NOTE A: I/OXFx represents either bit 1 or bit 5 of the IOF register, and INXFx represents either bit 3 or bit 7 of the IOF register depending on whether XF0 or XF1, respectively, is being affected.

Figure 18. Change of XFx From Input to Output Mode

reset timing

RESET is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 19 occurs; otherwise, an additional delay of one clock cycle may occur. R/W and XR/W are in the high-impedance state during reset and can be provided with a resistive pullup, nominally 18 kΩ to 22 kΩ, to prevent spurious writes from occurring. The asynchronous reset signals include XF0/1, CLKX0/1, DX0/1, FSX0/1, CLKR0/1, DR0/1, FSR0/1, and TCLK0/1. HOLD is an asynchronous input and can be asserted during reset.

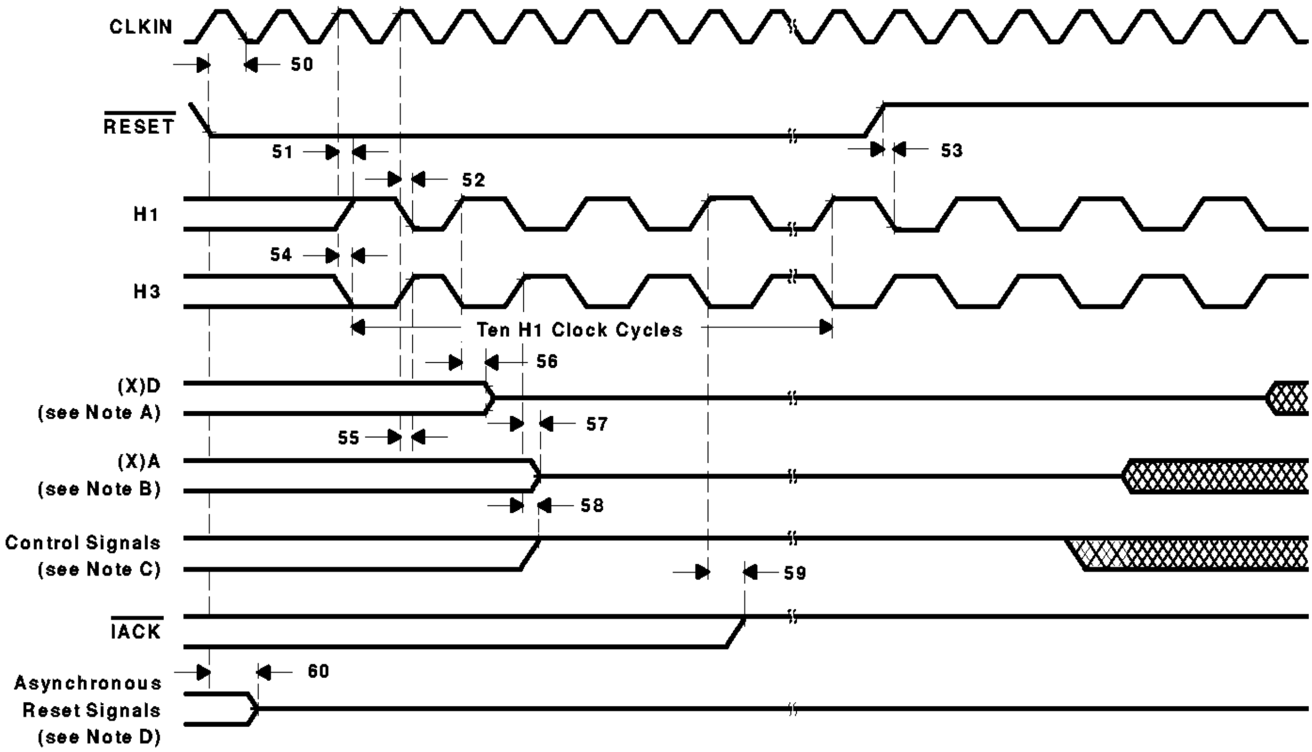
Resetting the device initializes the primary- and expansion-bus control registers to seven software wait states and, therefore, results in slow external accesses until these registers are initialized.

reset timing [P = $t_{c(CI)}$] (see Figure 19)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
50	$t_{su(RESET)}$	Setup time, RESET before CLKIN low	10	P†	10	P‡	10	P‡	ns
51	$t_{d(CLKINH-H1H)}$	Delay time, CLKIN high to H1 high§	2	14	2	14	2	10	ns
52	$t_{d(CLKINH-H1L)}$	Delay time, CLKIN high to H1 low§	2	14	2	14	2	10	ns
53	$t_{su(RESETH-H1L)}$	Setup time, RESET high before H1 low after ten H1 clock cycles	10		9		7		ns
54	$t_{d(CLKINH-H3L)}$	Delay time, CLKIN high to H3 low§	2	14	2	14	2	10	ns
55	$t_{d(CLKINH-H3H)}$	Delay time, CLKIN high to H3 high§	2	14	2	14	2	10	ns
56	$t_{dis(H1H-XD)}$	Disable time, H1 high to (X)D high-impedance state		18†		15†		12†	ns
57	$t_{dis(H3H-XA)}$	Disable time, H3 high to (X)A high-impedance state		10†		9†		8†	ns
58	$t_{d(H3H-CONTROLH)}$	Delay time, H3 high to control signals high		10†		9†		8†	ns
59	$t_{d(H1H-IACKH)}$	Delay time, H1 high to IACK high		10†		9†		8†	ns
60	$t_{dis(RESETL-ASYNCH)}$	Disable time, RESET low to asynchronous reset signals in the high-impedance state		25†		21†		17†	ns

† These values are derived from characterization but not tested.
‡ These values are derived by design but not tested.
§ See Figure 7 and Figure 8 for temperature dependence for the 40-MHz SMJ320C30 and SMJ320C31.

reset timing (continued)



NOTES: A. In this diagram X(D) includes D31–D0 and XD31–XD0.
B. In this diagram, (X)A includes A23–A0 and XA12–XA0.
C. Control signals include STRB, MSTRB, and IOSTRB.
D. Asynchronous reset signals include XF1, XF0, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, CLKX1, DX1, FSX1, CLKR1, DR1, FSR1, TCLK0, and TCLK1.
E. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In micromputer mode, the reset vector is fetched twice, with no software wait states.

Figure 19. Reset Timing [P = $t_{c(CI)}$]

$\overline{INT3}$–$\overline{INT0}$ response timing [Q = $t_{c(H)}$] (see Figure 20)

NO.			'320C30-33 '320C31-33 MIN	'320C30-33 '320C31-33 MAX	'320C30-40 '320C31-40 MIN	'320C30-40 '320C31-40 MAX	'320C31-50 MIN	'320C31-50 MAX	UNIT
61	$t_{su(INT)}$	Setup time, $\overline{INT3}$–$\overline{INT0}$ before H1 low	15		13		11		ns
62	$t_{w(INT)}$	Pulse duration, $\overline{INT3}$–$\overline{INT0}$, to assure only one interrupt seen (see Notes 9 and 10)	Q	< 2Q†	Q	< 2Q†	Q	< 2Q†	ns

† These values derived from characterization but not tested.

NOTES: 9. Interrupt pulse duration must be at least 1Q wide to ensure it is seen. It must be less than 2Q wide to ensure it is responded to only once.

10. $\overline{INT3}$–$\overline{INT0}$ are asynchronous inputs and can be asserted at any point during a clock cycle. The SMJ320C3x interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to a minimum of one H1 falling edge and no more than two H1 falling edges. The SMJ320C3x can accept an interrupt from the same source every two H1 clock cycles. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle may occur.

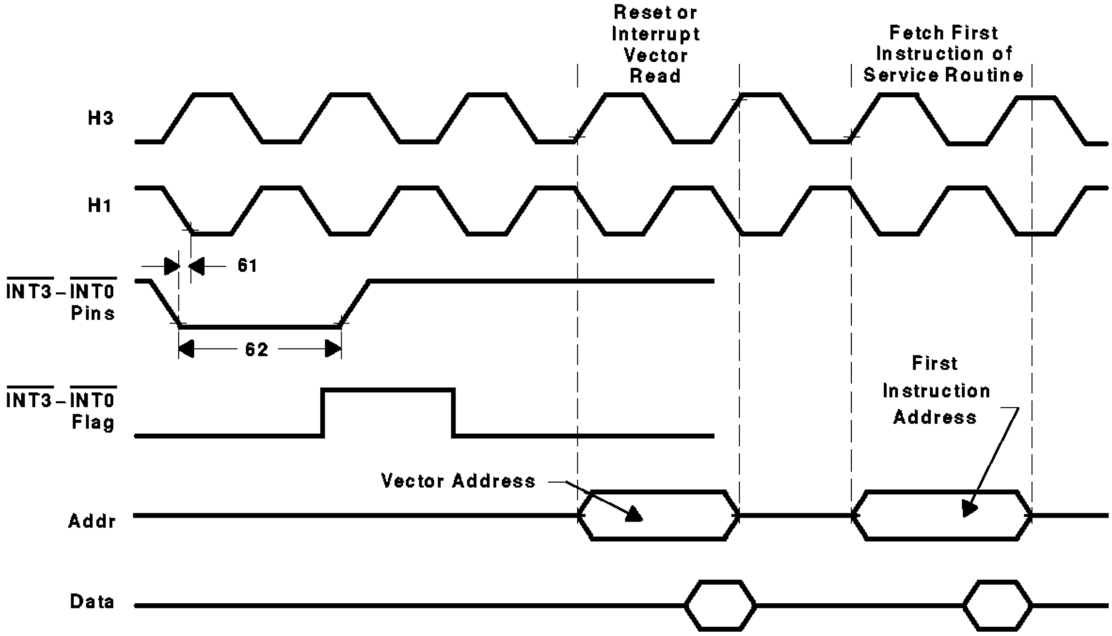


Figure 20. $\overline{INT3}$–$\overline{INT0}$ Response Timing [Q = $t_{c(H)}$]

interrupt-acknowledge ($\overline{IACK}$) timing (see Figure 21)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
63	$t_{d(H1H-IACKL)}$	Delay time, H1 high to $\overline{IACK}$ low		10		9		8	ns
64	$t_{d(H1H-IACKH)}$	Delay time, H1 high to $\overline{IACK}$ high		10		9		8	ns

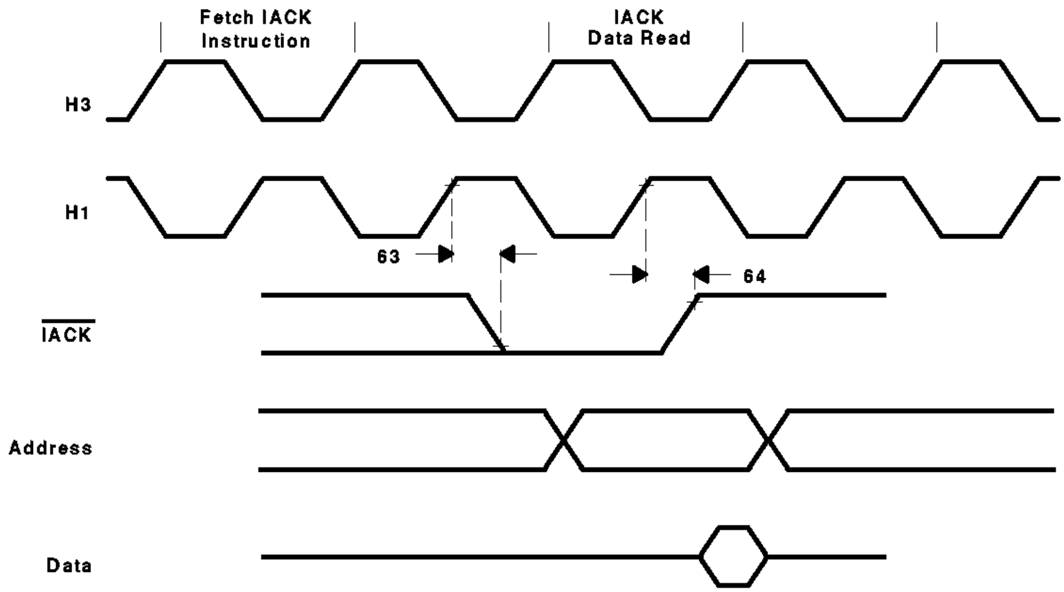


Figure 21. Interrupt-Acknowledge ($\overline{IACK}$) Timing

serial-port timing (see Figure 22 and Figure 23)

NO.			CLOCK SOURCE	'320C30-33 '320C31-33 MIN	'320C30-33 '320C31-33 MAX	'320C30-40 '320C31-40 MIN	'320C30-40 '320C31-40 MAX	UNIT
65	$t_{d(H1\text{-}SCK)}$	Delay time, H1 high to internal CLKX/R			15		13	ns
66	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)} \times 2.5$†		$t_{c(H)} \times 2.5$†		ns
			CLKX/R int	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$‡	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$‡	
67	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}+12$†		$t_{c(H)}+12$†		ns
			CLKX/R int	$[t_{c(SCK)}/2]-15$	$[t_{c(SCK)}/2]+5$	$[t_{c(SCK)}/2]-15$	$[t_{c(SCK)}/2]+5$	
68	$t_{r(SCK)}$	Rise time, CLKX/R			8†		7†	ns
69	$t_{f(SCK)}$	Fall time, CLKX/R			8†		7†	ns
70	$t_{d(DX)}$	Delay time, CLKX to DX valid	CLKX ext		35		30	ns
			CLKX int		20		17	
71	$t_{su(DR)}$	Setup time, DR before CLKR low	CLKR ext	10		9		ns
			CLKR int	25		21		
72	$t_{h(DR)}$	Hold time, DR from CLKR low	CLKR ext	10		9		ns
			CLKR int	0†		0		
73	$t_{d(FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		32		27	ns
			CLKX int		17		15	
74	$t_{su(FSR)}$	Setup time, FSR before CLKR low	CLKR ext	10		9		ns
			CLKR int	10		9		
75	$t_{h(FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	10		9		ns
			CLKX/R int	0		0		
76	$t_{su(FSX)}$	Setup time, external FSX before CLKX	CLKX ext	$-[t_{c(H)}-8]$	$[t_{c(SCK)}/2]-10$‡	$-[t_{c(H)}-8]$	$[t_{c(SCK)}/2]-10$‡	ns
			CLKX int	$-[t_{c(H)}-21]$	$t_{c(SCK)}/2$‡	$-[t_{c(H)}-21]$	$t_{c(SCK)}/2$‡	
77	$t_{d(CH\text{-}DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		36		30	ns
			CLKX int		21		18	
78	$t_{d(FSX\text{-}DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			36		30	ns
79	t_{dDXZ}	Delay time, CLKX high to DX high impedance following last data bit			20†		17†	ns

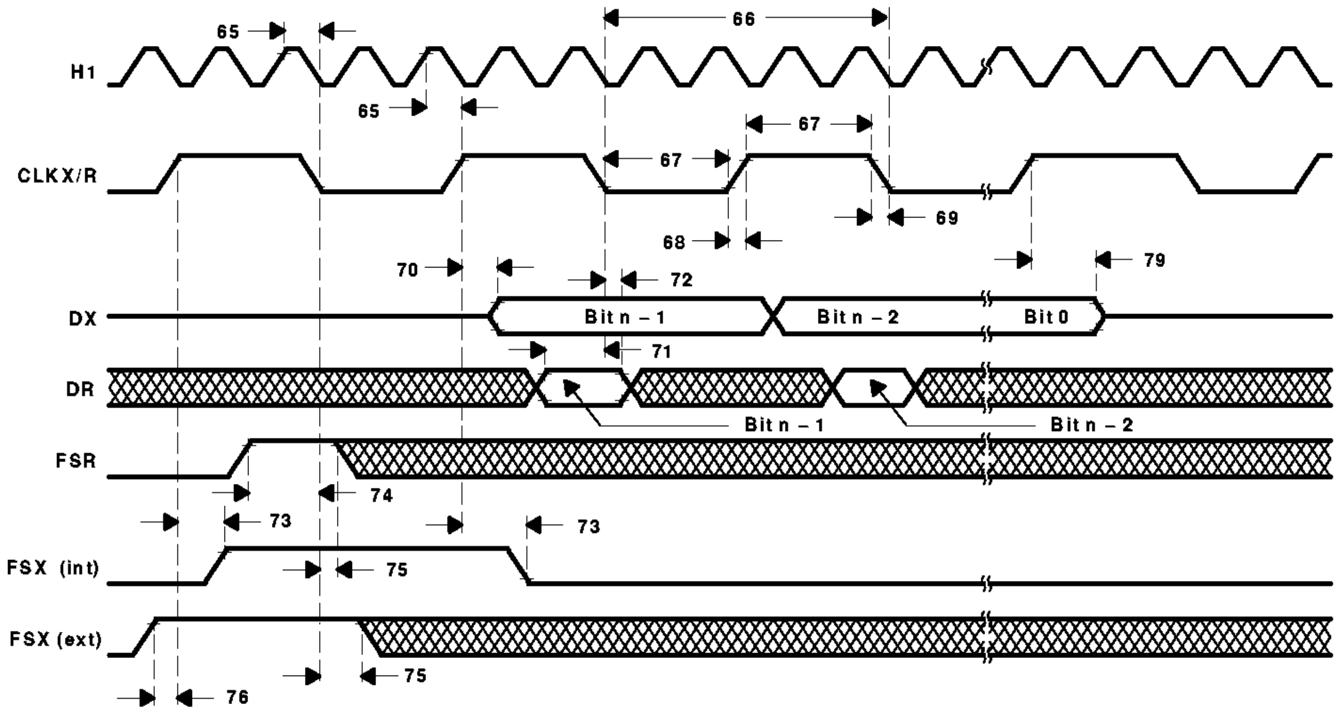
† These values are derived from characterization but not tested.
‡ These values are derived by design but not tested.

serial-port timing (see Figure 22 and Figure 23) (continued)

NO.			CLOCK SOURCE	'320C31-50 MIN	'320C31-50 MAX	UNIT
65	$t_{d(H1\text{-}SCK)}$	Delay time, H1 high to internal CLKX/R			10	ns
66	$t_{c(SCK)}$	Cycle time, CLKX/R	CLKX/R ext	$t_{c(H)} \times 2.5$		ns
			CLKX/R int	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$‡	
67	$t_{w(SCK)}$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_{c(H)}+10$†		ns
			CLKX/R int	$[t_{c(SCK)}/2]-5$	$[t_{c(SCK)}/2]+5$	
68	$t_{r(SCK)}$	Rise time, CLKX/R			6†	ns
69	$t_{f(SCK)}$	Fall time, CLKX/R			6†	ns
70	$t_{d(DX)}$	Delay time, CLKX to DX valid	CLKX ext		24	ns
			CLKX int		16	
71	$t_{su(DR)}$	Setup time, DR before CLKR low	CLKR ext	9		ns
			CLKR int	17		
72	$t_{h(DR)}$	Hold time, DR from CLKR low	CLKR ext	7		ns
			CLKR int	0†		
73	$t_{d(FSX)}$	Delay time, CLKX to internal FSX high/low	CLKX ext		22	ns
			CLKX int		15	
74	$t_{su(FSR)}$	Setup time, FSR before CLKR low	CLKR ext	7		ns
			CLKR int	7		
75	$t_{h(FS)}$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	7		ns
			CLKX/R int	0		
76	$t_{su(FSX)}$	Setup time, external FSX before CLKX	CLKX ext	$-[t_{c(H)}-8]$	$[t_{c(SCK)}/2]-10$‡	ns
			CLKX int	$-[t_{c(H)}-21]$	$t_{c(SCK)}/2$‡	
77	$t_{d(CH\text{-}DX)V}$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext		24	ns
			CLKX int		14	
78	$t_{d(FSX\text{-}DX)V}$	Delay time, FSX to first DX bit, CLKX precedes FSX			24	ns
79	t_{dDXZ}	Delay time, CLKX high to DX high impedance following last data bit			15†	ns

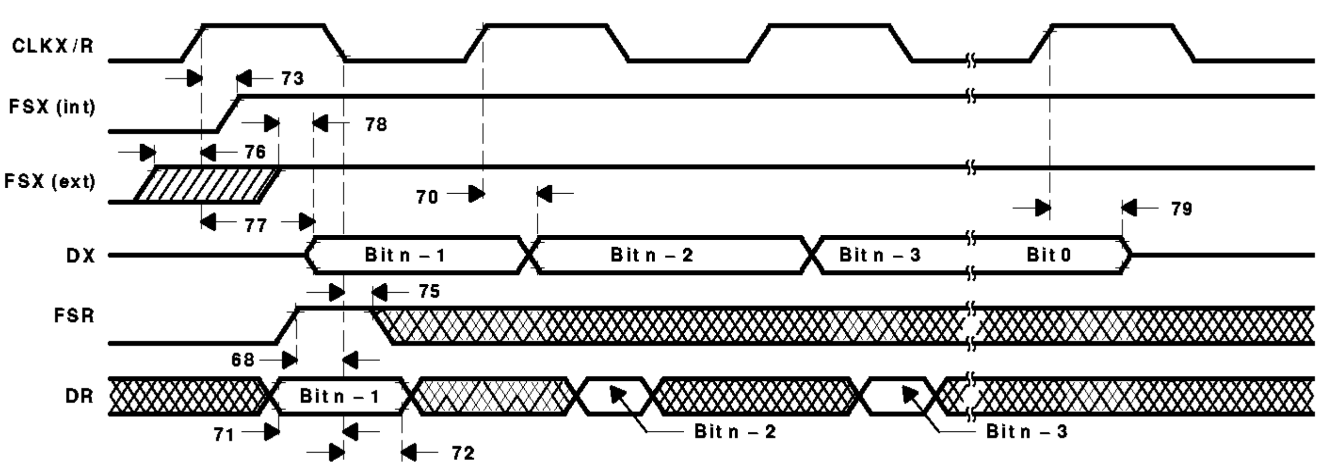
† These values are derived from characterization but not tested.
‡ These values are derived by design but not tested.

serial-port timing (continued)



NOTES: A. Timing diagrams show operations with the serial port global-control register bits CLKXP = CLKRP = FSXP = FSRP = 0.
B. These timings are valid for all serial-port modes, including handshake, except where otherwise indicated. For a functional description of serial port operation, refer to the *TMS320C3x User's Guide* (literature number SPRU031D).
C. Timing diagrams depend upon the length of the serial-port word, n, where n = 8, 16, 24, or 32 bits, respectively.

Figure 22. Serial-Port Timing, Fixed-Data-Rate Mode



NOTES: A. Timing diagrams show operations with the serial port global-control register bits CLKXP = CLKRP = FSXP = FSRP = 0.
B. These timings are valid for all serial-port modes, including handshake, except where otherwise indicated.
C. Timings not expressly specified for variable-data-rate mode are the same as those for fixed-data-rate mode.
D. Timing diagrams depend upon the length of the serial-port word, n, where n = 8, 16, 24, or 32 bits, respectively.

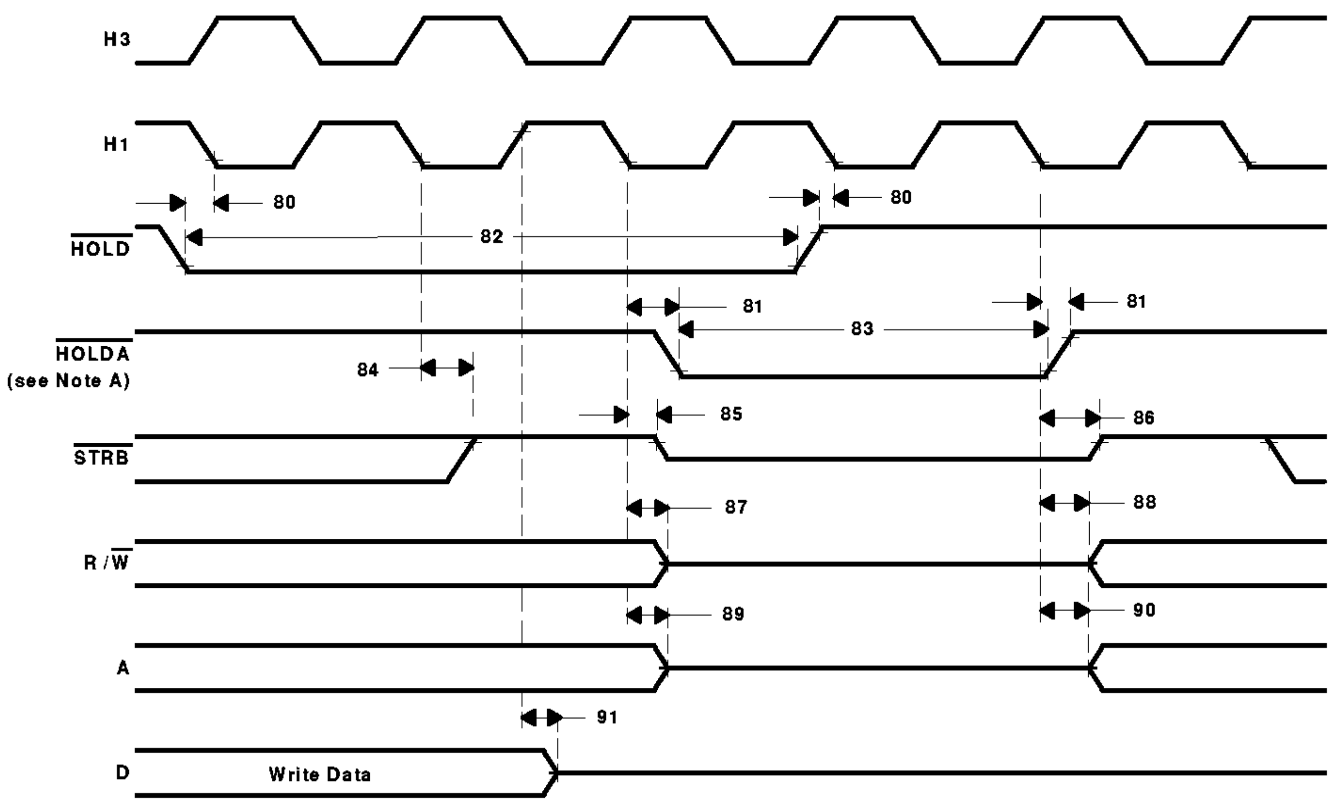
Figure 23. Serial-Port Timing, Variable-Data-Rate Mode

$\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ timing (see Note 11 and Figure 24)

NO.			’320C30-33 ’320C31-33		’320C30-40 ’320C31-40		’320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
80	$t_{su(HOLD)}$	Setup time, $\overline{\text{HOLD}}$ before H1 low	15		13		10		ns
81	$t_{v(HOLDA)}$	Valid time, $\overline{\text{HOLDA}}$ after H1 low	0†	10	0‡	9	0‡	7	ns
82	$t_{w(HOLD)}$	Pulse duration, $\overline{\text{HOLD}}$ low	$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		ns
83	$t_{w(HOLDA)}$	Pulse duration, $\overline{\text{HOLDA}}$ low	$t_{c(H)}-5$‡		$t_{c(H)}-5$‡		32‡		ns
84	$t_{d(H1L-SH)H}$	Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	0†	10‡	0†	9‡	0†	7‡	ns
85	$t_{dis(H1L-S)}$	Disable time, H1 low to $\overline{\text{STRB}}$ high impedance	0†	10‡	0†	9‡	0†	7‡	ns
86	$t_{en(H1L-S)}$	Enable time, H1 low to $\overline{\text{STRB}}$ active	0†	10‡	0†	9‡	0†	7‡	ns
87	$t_{dis(H1L-RW)}$	Disable time, H1 low to R/$\overline{\text{W}}$ high impedance	0†	10‡	0†	9‡	0†	8‡	ns
88	$t_{en(H1L-RW)}$	Enable time, H1 low to R/$\overline{\text{W}}$ active	0†	10‡	0†	9‡	0†	7‡	ns
89	$t_{dis(H1L-A)}$	Disable time, H1 low to address high impedance	0†	10‡	0†	9‡	0†	8‡	ns
90	$t_{en(H1L-A)}$	Enable time, H1 low to address valid	0†	15‡	0†	13‡	0†	10‡	ns
91	$t_{dis(H1H-D)}$	Disable time, H1 high to data high impedance	0†	15‡	0†	12‡	0†	10‡	ns

† These values are derived by design but not tested.
‡ These values are derived from characterization but not tested.

NOTE 11: $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 24 occurs; otherwise, an additional delay of one clock cycle can occur. The $\overline{\text{NOHOLD}}$ bit of the primary-bus-control register (refer to the *TMS320C3x User's Guide*, literature number SPRU031D) overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles from occurring.



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low through one H1 cycle after $\overline{\text{HOLD}}$ returns to high.

Figure 24. $\overline{\text{HOLD}}$/$\overline{\text{HOLDA}}$ Timing

peripheral-pin general-purpose I/O timing (see Note 12 and Figure 25)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
92	$t_{su(GPIOH1L)}$	Setup time, general-purpose input before H1 low	12		10		9		ns
93	$t_{h(GPIOH1L)}$	Hold time, general-purpose input after H1 low	0		0		0		ns
94	$t_{d(GPIOH1H)}$	Delay time, general-purpose output after H1 high		15		13		10	ns

NOTE 12: Peripheral pins include CLKX0/1, CLKR0/1, DX0/1, DR0/1, FSX0/1, FSR0/1, and TCLK0/1. The modes of these pins are defined by the contents of internal control registers associated with each peripheral.

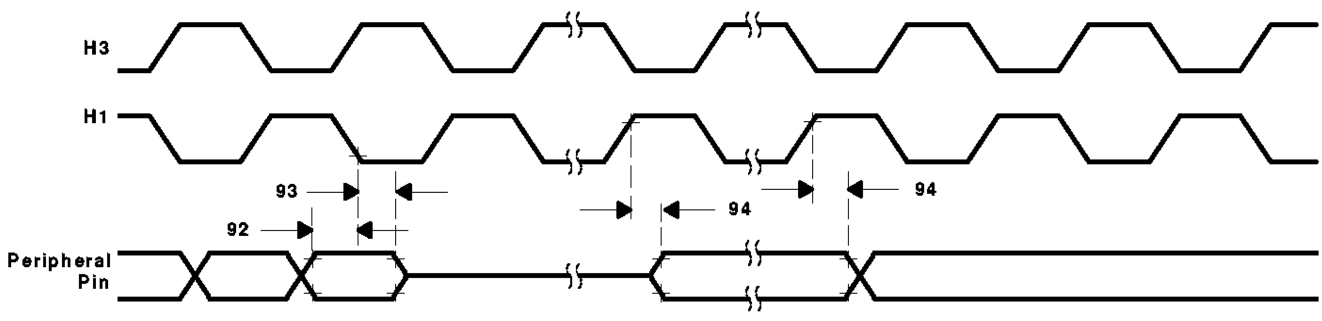


Figure 25. Peripheral-Pin General-Purpose I/O Timing

change of peripheral pin from general-purpose output to input mode (see Figure 26)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
95	$t_{h(H1H)}$	Hold time after H1 high		15		13		10	ns
96	$t_{su(GPIOH1L)}$	Setup time, peripheral pin before H1 low	12		9		9		ns
97	$t_{h(GPIOH1L)}$	Hold time, peripheral pin after H1 low	0		0		0		ns

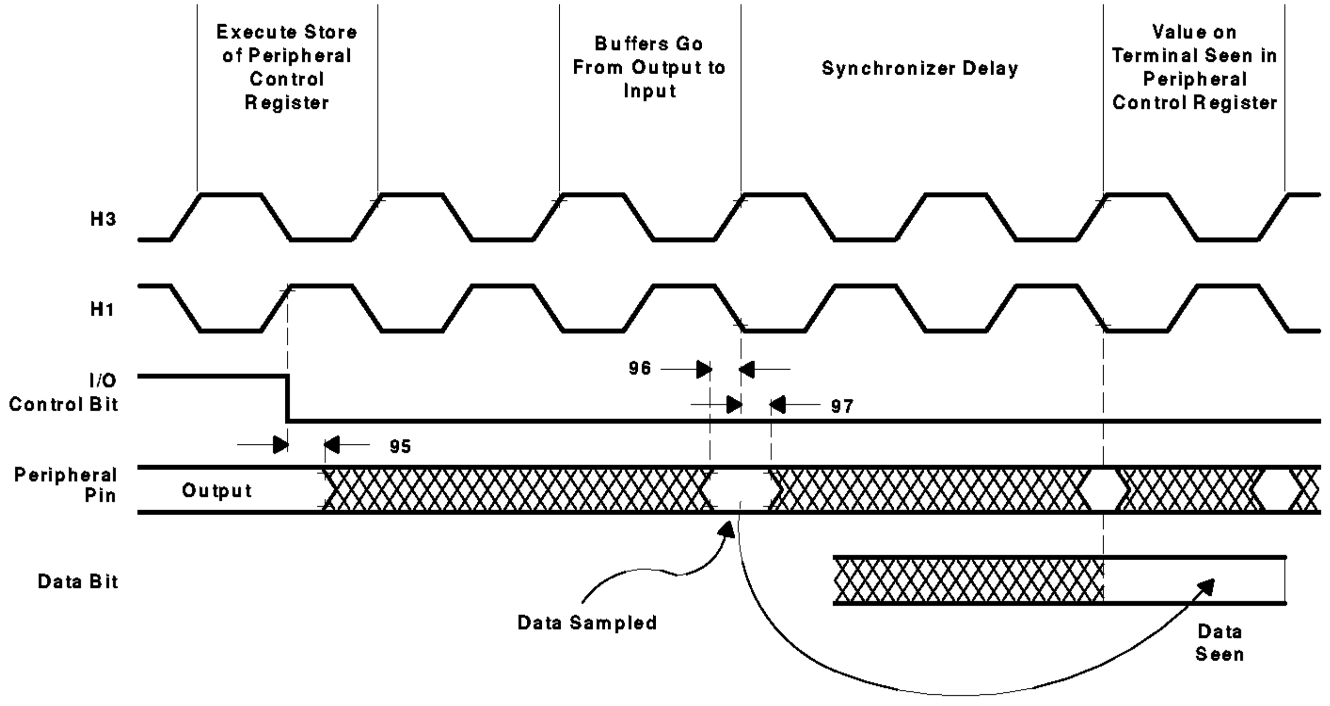


Figure 26. Change of Peripheral Pin From General-Purpose Output to Input Mode

change of peripheral pin from general-purpose input to output mode (see Figure 27)

NO.			'320C30-33 '320C31-33		'320C30-40 '320C31-40		'320C31-50		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
98	$t_{d(GPIOH1H)}$	Delay time, H1 high to peripheral pin switching from input to output		15		13		10	ns

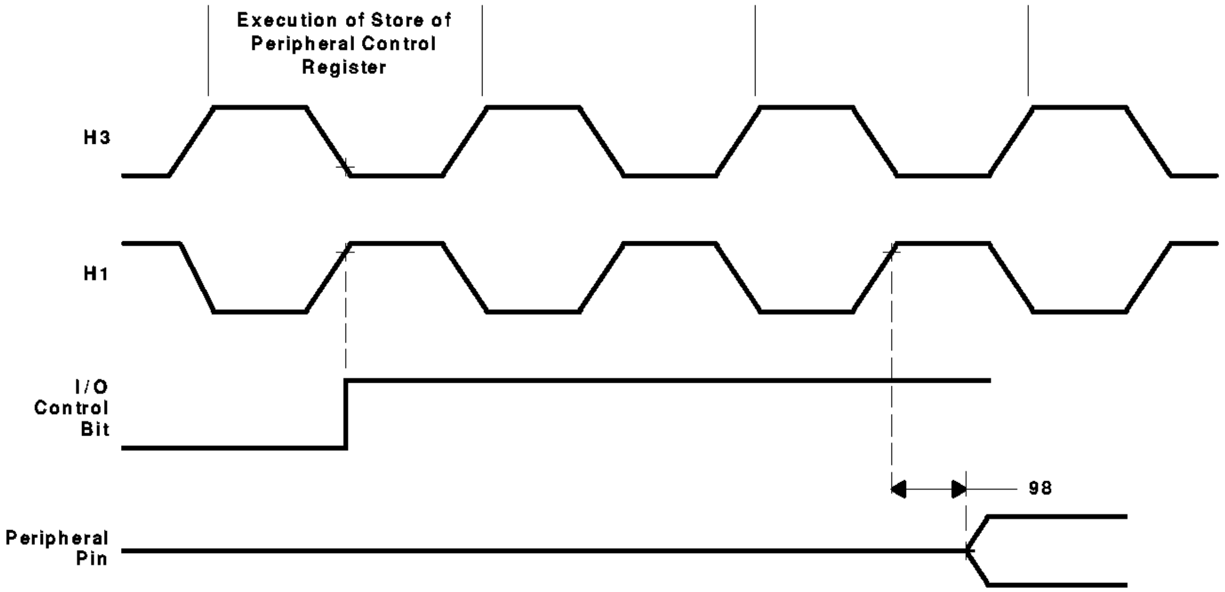


Figure 27. Change of Peripheral Pin From General-Purpose Input to Output Mode

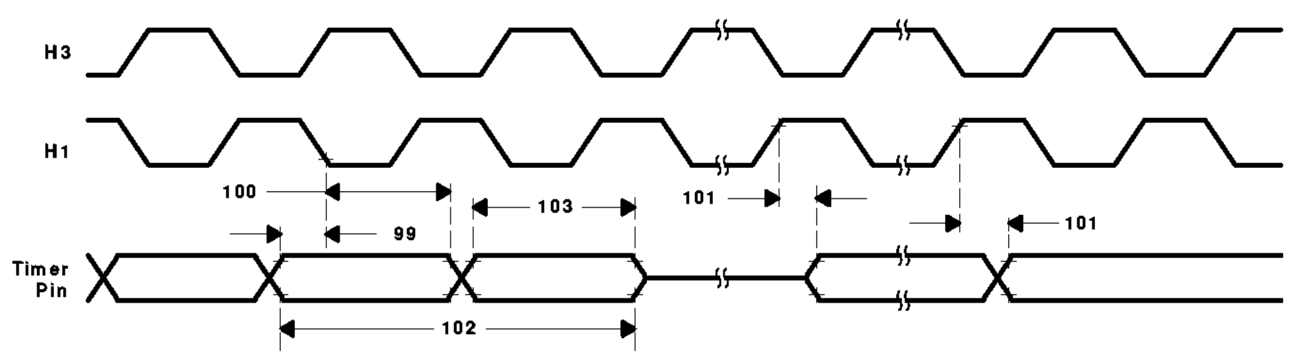
timing parameters for timer pin (see Figure 28)

NO.				’320C30-33 ’320C31-33 MIN	’320C30-33 ’320C31-33 MAX	UNIT
99	$t_{su(TCLK-H1L)}$	Setup time, TCLK ext before H1 low†	TCLK ext	12		ns
100	$t_{h(TCLK-H1L)}$	Hold time, TCLK ext after H1 low†	TCLK ext	0		ns
101	$t_{d(TCLK-H1H)}$	Delay time, H1 high to TCLK int valid	TCLK int		12	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK†	TCLK ext	$t_{c(H)} \times 2.6$‡		ns
			TCLK int	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$‡	ns
103	$t_{w(TCLK)}$	Pulse duration, TCLK high/low†	TCLK ext	$t_{c(H)} + 12$‡		ns
			TCLK int	$[t_{c(TCLK)}/2]-15$	$[t_{c(TCLK)}/2]+5$	ns

NO.				’320C30-40 ’320C31-40 MIN	’320C30-40 ’320C31-40 MAX	UNIT
99	$t_{su(TCLK-H1L)}$	Setup time, TCLK ext before H1 low†	TCLK ext	10		ns
100	$t_{h(TCLK-H1L)}$	Hold time, TCLK ext after H1 low†	TCLK ext	0		ns
101	$t_{d(TCLK-H1H)}$	Delay time, H1 high to TCLK int valid	TCLK int		9	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK †	TCLK ext	$t_{c(H)} \times 2.6$‡		ns
			TCLK int	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$‡	ns
103	$t_{w(TCLK)}$	Pulse duration, TCLK high/low†	TCLK ext	$t_{c(H)} + 12$‡		ns
			TCLK int	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	ns

NO.				’320C31-50 MIN	’320C31-50 MAX	UNIT
99	$t_{su(TCLK-H1L)}$	Setup time, TCLK ext before H1 low†	TCLK ext	10		ns
100	$t_{h(TCLK-H1L)}$	Hold time, TCLK ext after H1 low†	TCLK ext	0		ns
101	$t_{d(TCLK-H1H)}$	Delay time, H1 high to TCLK int valid	TCLK int		8	ns
102	$t_{c(TCLK)}$	Cycle time, TCLK †	TCLK ext	$t_{c(H)} \times 2.6$‡		ns
			TCLK int	$t_{c(H)} \times 2$	$t_{c(H)} \times 2^{32}$‡	ns
103	$t_{w(TCLK)}$	Pulse duration, TCLK high/low†	TCLK ext	$t_{c(H)} + 12$‡		ns
			TCLK int	$[t_{c(TCLK)}/2]-5$	$[t_{c(TCLK)}/2]+5$	ns

† Timing parameters 99 and 100 are applicable for a synchronous input clock. Timing parameters 102 and 103 are applicable for an asynchronous input clock.
‡ Assured by design but not tested



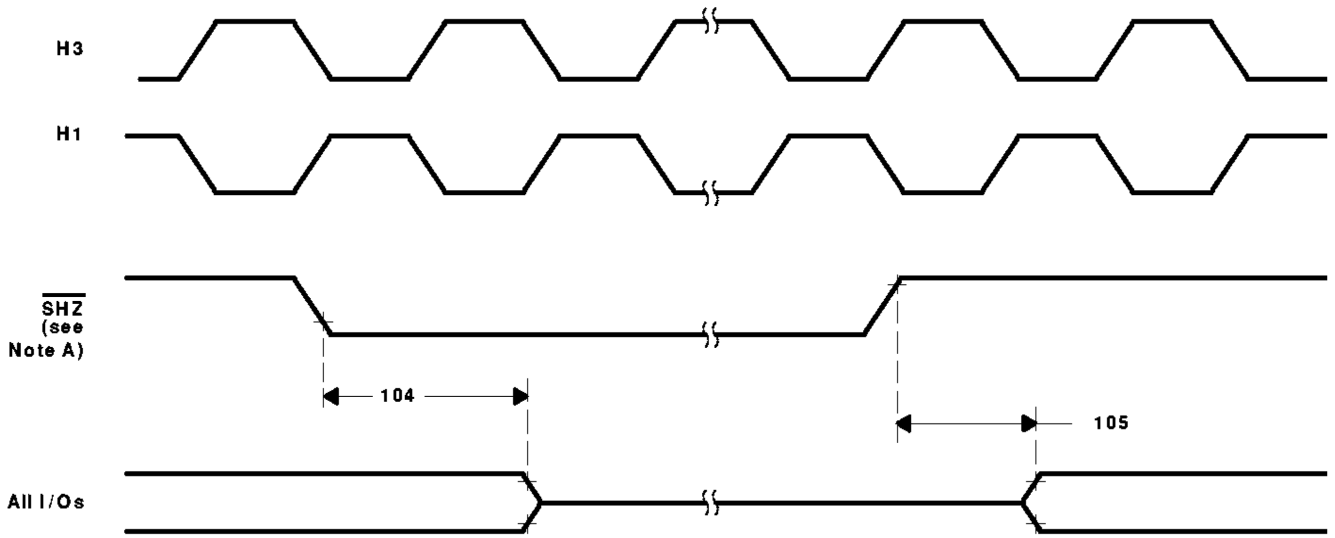
NOTE A: Period and polarity of valid logic level are specified by contents of internal control registers.

Figure 28. Timer-Pin Timing

timing parameters for $\overline{SHZ}$ [P = $t_{c(CI)}$] (see Figure 29)

NO.			’320C30-33 ’320C31-33 ’320C30-40 ’320C31-40		’320C31-50		UNIT
			MIN	MAX	MIN	MAX	
104	$t_{dis(SHZ)}$	Disable time, $\overline{SHZ}$ low to all O, I/O high impedance†	0†	3P + 15†	0†	2P†	ns
105	$t_{en(SHZ)}$	Enable time, $\overline{SHZ}$ high to all O, I/O active†	0†	2P†	0†	2P†	ns

† These values are derived from characterization but not tested.



NOTE A: Enabling $\overline{SHZ}$ destroys SMJ320C3x register and memory contents. Assert $\overline{SHZ}$ and reset the SMJ320C3x to restore it to a known condition.

Figure 29. Timing for $\overline{SHZ}$

SMJ320C30 part order information

DEVICE	TECHNOLOGY	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
SMJ320C30GBM33	0.8-µm CMOS	5 V ± 10%	33 MHz	Ceramic 181-pin PGA	QML
SM320C30GBM33	0.8-µm CMOS	5 V ± 10%	33 MHz	Ceramic 181-pin PGA	Standard
5962-9052603MXA	0.8-µm CMOS	5 V ± 10%	33 MHz	Ceramic 181-pin PGA	DESC SMD
SMJ320C30HFGM33	0.8-µm CMOS	5 V ± 10%	33 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	QML
SM320C30HFGM33	0.8-µm CMOS	5 V ± 10%	33 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	Standard
5962-9052603MUA	0.8-µm CMOS	5 V ± 10%	33 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	DESC SMD
SMJ320C30GBM40	0.8-µm CMOS	5 V ± 5%	40 MHz	Ceramic 181-pin PGA	QML
SM320C30GBM40	0.8-µm CMOS	5 V ± 5%	40 MHz	Ceramic 181-pin PGA	Standard
SMJ320C30TAM33	0.8-µm CMOS	5 V ± 10%	33 MHz	203-lead ILB TAB frame with polyimide encapsulant	QML
SM320C30TAM33	0.8-µm CMOS	5 V ± 10%	33 MHz	203-lead ILB TAB frame with polyimide encapsulant	Standard
SMJ320C30TBM33	0.8-µm CMOS	5 V ± 10%	33 MHz	203-lead ILB TAB frame bare-die option	QML
SM320C30TBM33	0.8-µm CMOS	5 V ± 10%	33 MHz	203-lead ILB TAB frame with bare-die option	Standard
SMJ320C30HFGM40	0.8-µm CMOS	5 V ± 5%	40 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	QML
SM320C30HFGM40	0.8-µm CMOS	5 V ± 5%	40 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	Standard
5962–9052604MUA	0.8-µm CMOS	5 V ± 5%	40 MHz	Ceramic 196-pin quad flatpack with nonconductive tie bar	DESC SMD
5962–9052604MXA	0.8-µm CMOS	5 V ± 5%	40 MHz	Ceramic 181-pin PGA	DESC SMD

SMJ 320 C 30 GB M 33

PREFIX
SMJ = MIL-STD-38535 (QML)
SM = Standard Processing

DEVICE FAMILY
320 = SMJ320 Family

TECHNOLOGY
C = CMOS

DEVICE
30 = ’320C30

SPEED RANGE
33 = 33 MHz
40 = 40 MHz

TEMPERATURE RANGE
M = – 55°C to 125°C
L = 0°C to 70°C

PACKAGE TYPE
GB = 181-Pin Grid Array (PGA) Ceramic Package
HFG = 196-Pin Ceramic Quad Flatpack with a nonconductive tie bar
TA = 203-lead ILB TAB frame with polyimide encapsulant
TB = 203-lead ILB TAB frame, bare-die option
KGD = Known Good Die

Figure 30. SMJ320C30 Device Nomenclature

SMJ320C31 part order information

DEVICE	TECHNOLOGY	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
SMJ320C31GFAM33	0.72-μm CMOS	5 V ± 10%	33 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM33	0.72-μm CMOS	5 V ± 10%	33 MHz	Ceramic 141-pin staggered PGA	Std
SMJ320C31GFAM40	0.72-μm CMOS	5 V ± 5%	40 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM40	0.72-μm CMOS	5 V ± 5%	40 MHz	Ceramic 141-pin staggered PGA	Std
SMJ320C31HFGM33	0.72-μm CMOS	5 V ± 10%	33 MHz	Ceramic 132-pin quad flatpack with a nonconductive tie bar	QML
SM320C31HFGM33	0.72-μm CMOS	5 V ± 10%	33 MHz	Ceramic 132-pin quad flatpack with a nonconductive tie bar	Std
SMJ320C31HFGM40	0.72-μm CMOS	5 V ± 5%	40 MHz	Ceramic 132-pin quad flatpack with a nonconductive tie bar	QML
SM320C31HFGM40	0.72-μm CMOS	5 V ± 5%	40 MHz	Ceramic 132-pin quad flatpack with a nonconductive tie bar	Std
SMJ320C31TAM33	0.72-μm CMOS	5 V ± 10%	33 MHz	132-lead ILB TAB frame with polyimide encapsulant	QML
SM320C31TAM33	0.72-μm CMOS	5 V ± 10%	33 MHz	132-lead ILB TAB frame with polyimide encapsulant	Standard
SMJ320C31TBM33	0.72-μm CMOS	5 V ± 10%	33 MHz	132-lead ILB TAB frame bare-die option	QML
SM320C31TBM33	0.72-μm CMOS	5 V ± 10%	33 MHz	132-lead ILB TAB frame with bare-die option	Standard
SMJ320C31GFAM50	0.72-μm CMOS	5 V ± 5%	50 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM50	0.72-μm CMOS	5 V ± 5%	50 MHz	Ceramic 141-pin staggered PGA	Standard
SMJ320C31HFGM50	0.72-μm CMOS	5 V ± 5%	50 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar	QML
SM320C31HFGM50	0.72-μm CMOS	5 V ± 5%	50 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar	Standard
5962-9205802MXA	0.72-μm CMOS	5 V ± 10%	33 MHz	141-pin CPGA	DESC SMD
5962-9205802MYA	0.72-μm CMOS	5 V ± 10%	33 MHz	132-pin CQFP	DESC SMD
5962-9205803MXA	0.72-μm CMOS	5 V ± 5%	40 MHz	141-pin CPGA	DESC SMD
5962-9205803MYA	0.72-μm CMOS	5 V ± 5%	40 MHz	132-pin CQFP	DESC SMD
5962-9205804MXA	0.72-μm CMOS	5 V ± 5%	50 MHz	Ceramic 141-pin staggered PGA	DESC SMD
5962-9205804MYA	0.72-μm CMOS	5 V ± 5%	50 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DESC SMD

SMJ320C31 part order information (continued)

SMJ 320 C 31 GFA M 33

PREFIX
SMJ = MIL-PRF-38535 (QML)
SM = Standard Processing

DEVICE FAMILY
320 = SMJ320 Family

TECHNOLOGY
C = CMOS

DEVICE
31 = '320C31

SPEED RANGE
33 = 33 MHz
40 = 40 MHz
50 = 50 MHz

TEMPERATURE RANGE
M = −55°C to 125°C
L = 0°C to 70°C

PACKAGE TYPE
GFA = 141-Pin Staggered Grid Array Ceramic Package
HFG = 132-Pin Ceramic Quad Flatpack with a nonconductive tie bar
TA = 132-lead ILB TAB frame with polyimide encapsulant
TB = 132-lead ILB TAB frame, bare-die option
KGD = Known Good Die

Figure 31. SMJ320C31 Device Nomenclature

SMJ320C30 (Rev. 5) Inner Lead Bond (ILB) Information for TAB

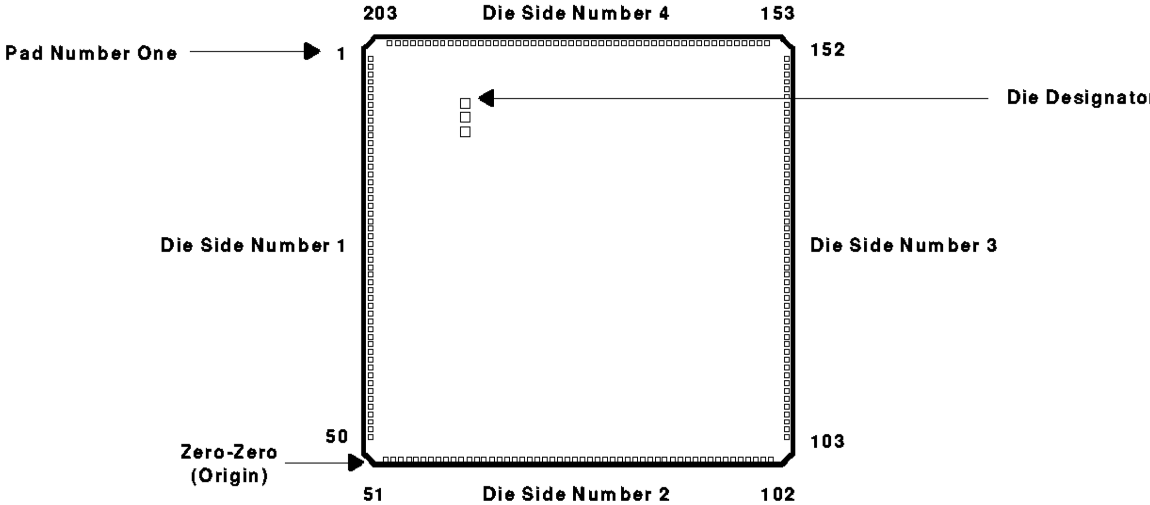


Figure 32. SMJ320C30 Die Numbering Format (Refer to Table 1)

The inner lead bond (ILB) pitch for the TAB leadframe is the same as the die bond pad pitch. Table 1 provides a reference for the following:

A. The TAB lead numbers. The TAB lead numbers are the same as the die bond pad numbers.

B. The ’C30 signal identities in relation to the pad numbers

C. Signal functions that fan out to more than one test pad location. (There are 203 bond pad locations, 203 TAB leads, and 244 test pad locations.)

D. The ’C30 X-,Y-coordinates, where bond pad 51 serves as the origin, (0,0)

E. The ILB pitch for the TAB leadframe

In addition, the following notes are significant:

F. X,Y coordinate data is in microns.

G. Coordinate origin is at (0,0) (center of bond pad 51).

H. Average pitch is 186 µm (7.32 mils).

I. Smallest pitch value is 156,8 µm (6.17 mils).

J. The active silicon dimensions are 10224,00 µm × 11032,00 µm (402.52 mils × 434.33 mils).

K. The die size is approximately 10541,00 µm × 11353,8 µm (415.00 mils × 447.00 mils).

L. Distance from diced silicon to polyimide support ring is 1016,0 µm (40 mils).

M. Bond pad dimensions are 115,00 µm × 115,00 µm (4.53 mils × 4.53 mils).

N. Center of bond pad to edge of die ranges from 180 µm – 220 µm (7.1 mils – 8.6 mils). The range of 40 µm (1.57 mils) exists since the dicing process will result in some tolerance. Due to the consistency and precision of the bond pad locations in reference to each other, the center of bond pad 51 was chosen as the origin.

Table 1. SMJ320C30 Die Pad/TAB Lead Information : Rev. 5 (0,8 µm)

DIE SIDE #1					
C30 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB C30 TEST PAD LOCATIONS	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
1	PDV$_{DD}$	1, 2		9563.00	195.20 (1,2)
2	PDV$_{DD}$	3, 4		9367.80	168.60 (2,3)
3	DR0	5		9199.20	192.00 (3,4)
4	FSR0	6		9007.20	184.00 (4,5)
5	CLKR0	7		8823.20	192.00 (5,6)
6	CLKX0	8		8631.20	184.00 (6,7)
7	FSX0	9		8447.20	192.00 (7,8)
8	DX0	10		8255.20	184.00 (8,9)
9	TCLK0	11		8071.20	192.00 (9,10)
10	TCLK1	12		7879.20	184.00 (10,11)
11	EMU6	13		7695.20	192.00 (11,12)
12	XD0	14		7503.20	184.00 (12,13)
13	XD1	15		7319.20	192.00 (13,14)
14	XD2	16		7127.20	180.20 (14,15)
15	IODV$_{DD}$	17, 18		6947.00	195.20 (15,16)
16	IODV$_{DD}$	19, 20		6751.80	168.60 (16,17)
17	XD3	21		6853.20	184.00 (17,18)
18	XD4	22		6399.20	192.00 (18,19)
19	XD5	23		6207.20	184.00 (19,20)
20	XD6	24		6023.20	192.00 (20,21)
21	XD7	25		5831.20	184.00 (21,22)
22	XD8	26		5647.20	192.00 (22,23)
23	XD9	27		5455.20	184.00 (23,24)
24	XD10	28		5271.20	188.20 (24,25)
25	V_{DD}	29, 30	– 423.80	5083.00	195.20 (25,26)
26	V_{DD}	31, 32		4887.80	156.80 (26,27)
27	V_{SS}	33, 34, 35		4731.00	195.20 (27,28)
28	V_{SS}	36, 37		4535.80	168.60 (28,29)
29	XD11	38		4367.20	184.00 (29,30)
30	XD12	39		4183.20	192.00 (30,31)
31	XD13	40		3991.20	184.00 (31,32)
32	XD14	41		3807.20	192.00 (32,33)
33	XD15	42		3615.20	184.00 (33,34)
34	XD16	43		3431.20	192.00 (34,35)
35	XD17	44		3239.20	184.00 (35,36)
36	XD18	45		3055.20	192.00 (36,37)
37	XD19	46		2863.20	184.00 (37,38)
38	XD20	47		2679.20	192.00 (38,39)
39	XD21	48		2487.20	184.00 (39,40)
40	XD22	49		2303.20	192.00 (40,41)
41	XD23	50		2111.20	184.00 (41,42)
42	XD24	51		1927.20	192.00 (42,43)
43	XD25	52		1735.20	184.00 (43,44)
44	XD26	53		1551.20	192.00 (44,45)
45	XD27	54		1359.20	184.00 (45,46)
46	XD28	55		1175.20	192.00 (46,47)
47	XD29	56		983.20	184.00 (47,48)
48	XD30	57		799.20	180.20 (48,49)
49	IODV$_{DD}$	58, 59		619.00	195.20 (49,50)
50	IODV$_{DD}$	60, 61		423.80	

Table 1. SMJ320C30 Die Pad/TAB Lead Information : Rev. 5 (0,8 μm) (Continued)

DIE SIDE #2					
C30 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB C30 TEST PAD LOCATIONS	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
51	DV_{SS}	62, 63	0.00		195.20 (51, 52)
52	DV_{SS}	64	195.2		179.60 (52, 53)
53	CV_{SS}	65, 66	374.80		195.20 (53, 54)
54	CV_{SS}	67	570.00		176.60 (54, 55)
55	XD31	68	746.60		192.00 (55, 56)
56	A23	69	938.60		200.00 (56, 57)
57	A22	70	1138.60		200.00 (57, 58)
58	A21	71	1338.60		192.00 (58, 59)
59	A20	72	1530.60		200.00 (59, 60)
60	A19	73	1730.60		192.00 (60, 61)
61	A18	74	1922.60		200.00 (61, 62)
62	A17	75	2122.60		200.00 (62, 63)
63	A16	76	2322.60		192.00 (63, 64)
64	A15	77	2514.36		200.00 (64, 65)
65	A14	78	2902.80		188.20 (65, 66)
66	ADV_{DD}	79, 80	2714.60		195.20 (66, 67)
67	ADV_{DD}	81	2902.80		176.60 (67, 68)
68	A13	82	3098.00		200.00 (68, 69)
69	A12	83	3274.60		192.00 (69, 70)
70	A11	84	3474.60		200.00 (70, 71)
71	A10	85	3666.60		200.00 (71, 72)
72	A9	86	3866.60		192.00 (72, 73)
73	A8	87	4258.60		200.00 (73, 74)
74	A7	88	4458.60		192.00 (74, 75)
75	A6	89	4650.60		196.20 (75, 76)
76	V_{DD}	90, 91	4846.80	0.00	195.20 (76, 77)
77	V_{DD}	92, 93	5042.00		172.80 (77, 78)
78	V_{SS}	94, 95	5214.80		195.20 (78, 79)
79	V_{SS}	96, 97	2410.00		168.60 (79, 80)
80	A5	98	5578.60		200.00 (80, 81)
81	A4	99	5778.60		192.00 (81, 82)
82	A3	100	5970.60		200.00 (82, 83)
83	A2	101	6170.60		200.00 (83, 84)
84	A1	102	6370.60		192.00 (84, 85)
85	A0	103	6562.60		212.20 (85, 86)
86	EMU0	104	6774.80		216.00 (86, 87)
87	EMU1	105	6990.80		208.00 (87, 88)
88	EMU2	106	7198.80		203.80 (88, 89)
89	EMU3	107	7402.60		204.20 (89, 90)
90	EMU4/$\overline{SHZ}$	108	7606.80		216.00 (90, 91)
91	MC/$\overline{MP}$	109	7822.80		203.80 (91, 92)
92	XA12	110	8026.60		192.00 (92, 93)
93	XA11	111	8218.60		200.00 (93, 94)
94	XA10	112	8418.60		192.00 (94, 95)
95	XA9	113	8610.60		200.00 (95, 96)
96	XA8	114	8810.60		200.00 (96, 97)
97	XA7	115	9010.60		192.00 (97, 98)
98	XA6	116	9202.60		196.20 (98, 99)
99	IV_{SS}	117, 118	9398.80		195.20 (99, 100)
100	IV_{SS}	119	9594.00		164.80 (100, 101)
101	DV_{SS}	120, 121	9758.80		195.20 (101, 102)
102	DV_{SS}	122	9954.00		

Table 1. SMJ320C30 Die Pad/TAB Lead Information : Rev. 5 (0,8 μm) (Continued)

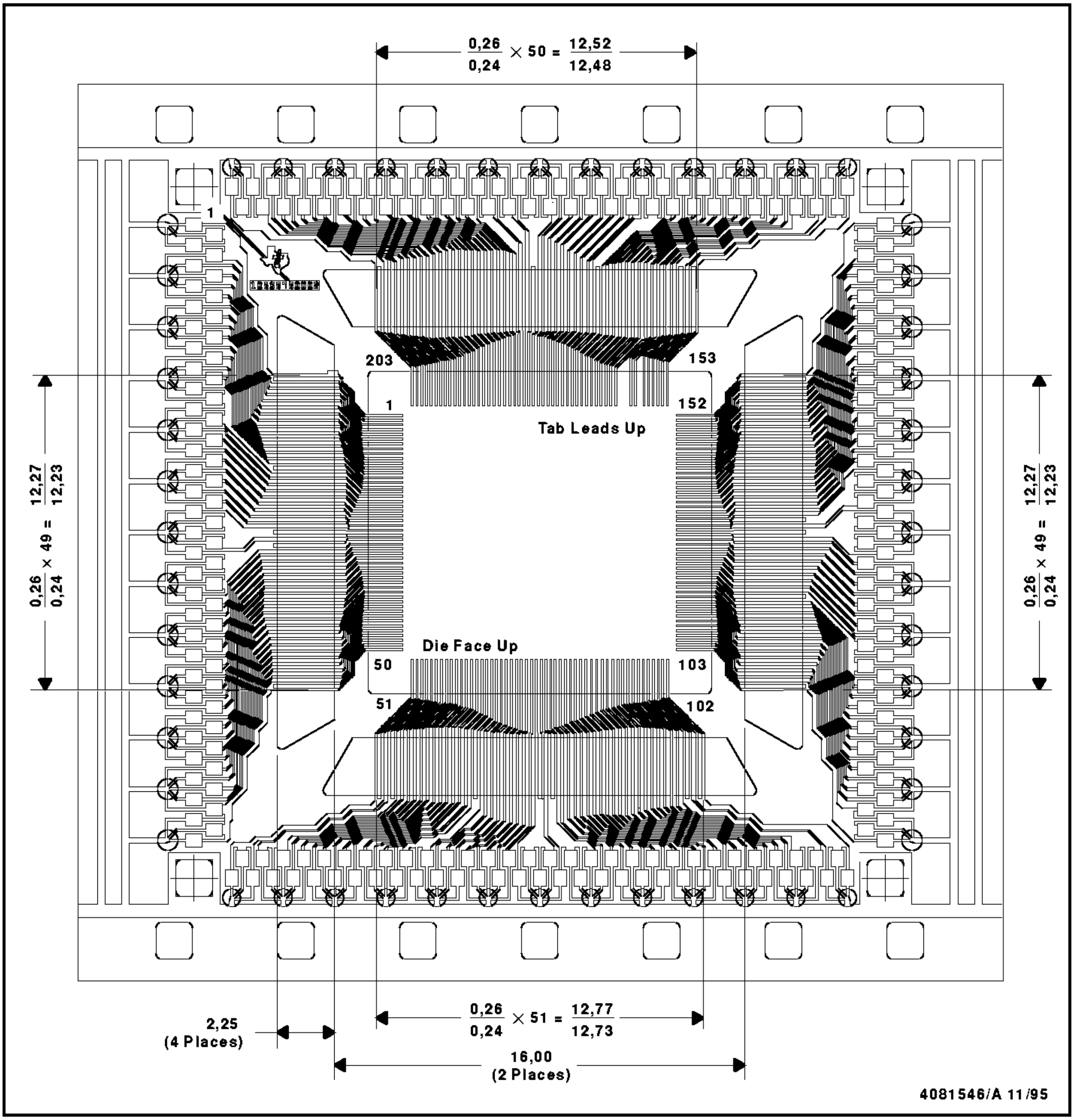
DIE SIDE #3					
C30 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB C30 TEST PAD LOCATIONS	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
103	ADV_{DD}	123, 124		430.60	195.20 (103,104)
104	ADV_{DD}	125, 126		625.80	168.60 (104,105)
105	XA5	127		764.40	192.00 (105,106)
106	XA4	128		986.40	184.00 (106,107)
107	XA3	129		1170.40	192.00 (107,108)
108	XA2	130		1362.40	184.00 (108,109)
109	XA1	131		1546.40	192.00 (109,110)
110	XA0	132		1738.40	184.00 (110,111)
111	D31	133		1922.40	192.00 (111,112)
112	D30	134		2114.40	184.00 (112,113)
113	D29	135		2298.40	192.00 (113,114)
114	D28	136		2490.40	184.00 (114,115)
115	D27	137		2674.40	192.00 (115,116)
116	D26	138		2866.40	180.20 (116,117)
117	DDV_{DD}	139, 140		3046.60	195.20 (117,118)
118	DDV_{DD}	141, 142		3241.80	168.60 (118,119)
119	D25	143		3410.40	184.00 (119,120)
120	D24	144		3594.40	192.00 (120,121)
121	D23	145		3786.40	184.00 (121,122)
122	D22	146		3970.40	192.00 (122,123)
123	D21	147		4162.40	184.00 (123,124)
124	D20	148		4346.40	192.00 (124,125)
125	D19	149	10377.80	4538.40	184.00 (125,126)
126	D18	150		4722.40	188.20 (126,127)
127	V_{DD}	151, 152		4910.60	195.20 (127,128)
128	V_{DD}	153, 154, 155		5105.80	156.80 (128,129)
129	V_{SS}	156, 157		5262.60	195.20 (129,130)
130	V_{SS}	158, 159		5457.80	168.60 (130,131)
131	D17	160		5626.40	184.00 (131,132)
132	D16	161		5810.40	192.00 (132,133)
133	D15	162		6002.40	184.00 (133,134)
134	D14	163		6186.40	192.00 (134,135)
135	D13	164		6378.40	184.00 (135,136)
136	D12	165		6562.40	192.00 (136,137)
137	D11	166		6754.40	184.00 (137,138)
138	D10	167		6938.40	192.00 (138,139)
139	D9	168		7130.40	184.00 (139,140)
140	D8	169		7314.40	192.00 (140,141)
141	D7	170		7506.40	184.00 (141,142)
142	D6	171		7690.40	192.00 (142,143)
143	D5	172		7882.40	184.00 (143,144)
144	D4	173		8066.40	192.00 (144,145)
145	D3	174		8258.40	184.00 (145,146)
146	D2	175		8442.40	192.00 (146,147)
147	D1	176		8634.40	184.00 (147,148)
148	D0	177		8818.40	192.00 (148,149)
149	H1	178		9010.40	184.00 (149,150)
150	H3	179		9194.40	180.20 (150,151)
151	DDV_{DD}	180, 181		9374.60	195.20 (151,152)
152	DDV_{DD}	182, 183		9569.80	

Table 1. SMJ320C30 Die Pad/TAB Lead Information : Rev. 5 (0,8 µm) (Continued)

DIE SIDE #4					
C30 DIE BOND PAD LOCATIONS	DIE/TAB BOND PAD IDENTITY	TAB C30 TEST PAD LOCATIONS	X-COORDINATE OF THE DIE BOND PAD	Y-COORDINATE OF THE DIE BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
153	DV_{SS}	184	9947.20		195.20 (153,154)
154	DV_{SS}	185, 186	9752.00		164.80 (154,155)
155	CV_{SS}	187	9587.20		195.20 (155,156)
156	CV_{SS}	188, 189	9392.00		175.00 (156,157)
157	X2/CLKIN	190	9217.00	9986.80	173.20 (157,158)
158	X1	191	9043.80	9986.80	347.80 (158,159)
159	V_{SUBS}	192, 193	8696.00		160.60 (159,160)
160	V_{BBP}	194	8535.40		600.00 (160,161)
161	EMU5	195	7935.40		196.00 (161,162)
162	$\overline{XRDY}$	196	7739.40		188.00 (162,163)
163	$\overline{MSTRB}$	197	7551.40		192.00 (163,164)
164	$\overline{IOSTRB}$	198	7359.40		184.00 (164,165)
165	$XR/\overline{W}$	199	7175.40		184.00 (165,166)
166	$\overline{HOLDA}$	200	6991.40		196.20 (166,167)
167	$\overline{HOLD}$	201	6795.20		184.00 (167,168)
168	MDV_{DD}	202	6611.20		195.20 (168,169)
169	MDV_{DD}	203, 204	6416.00		172.80 (169,170)
170	$\overline{RDY}$	205	6243.20		187.80 (170,171)
171	$\overline{STRB}$	206	6055.40		192.00 (171,172)
172	$R/\overline{W}$	207	5863.40		196.20 (172,173)
173	$\overline{RESET}$	208	5667.20		187.80 (173,174)
174	XF1	209	5479.40		184.00 (174,175)
175	XF0	210	5295.40		184.00 (175,176)
176	$\overline{IACK}$	211	5111.40	9993.60	196.20 (176,177)
177	$\overline{INT0}$	212	4915.20		184.00 (177,178)
178	V_{DD}	213, 214	4731.20		195.20 (178,179)
179	V_{DD}	215, 216	4536.00		164.80 (179,180)
180	V_{SS}	217, 218	4371.20		195.20 (180,181)
181	V_{SS}	219, 220	4176.00		172.80 (181,182)
182	$\overline{INT1}$	221	4003.20		200.00 (182,183)
183	$\overline{INT2}$	222	3803.20		200.00 (183,184)
184	$\overline{INT3}$	223	3603.20		200.00 (184,185)
185	RSV0	224	3403.20		200.00 (185,186)
186	RSV1	225	3203.20		200.00 (186,187)
187	RSV2	226	3003.20		208.00 (187,188)
188	RSV3	227	2795.20		200.00 (188,189)
189	RSV4	228	2595.20		187.80 (189,190)
190	RSV5	229	2407.40		184.00 (190,191)
191	RSV6	230	2223.40		184.00 (191,192)
192	RSV7	231	2039.40		184.00 (192,193)
193	RSV8	232	1855.40		184.00 (193,194)
194	RSV9	233	1671.40		192.00 (194,195)
195	RSV10	234	1479.40		184.00 (195,196)
196	DR1	235	1295.40		184.00 (196,197)
197	FSR1	236	1111.40		184.00 (197,198)
198	CLKR1	237	927.40		184.00 (198,199)
199	CLKX1	238	743.40		184.00 (199,200)
200	FSX1	239	559.40		184.00 (200,201)
201	DX1	240	375.40		180.20 (201,202)
202	DV_{SS}	241, 242	195.20		195.20 (202,203)
203	DV_{SS}	243, 244	0.00		

MECHANICAL DATA

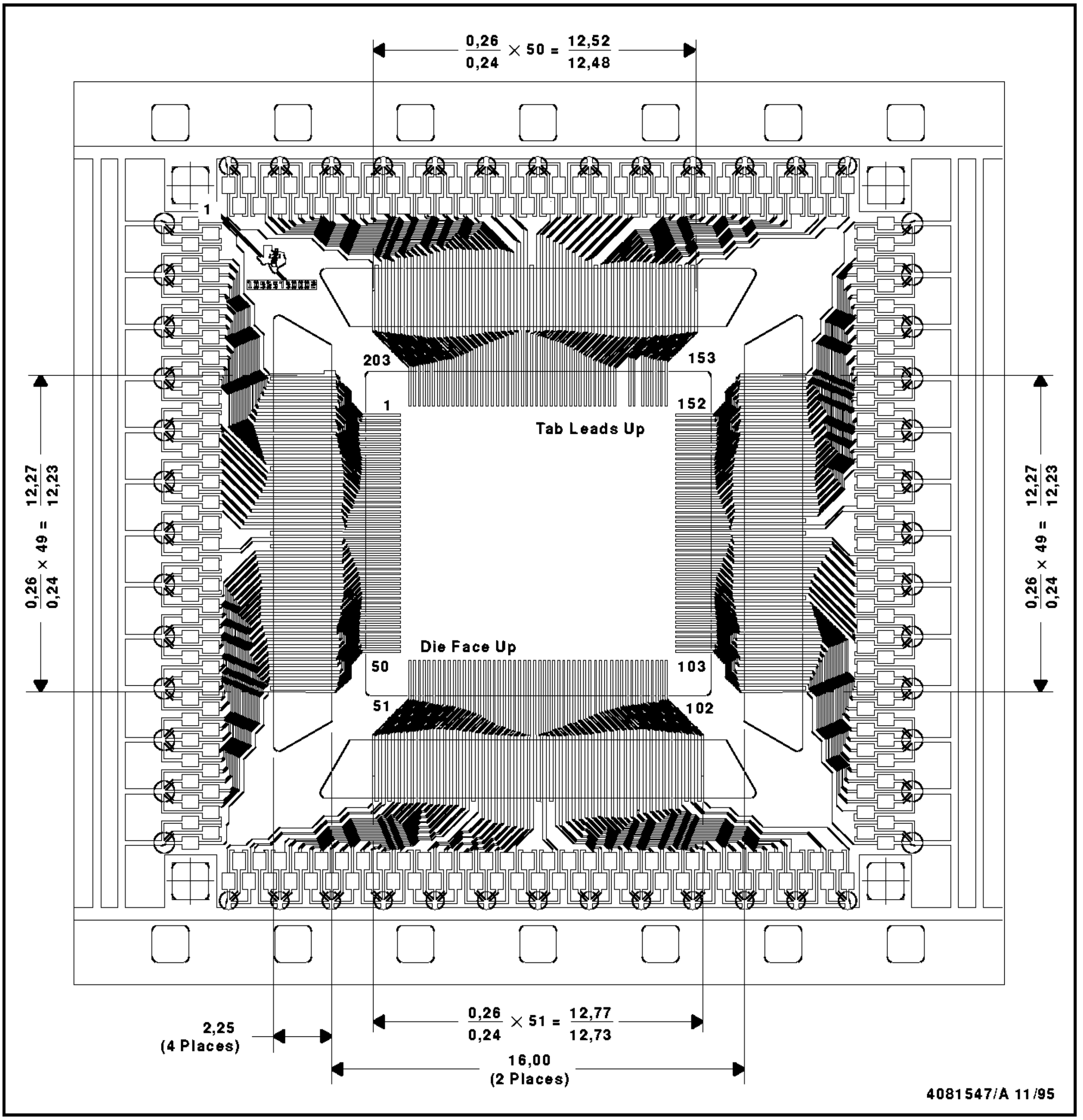
TA (35 OR 70 mm WITH PROTECTIVE FILM) **SMJ320C30 244-PIN TAB FRAME (PG5) SOCKET, 203 OLB/ILB 0,25-mm OLB PITCH**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The OLB lead width is 0,1016 ± 0,02 mm.
D. The ILB lead width is 0,0832 ± 0,015 mm.
E. The Tape width is 35 mm.
F. The TA is encapsulated die with polyimide overcoat.

MECHANICAL DATA

TB (35 OR 70 mm WITHOUT PROTECTIVE FILM) **SMJ320C30 244-PIN TAB FRAME (PG5) SOCKET, 203 OLB/ILB 0,25-mm OLB PITCH**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The OLB lead width is 0,1016 ± 0,02 mm.
D. The ILB lead width is 0,0832 ± 0,015 mm.
E. The Tape width is 35 mm.
F. The TB is bare die.

SMJ320C31 (Rev. 2) Inner Lead Bond Information for TAB

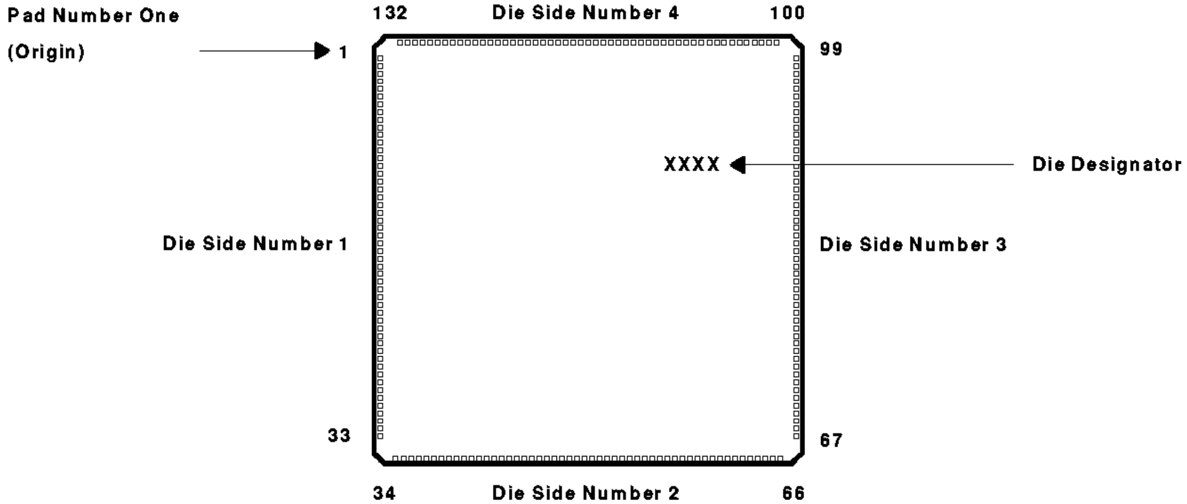


Figure 33. SMJ320C31 Die Numbering Format
(Refer to Table 2)

The inner lead bond (ILB) pitch for the TAB leadframe is the same as the die bond pad pitch. Table 2 provides a reference for the following:

A. The TAB lead numbers. The TAB lead numbers are the same as the die bond pad numbers.

B. The ’C31 signal identities in relation to the pad numbers

C. Signal functions that fan out to more than one test pad location. (There are 132 bond pad locations, 132 TAB leads, and 244 test pad locations.)

D. The ’C31 X-,Y-coordinates, where bond pad 1 serves as the origin, (0,0)

E. The ILB pitch for the TAB leadframe

In addition, the following notes are significant:

F. X-,Y-coordinate data is in microns.

G. Coordinate origin is at (0,0) (center of bond pad 1).

H. Average pitch is 233 µm (9.17 mils).

I. Smallest pitch value is 179,6 µm (7.07 mils).

J. The active silicon dimensions are 10215,20 µm × 10324,00 µm (402.17 mils × 406.46 mils).

K. The die size is approximately 10541 µm × 10642,60 µm (415.00 mils × 419.00 mils).

L. Distance from diced silicon to polyimide support ring is 635.00 µm (25 mils).

Table 2. SMJ320C31 Die Pad /TAB Lead Information : Rev. 2 (0,8 µm)

DIE SIDE #1					
C31 DIE BOND PAD LOCATIONS	DIE /TAB BOND PAD IDENTITY	TAB C31 TEST PAD LOCATIONS	X-COORDINATE OF THE CENTER OF BOND PAD	Y-COORDINATE OF THE CENTER OF BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
	N/C	1, 2, 3			
1	A9	4		0.00	300.00 (1,2)
2	DV_{SS}	5, 6, 7		–300.00	269.20 (2,3)
3	A8	8		–569.20	274.60 (3,4)
4	A7	9		–843.80	293.20 (4,5)
5	A6	10		–1137.00	278.60 (5,6)
6	A5	11		–1415.60	295.20 (6,7)
7	AV_{DD}	12, 13, 14		–1710.80	263.20 (7,8)
8	A4	15		–1974.00	277.40 (8,9)
9	A3	16		–2251.40	285.00 (9,10)
10	A2	17		–2536.40	273.40 (10,11)
11	A1	18		–2809.80	298.40 (11,12)
12	A0	19		–3108.20	297.80 (12,13)
13	CV_{SS}	20, 21, 22		–3406.00	256.80 (13,14)
14	D31	23		–3662.80	320.80 (14,15)
15	V_{DDL}	24, 25, 26		–3983.60	180.40 (15,16)
16	V_{DDL}	27, 28, 29		–4164.00	293.80 (16,17)
17	D30	30	0.00	–4457.80	363.60 (17,18)
18	V_{SSL}	31, 32, 33		–4821.40	180.00 (18,19)
19	V_{SSL}	34, 35, 36		–5001.40	315.40 (19,20)
20	DV_{SS}	37, 38, 39		–5316.80	278.00 (20,21)
21	D29	40		–5594.80	278.40 (21,22)
22	D28	41		–5873.20	320.20 (22,23)
23	DV_{DD}	42, 43, 44		–6193.40	349.80 (23,24)
24	D27	45		–6543.20	253.20 (24,25)
25	IV_{SS}	46, 47, 48		–6796.40	305.80 (25,26)
26	D26	49		–7102.20	272.20 (26,27)
27	D25	50		–7374.40	285.20 (27,28)
28	D24	51		–7659.60	287.80 (28,29)
29	D23	52		–7947.40	290.40 (29,30)
30	D22	53		–8237.80	258.80 (30,31)
31	D21	54		–8496.60	291.60 (31,32)
32	DV_{DD}	55, 56, 57		–8788.20	224.20 (32,33)
33	D20	58		–9012.40	
	N/C	59, 60, 61			

Table 2. SMJ320C31 Die Pad / TAB Lead Information : Rev. 2 (0,8 µm) (Continued)

DIE SIDE #2					
C31 DIE BOND PAD LOCATIONS	DIE / TAB BOND PAD IDENTITY	TAB C31 TEST PAD LOCATIONS	X-COORDINATE OF THE CENTER OF BOND PAD	Y-COORDINATE OF THE CENTER OF BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
	N/C	62, 63, 64			
34	DV_{SS}	65, 66, 67	508.60		352.60 (34, 35)
35	D19	68	861.20		280.80 (35, 36)
36	D18	69	1142.00		272.00 (36, 37)
37	D17	70	1414.00		268.80 (37, 38)
38	D16	71	1682.80		243.20 (38, 39)
39	D15	72	1926.00		375.60 (39, 40)
40	CV_{SS}	73, 74, 75	2301.60		212.40 (40, 41)
41	D14	76	2514.00		314.00 (41, 42)
42	DV_{DD}	77, 78, 79	2828.00		207.60 (42, 43)
43	D13	80	3035.60		400.60 (43, 44)
44	IV_{SS}	81, 82, 83	3436.20		214.60 (44, 45)
45	D12	84	3650.80		268.80 (45, 46)
46	D11	85	3919.60		293.60 (46, 47)
47	D10	86	4213.20		343.40 (47, 48)
48	V_{DDL}	87, 88, 89	4556.60		179.60 (48, 49)
49	V_{DDL}	90, 91, 92	4736.20		315.40 (49, 50)
50	D9	93	5051.60	–9480.40	281.60 (50, 51)
51	D8	94	5333.20		285.20 (51, 52)
52	DV_{SS}	95, 96, 97	5618.40		340.00 (52, 53)
53	V_{SSL}	98, 99, 100	5958.40		180.40 (53, 54)
54	V_{SSL}	101, 102, 103	6138.80		289.60 (54, 55)
55	D7	104	6428.40		286.40 (55, 56)
56	D6	105	6714.80		297.80 (56, 57)
57	DV_{DD}	106, 107, 108	7012.60		267.00 (57, 58)
58	D5	109	7279.60		280.80 (58, 59)
59	D4	110	7560.40		282.40 (59, 60)
60	D3	111	7842.80		284.80 (60, 61)
61	D2	112	8127.60		276.00 (61, 62)
62	D1	113	8403.60		285.60 (62, 63)
63	D0	114	8689.20		290.40 (63, 64)
64	H1	115	8979.60		274.40 (64, 65)
65	H3	116	9254.00		377.20 (65, 66)
66	DV_{DD}	117, 118, 119	9631.20		
	N/C	120, 121, 122			

Table 2. SMJ320C31 Die Pad /TAB Lead Information : Rev. 2 (0,8 µm) (Continued)

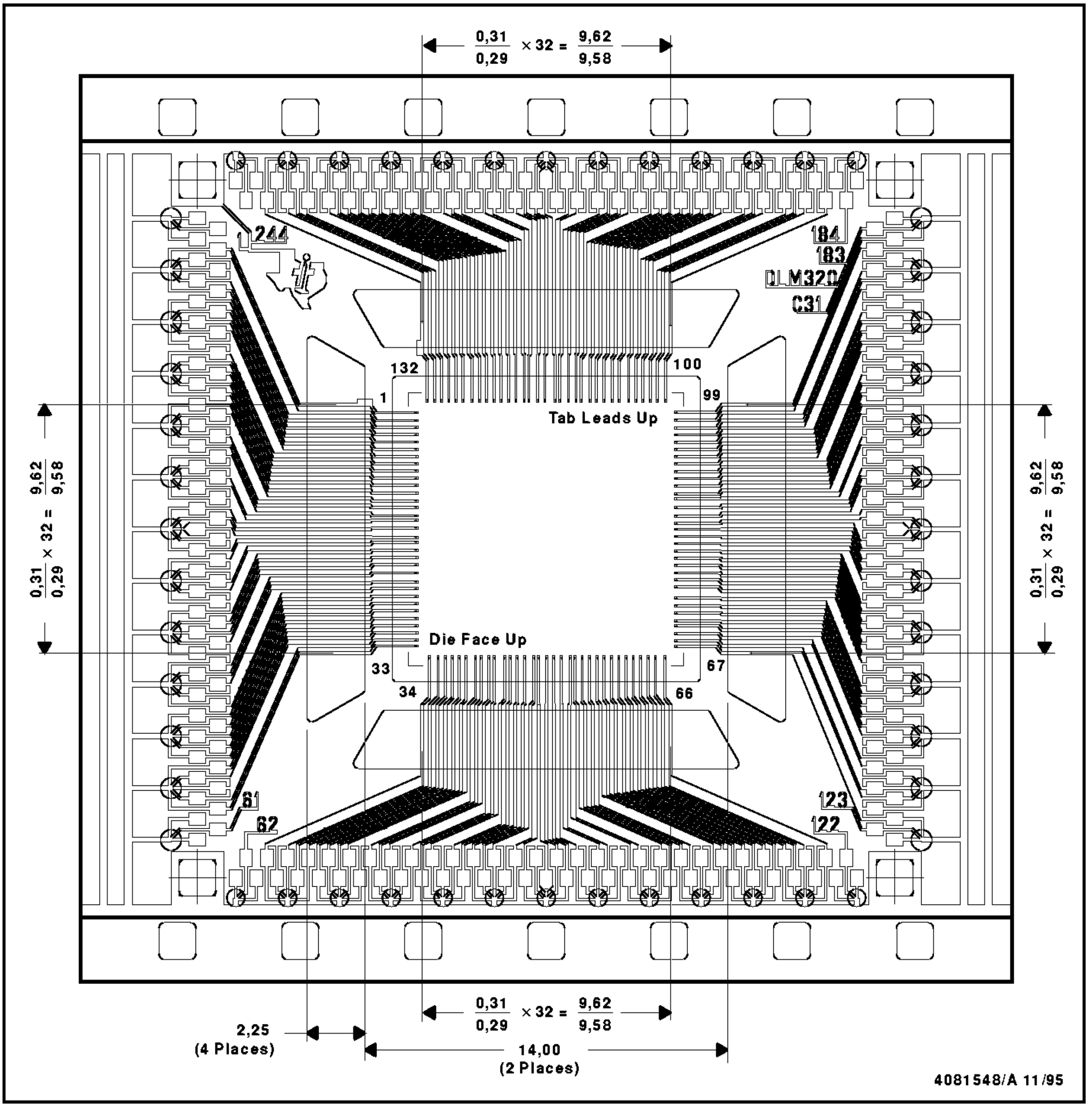
DIE SIDE #3					
C31 DIE BOND PAD LOCATIONS	**DIE /TAB BOND PAD IDENTITY**	**TAB C31 TEST PAD LOCATIONS**	**X-COORDINATE OF THE CENTER OF BOND PAD**	**Y-COORDINATE OF THE CENTER OF BOND PAD**	**PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS**
	N/C	123, 124			
67	DV_{SS}	125, 126, 127		–9032.60	210.40 (67, 68)
68	CV_{SS}	128, 129, 130		–8822.20	280.00 (68, 69)
69	IV_{SS}	131, 132, 133		–8542.20	301.80 (69, 70)
70	X2/CLKIN	134		–8240.40	186.20 (70, 71)
71	X1	135		–8054.20	311.40 (71, 72)
72	$\overline{HOLDA}$	136		–7742.80	282.80 (72,73)
73	$\overline{HOLD}$	137		–7460.00	293.00 (73, 74)
74	CV_{DD}	138, 139, 140		–7167.00	431.00 (74, 75)
75	$\overline{RDY}$	141		–6736.00	276.80 (75, 76)
76	$\overline{STRB}$	142		–6459.20	268.00 (76, 77)
77	R/$\overline{W}$	143		–6191.20	295.20 (77, 78)
78	$\overline{RESET}$	144		–5896.00	278.40 (78, 79)
79	XF0	145		–5617.60	266.60 (79, 80)
80	CV_{DD}	146, 147, 148		–5351.00	291.00 (80, 81)
81	XF1	149		–5060.00	275.20 (81, 82)
82	$\overline{IACK}$	150		–4784.80	280.80 (82, 83)
83	$\overline{INT0}$	151	10074.00	–4504.00	224.80 (83, 84)
84	DV_{SS}	152, 153, 154		–4279.20	280.40 (84, 85)
85	V_{SSL}	155, 156, 157		–3998.80	326.80 (85, 86)
86	$\overline{INT1}$	158		–3672.00	341.40 (86, 87)
87	V_{DDL}	159, 160, 161		–3330.60	180.40 (87, 88)
88	V_{DDL}	162, 163, 164		–3150.20	323.80 (88, 89)
89	$\overline{INT2}$	165		–2826.40	279.80 (89, 90)
90	$\overline{INT3}$	166		–2546.60	266.40 (90, 91)
91	DR0	167		–2280.20	310.00 (91, 92)
92	CV_{SS}	168, 169, 170		–1970.20	270.80 (92, 93)
93	FSR0	171		–1699.40	275.60 (93, 94)
94	CLKR0	172		–1423.80	280.60 (94, 95)
95	CLKX0	173		–1143.20	280.40 (95, 96)
96	IV_{SS}	174, 175, 176		–862.80	261.40 (96, 97)
97	FSX0	177		–601.40	312.80 (97, 98)
98	PV_{DD}	178, 179, 180		–288.60	294.20 (98, 99)
99	DX0	181		5.60	
	N/C	182, 183			

Table 2. SMJ320C31 Die Pad / TAB Lead Information : Rev. 2 (0,8 µm) (Continued)

DIE SIDE #4					
C31 DIE BOND PAD LOCATIONS	DIE / TAB BOND PAD IDENTITY	TAB C31 TEST PAD LOCATIONS	X-COORDINATE OF THE CENTER OF BOND PAD	Y-COORDINATE OF THE CENTER OF BOND PAD	PITCH OF LEAD (#, #) REFERENCE WHICH DIE BOND PADS
	N/C	184, 185, 186			
100	V_{SUBS}	187, 188, 189	9649.40		314.20 (100, 101)
101	$\overline{SHZ}$	190	9335.20		279.60 (101, 102)
102	DV_{SS}	191, 192, 193,	9055.60		278.80 (102, 103)
103	TCLK0	194	8776.80		270.00 (103, 104)
104	PV_{DD}	195, 196, 197	8506.80		283.60 (104, 105)
105	TCLK1	198	8223.20		372.20 (105, 106)
106	EMU3	199	7851.00		270.40 (106, 107)
107	EMU0	200	7580.60		303.20 (107, 108)
108	EMU1	201	7277.40		300.80 (108, 109)
109	EMU2	202	6976.60		240.00 (109, 110)
110	MCBL / $\overline{MP}$	203	6736.60		342.60 (110, 111)
111	CV_{SS}	204, 205, 206	6394.00		203.00 (111, 112)
112	A23	207	6191.00		295.60 (112, 113)
113	A22	208	5895.40		330.80 (113, 114)
114	V_{DDL}	209, 210, 211	5564.60		180.40 (114, 115)
115	V_{DDL}	212, 213, 214	5384.20		397.40 (115, 116)
116	A21	215	4986.80	484.80	282.00 (116, 117)
117	A20	216	4704.80		338.00 (117, 118)
118	V_{SSL}	217, 218, 219	4366.80		180.40 (118, 119)
119	DV_{SS}	220, 221, 222	4186.40		322.60 (119, 120)
120	A19	223	3863.80		277.40 (120, 121)
121	AV_{DD}	224, 225, 226	3586.40		295.60 (121, 122)
122	A18	227	3290.80		276.20 (122, 123)
123	A17	228	3014.60		290.20 (123, 124)
124	A16	229	2724.40		267.00 (124, 125)
125	A15	230	2457.40		284.80 (125, 126)
126	A14	231	2172.60		346.60 (126, 127)
127	A13	232	1826.00		276.00 (127, 128)
128	A12	233	1550.00		278.20 (128, 129)
129	A11	234	1271.80		282.80 (129, 130)
130	AV_{DD}	235, 236, 237,	989.00		273.80 (130, 131)
131	A10	238	715.20		274.20 (131, 132)
132	CV_{SS}	239, 240, 241	441.00		
	N/C	242, 243, 244			

MECHANICAL DATA

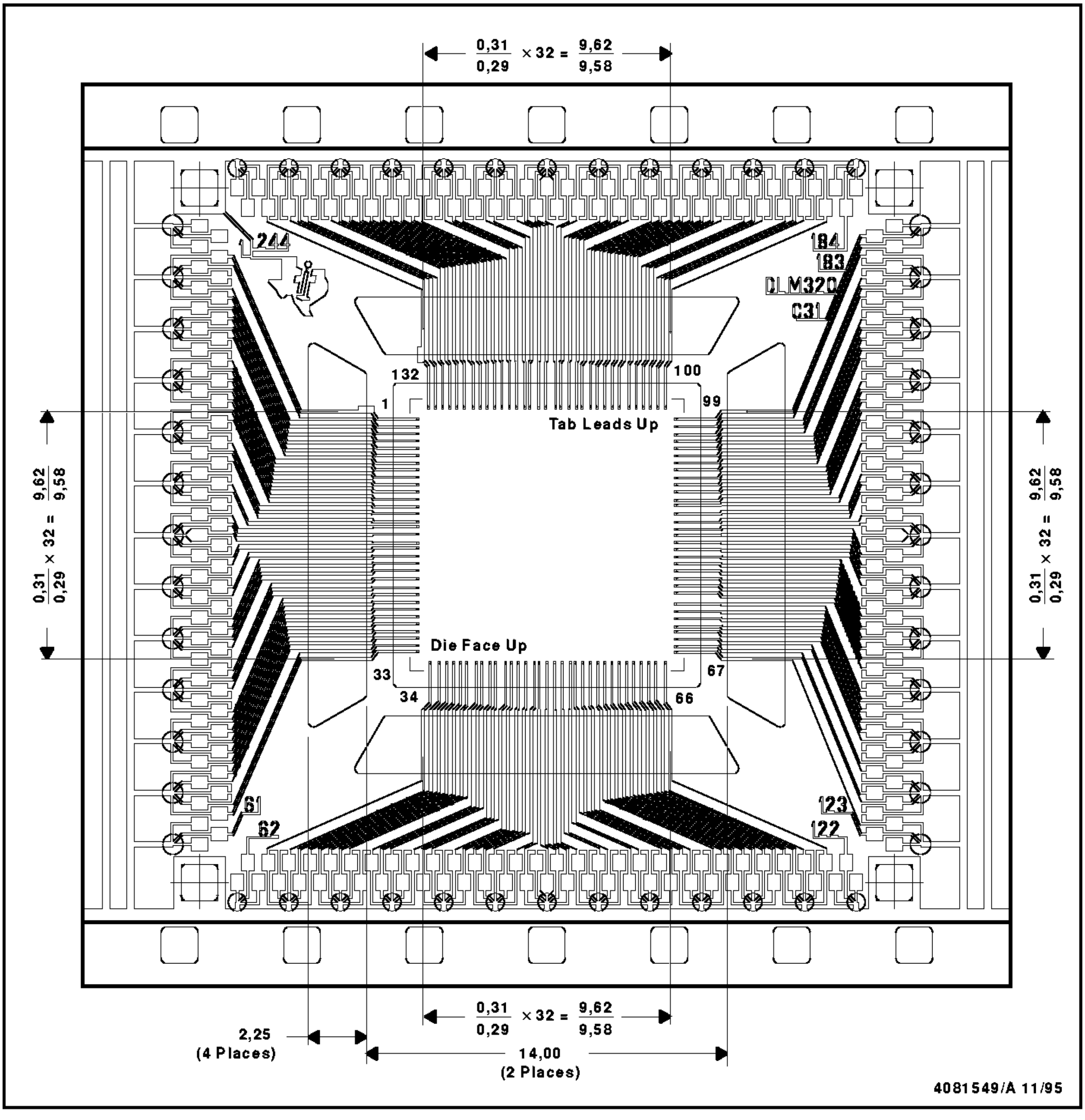
TA (35 OR 70 mm WITH PROTECTIVE FILM) **SMJ320C31 244-PIN TAB FRAME (PG2) SOCKET, 132 OLB/ILB 0,30-mm PITCH**



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The OLB lead width is 0,120 ± 0,03 mm.
D. The ILB lead width is 0,0832 ± 0,015 mm.
E. The tape width is 35 mm.
F. The TA is encapsulated die with polyimide overcoat.

MECHANICAL DATA

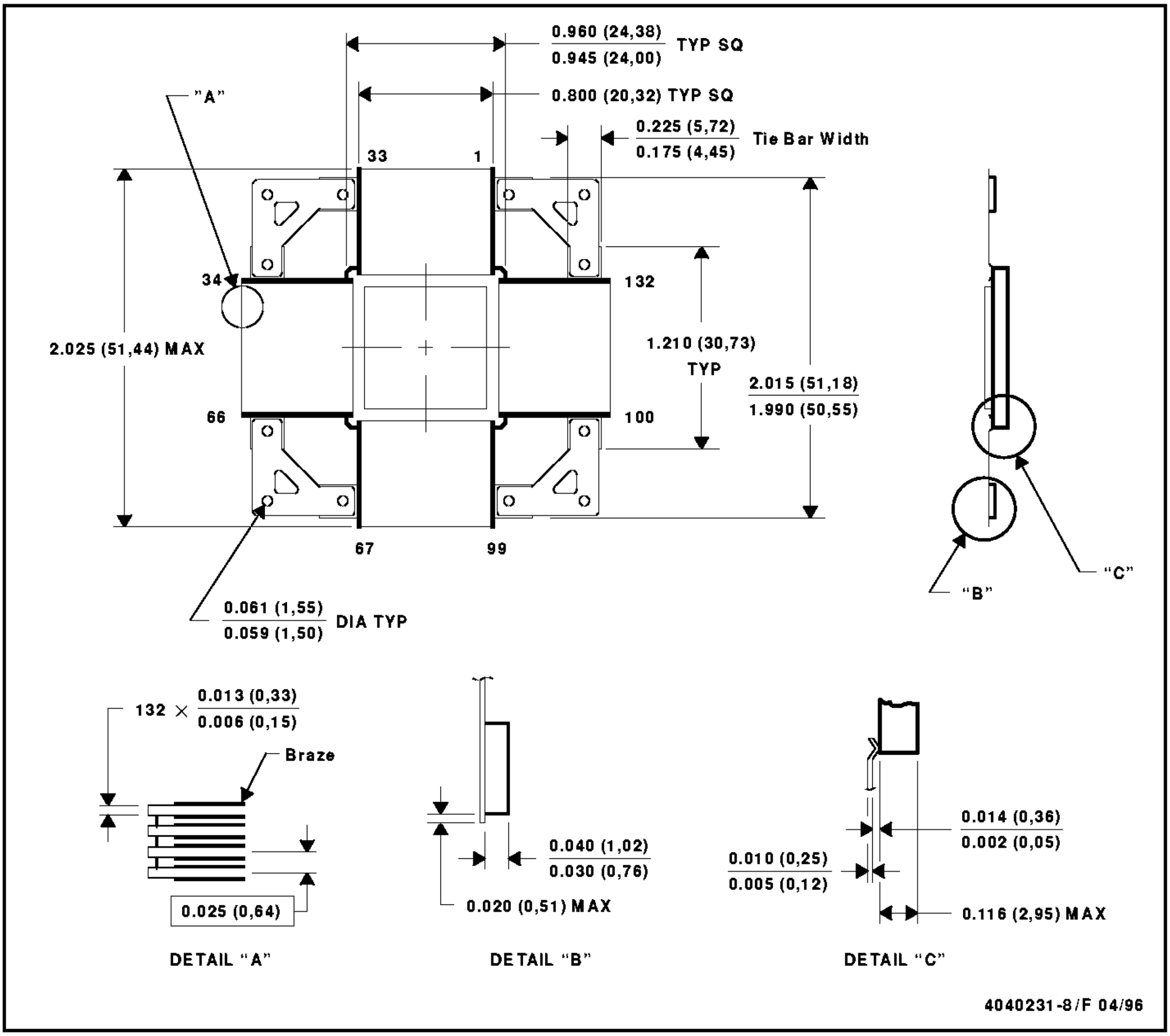
TB (35 OR 70 mm WITHOUT PROTECTIVE FILM) SMJ320C31 244-PIN TAB FRAME (PG2) SOCKET, 132 OLB/ILB 0,30-mm PITCH



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. The OLB lead width is 0,120 ± 0,03 mm.
D. The ILB lead width is 0,0832 ± 0,015 mm.
E. The tape width is 35 mm.
F. The TB is bare die.

MECHANICAL DATA

HFG (S-CQFP-F132) **CERAMIC QUAD FLATPACK WITH TIE-BAR**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
D. This package can be hermetically sealed with a metal lid.
E. The terminals will be gold plated.

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\theta JA}$	2.1
$R_{\theta JC}$	44.3

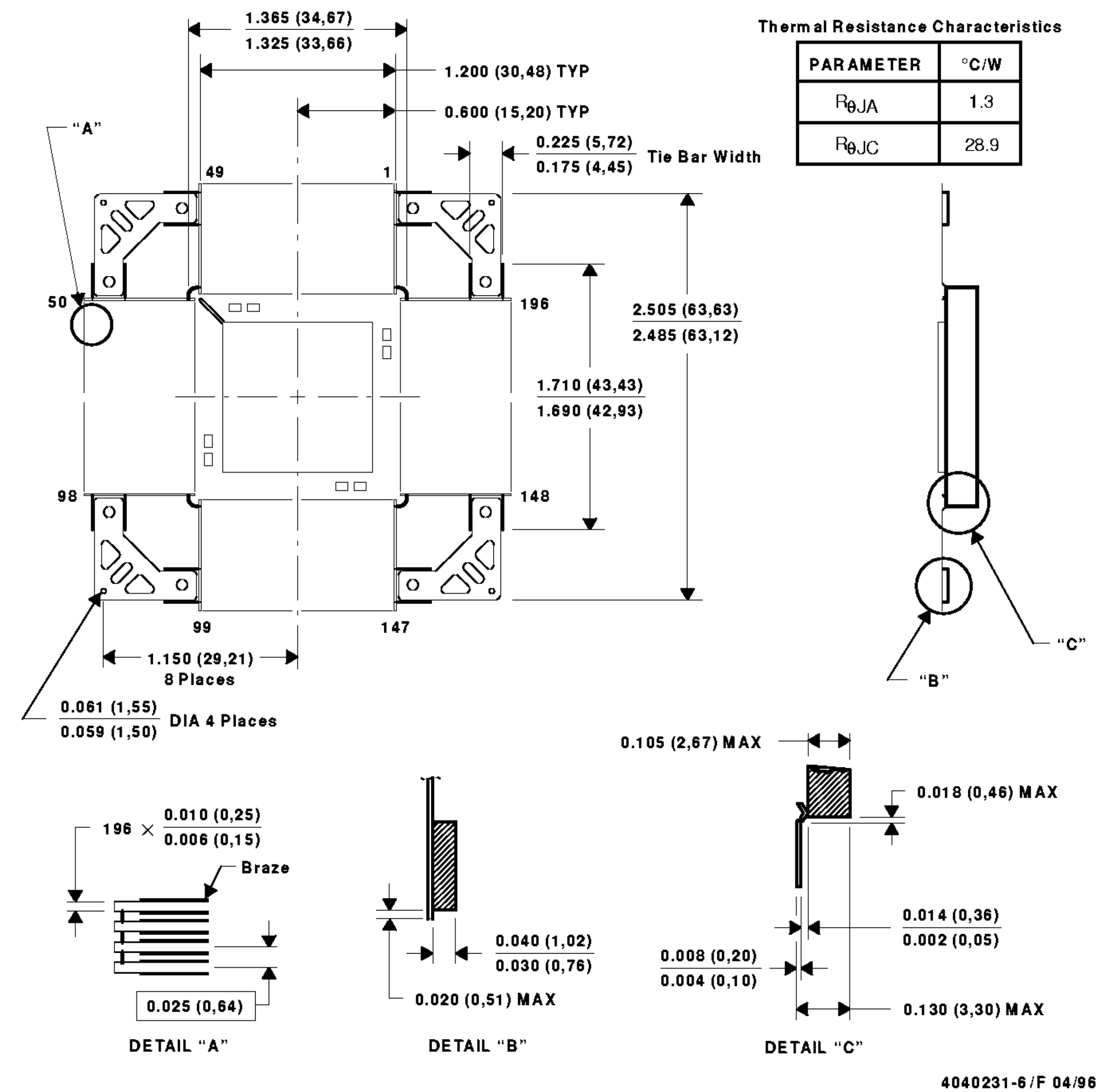
The above data applies to the SMJ320C31 132-pin QFP.

MECHANICAL DATA

HFG (S-CQFP-F196) **CERAMIC QUAD FLATPACK WITH TIE BAR**

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\theta JA}$	1.3
$R_{\theta JC}$	28.9

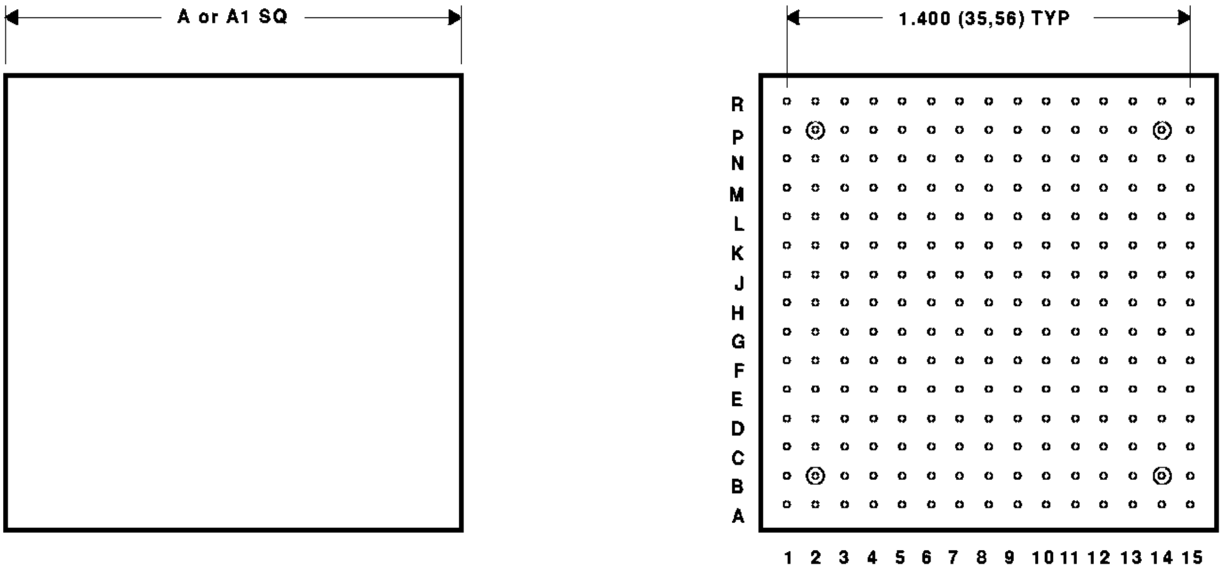


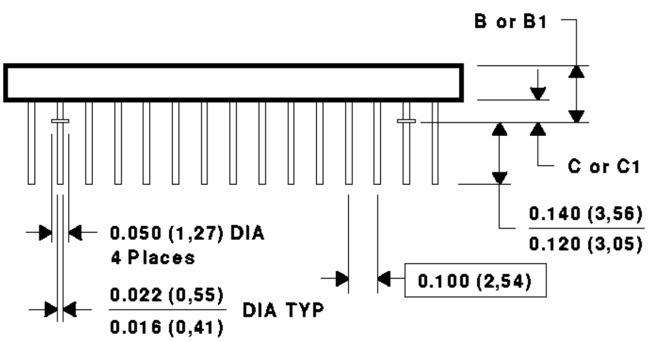
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to nonconductive tie-bar carrier
D. This package can be hermetically sealed with a metal lid.
E. The terminals will be gold plated.
F. Falls within JEDEC MO-113 AB

The above data applies to the SMJ320C30 196-pin QFP.

MECHANICAL DATA

GA-GB (S-CPGA-P15 X 15) **CERAMIC PIN GRID ARRAY PACKAGE**





DIM	MIN	MAX	Notes
A	1.540 (39,12)	1.590 (40,38)	Large Outline
A1	1.480 (37,59)	1.535 (38,99)	Small Outline
B	0.110 (2,79)	0.205 (5,21)	Cavity Up
B1	0.095 (2,41)	0.205 (5,21)	Cavity Down
C	0.040 (1,02)	0.060 (1,52)	Cavity Up
C1	0.025 (0,63)	0.060 (1,52)	Cavity Down
MAXIMUM PINS WITHIN MATRIX – 225			

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Index mark may appear on top or bottom depending on package vendor.
D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edges of the ceramic.
E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
F. The pins can be gold plated or solder dipped.
G. Falls within MIL-STD-1835 CMGA7-PN and CMGA19-PN and JEDEC MO-067AG and MO-066AG, respectively

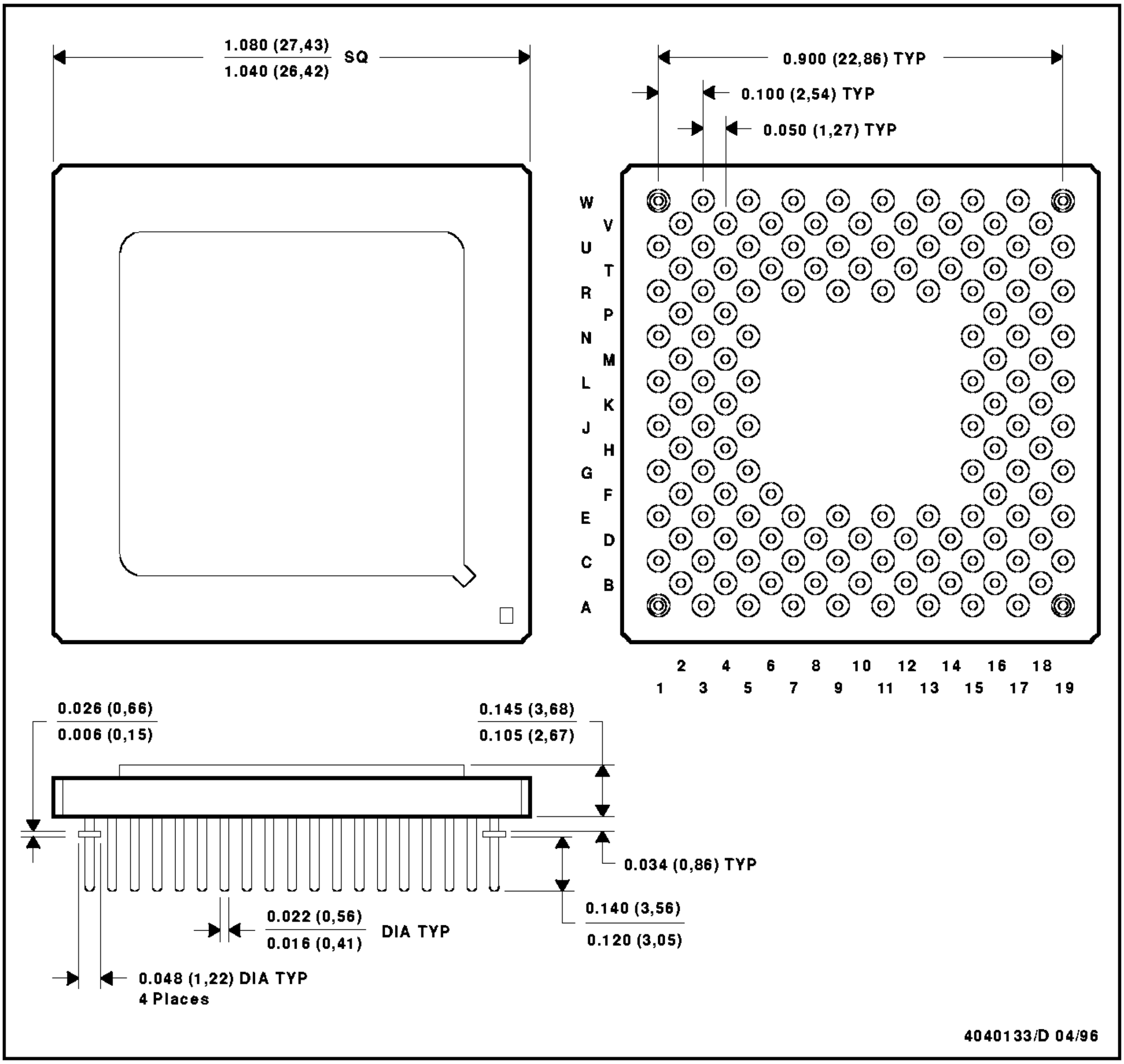
Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\theta JA}$	1.1
$R_{\theta JC}$	26.6

The above data applies to the SMJ320C30 181-pin PGA.

MECHANICAL DATA

GFA (S-CPGA-P141) **CERAMIC PIN GRID ARRAY PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-128

Thermal Resistance Characteristics

PARAMETER	°C/W
$R_{\theta JA}$	4.3
$R_{\theta JC}$	39.0

The above data applies to the SMJ320C31 141-pin PGA.

IMPORTANT NOTICE