ISP1110

Universal Serial Bus transceiver with UART signaling

Rev. 01 — 23 March 2006 Product data sheet

1. General description

The ISP1110 is a Universal Serial Bus (USB) transceiver that supports Universal Asynchronous Receiver-Transmitter (UART) signaling mode.

The ISP1110 USB transceiver is fully compliant with *Universal Serial Bus Specification Rev. 2.0*. The ISP1110 can transmit and receive USB data at full-speed (12 Mbit/s).

The ISP1110 transceiver allows USB Application Specific Integrated Circuits (ASICs) with I/O power supply voltage from 1.65 V to 2.85 V to interface to the physical layer of the USB. The transceiver has an integrated 5 V-to-3.3 V voltage regulator for direct powering through USB supply line V_{BUS} and an integrated voltage detector to detect the presence of the V_{BUS} voltage on the $V_{CC(5V0)}$ pin. When V_{BUS} is present, the transceiver is in USB mode. When V_{BUS} is not present, the transceiver can be set to UART signaling mode.

The ISP1110 transceiver is available in HBCC16 lead-free and halogen-free package.

2. Features

- Fully complies with *Universal Serial Bus Specification Rev. 2.0*
- Supports USB data transfer at full-speed (12 Mbit/s)
- Integrated DP pull-up resistor to reduce external components
- Implemented internal DP pull-up resistor as described in *ECN_27%_Resistor*
- Integrated 5 V-to-3.3 V voltage regulator to power through USB line V_{BUS}
- V_{BUS} voltage presence is indicated on pin VBUSDET
- Pins VP and VM function in bidirectional mode, allowing pin count saving for ASIC interface
- Used as a USB peripheral transceiver
- Stable RCV output during Single-Ended Zero (SE0) condition
- Two single-ended receivers with hysteresis
- Low-power operation
- Supports 2.8 V UART signaling mode on the DP and DM lines
- Supports $V_{CC(I/O)}$ voltage range from 1.65 V to 2.85 V
- Supports $V_{CC(UART)}$ voltage range from 2.7 V to 4.5 V
- Off-state supply current from $V_{CC(UART)}$ is less than 3 μA
- Static current from $V_{CC(I/O)}$ is less than 3 μA (typical 1 μA)
- Available in small HBCC16 (3×3 mm^2) lead-free and halogen-free package

3. Applications

- Mobile phone
- Personal Digital Assistant (PDA)
- Other portable devices

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
ISP1110VH	HBCC16	plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 × 3 × 0.65 mm	SOT639-2

5. Block diagram

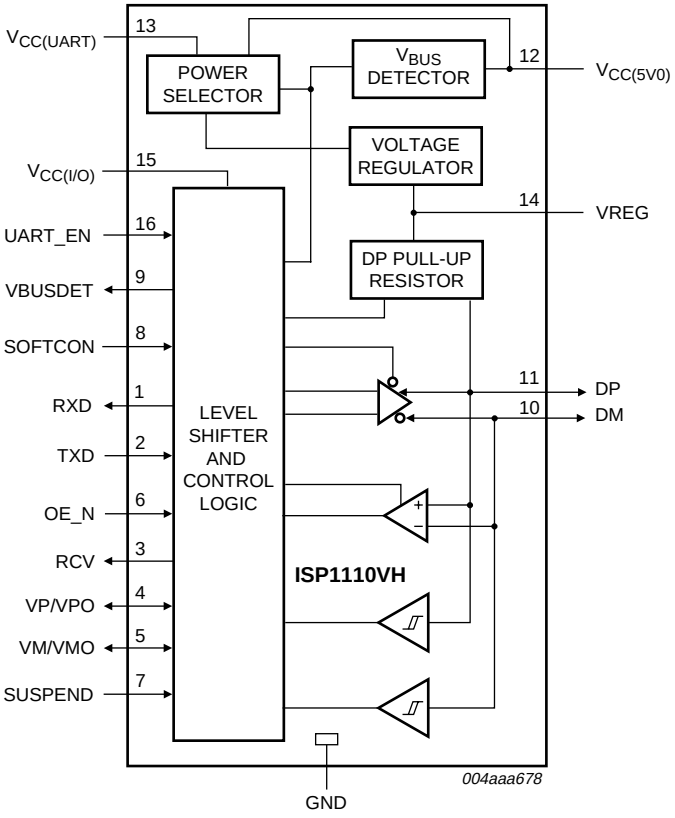
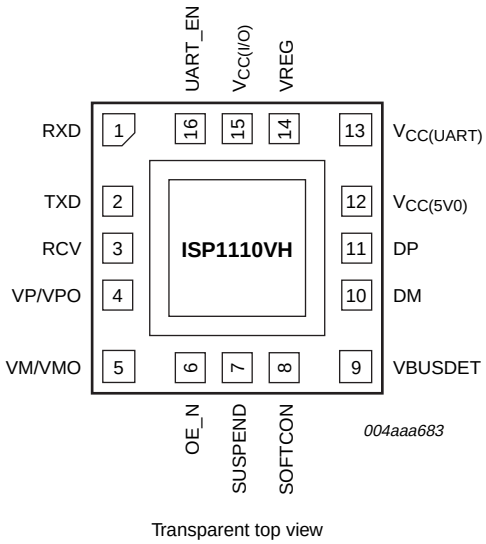


Fig 1. Block diagram

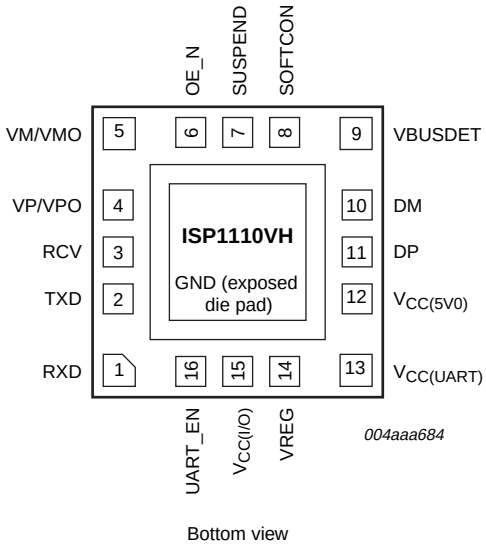
6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration HBCC16; top view



Bottom view

Fig 3. Pin configuration HBCC16; bottom view

6.2 Pin description

Table 2: Pin description

Symbol [1]	Pin	Type	Description
RXD	1	O	UART RXD output to microcontroller (CMOS level with respect to $V_{CC(I/O)}$); driven LOW in USB mode output pad; push pull; 4 mA output drive; CMOS
TXD	2	I	UART TXD input from microcontroller (CMOS level with respect to $V_{CC(I/O)}$) input pad; push pull; CMOS
RCV	3	O	differential data receiver output (CMOS level with respect to $V_{CC(I/O)}$); driven LOW when input SUSPEND is HIGH; the output state of RCV is preserved and stable during an SE0 condition; driven LOW when in UART mode output pad; push pull; 4 mA output drive; CMOS
VP/VPO	4	I/O	single-ended DP receiver output VP (CMOS level with respect to $V_{CC(I/O)}$); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VPO; see Table 4 and Table 5 bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
VM/VMO	5	I/O	single-ended DM receiver output VM (CMOS level with respect to $V_{CC(I/O)}$); for external detection of SE0, error conditions and speed of connected device; this pin also acts as drive data input VMO; see Table 4 and Table 5 bidirectional pad; push-pull input; 3-state output; 4 mA output drive; CMOS
OE_N	6	I	USB output enable (CMOS level with respect to $V_{CC(I/O)}$, active LOW); enables the transceiver to transmit data on the USB bus; this pin is ignored when in UART mode input pad; push pull; CMOS
SUSPEND	7	I	suspend input (CMOS level with respect to $V_{CC(I/O)}$); a HIGH level enables low-power state while the USB bus is inactive and drives output RCV to a LOW level; this pin is ignored when in UART mode input pad; push pull; CMOS
SOFTCON	8	I	software controlled USB connection input; a HIGH level enables the internal DP pull-up resistor when VBUSDET is HIGH; this pin is ignored when in UART mode input pad; push pull; CMOS
VBUSDET	9	O	V_{BUS} indicator output (CMOS level with respect to $V_{CC(I/O)}$); when $V_{BUS} > V_{CC(5V0)th}$, then VBUSDET = HIGH and when $V_{BUS} < V_{CC(5V0)th}$, then VBUSDET = LOW output pad; push pull; 4 mA output drive; CMOS
DM	10	AI/O	**USB mode —** Negative USB data bus connection (analog, bidirectional, differential) **UART mode —** UART TXD line (digital output)
DP	11	AI/O	**USB mode —** Positive USB data bus connection (analog, bidirectional, differential) **UART mode —** UART RXD line (digital input)

Table 2: Pin description…*continued*

Symbol [1]	Pin	Type	Description
$V_{CC(5V0)}$	12	-	supply voltage input (4.0 V to 5.5 V); can be directly connected to USB line V_{BUS}
$V_{CC(UART)}$	13	-	supply voltage input (2.7 V to 4.5 V) for the UART signaling
VREG	14	-	internal regulator output; a decoupling capacitor of at least 0.1 µF is required
$V_{CC(I/O)}$	15	-	supply voltage for digital I/O pins (1.65 V to 2.85 V). When $V_{CC(I/O)}$ is not connected, the DP and DM pins are in off-state. This supply pin is totally independent of $V_{CC(5V0)}$ and VREG, and must never exceed VREG.
UART_EN	16	I	enable UART signaling mode when $V_{CC(5V0)}$ is not present input pad; push-pull; CMOS
GND	exposed die pad	-	ground supply; down-bonded to the exposed die pad (heat sink); to be connected to the PCB ground

[1] Symbol names ending with underscore N, for example, _N, indicate active LOW signals.

7. Functional description

7.1 Modes of operation

The ISP1110 supports two modes of operation:

- USB mode (3.3 V signaling)
- UART mode (2.8 V signaling)

Table 3 shows the behavior of the ISP1110 in different power modes.

Table 3: Device operation mode summary

$V_{CC(I/O)}$	$V_{CC(5V0)} = V_{BUS}$	UART_EN	DP and DM	RXD
off	X	X	off-state	off-state
on	off	LOW	off-state	driven (LOW)
on	off	HIGH	UART mode	driven (DP)
on	on	X	USB mode	driven (LOW)

7.1.1 USB mode

When the ISP1110 is in USB mode, pins DP and DM work as the USB D+ and D– lines, respectively. The DP and DM driver is powered by VREG. The USB function is compatible with the ISP1102 transceiver.

When the ISP1110 is in USB mode, the TXD input pin is ignored and the RXD output pin is driven LOW.

The ISP1110 is in USB mode when $V_{CC(5V0)} > V_{CC(5V0)th}$.

A short description of the USB detection sequence is:

1. The phone is connected to the USB port of a powered PC.
2. The ISP1110 detects V_{BUS} is above $V_{CC(5V0)th}$. The ISP1110 enters USB mode and the Analog USB Transceiver (ATX) is powered by VREG.
3. If the phone is switched off ($V_{CC(I/O)}$ is not present), then the DP and DM pins of the ISP1110 remain at high-impedance and the PC will not detect any device attachment.
4. If the phone is switched on ($V_{CC(I/O)}$ is present), then the ISP1110 will drive the VBUSDET pin to a HIGH level.
5. The phone processor detects that pin VBUSDET is HIGH. If the phone system software is ready for USB operation, the phone processor will assert pin SOFTCON.
6. The ISP1110 will enable the DP pull-up resistor ($R_{PU(DP)}$).
7. The PC detects DP at the HIGH level and starts USB full-speed enumeration.
8. The PC loads the driver for the phone, if enumeration is successful.

For the flowchart, see Section 7.1.3.

7.1.2 UART mode

When the ISP1110 is in UART mode, the DP and DM driver is powered by 2.8 V. The ISP1110 works as a level shifter between these pairs of pins:

- From TXD ($V_{CC(I/O)}$ level) to DM (2.8 V level)
- From DP (2.8 V level) to RXD ($V_{CC(I/O)}$ level).

When the ISP1110 is in UART mode, the USB differential receiver is disabled. The SUSPEND and SOFTCON input pins are ignored. The RCV pin is driven LOW. The VP/VPO and VM/VMO pins are driven LOW, if OE_N is HIGH. The VP/VPO and VM/VMO pins are 3-state LOW, if OE_N is LOW.

The ISP1110 is in UART mode when $V_{CC(5V0)} < V_{CC(5V0)th}$.

A short description of the UART detection sequence is:

1. The phone is switched on ($V_{CC(I/O)}$ is present).
2. If V_{BUS} is off, the ISP1110 will drive VBUSDET to a LOW level. The ATX is powered by 2.8 V.
3. The ISP1110 will enter UART signaling mode, if UART_EN is HIGH.

For the flowchart, see Section 7.1.3.

7.1.3 Mode detection flowchart

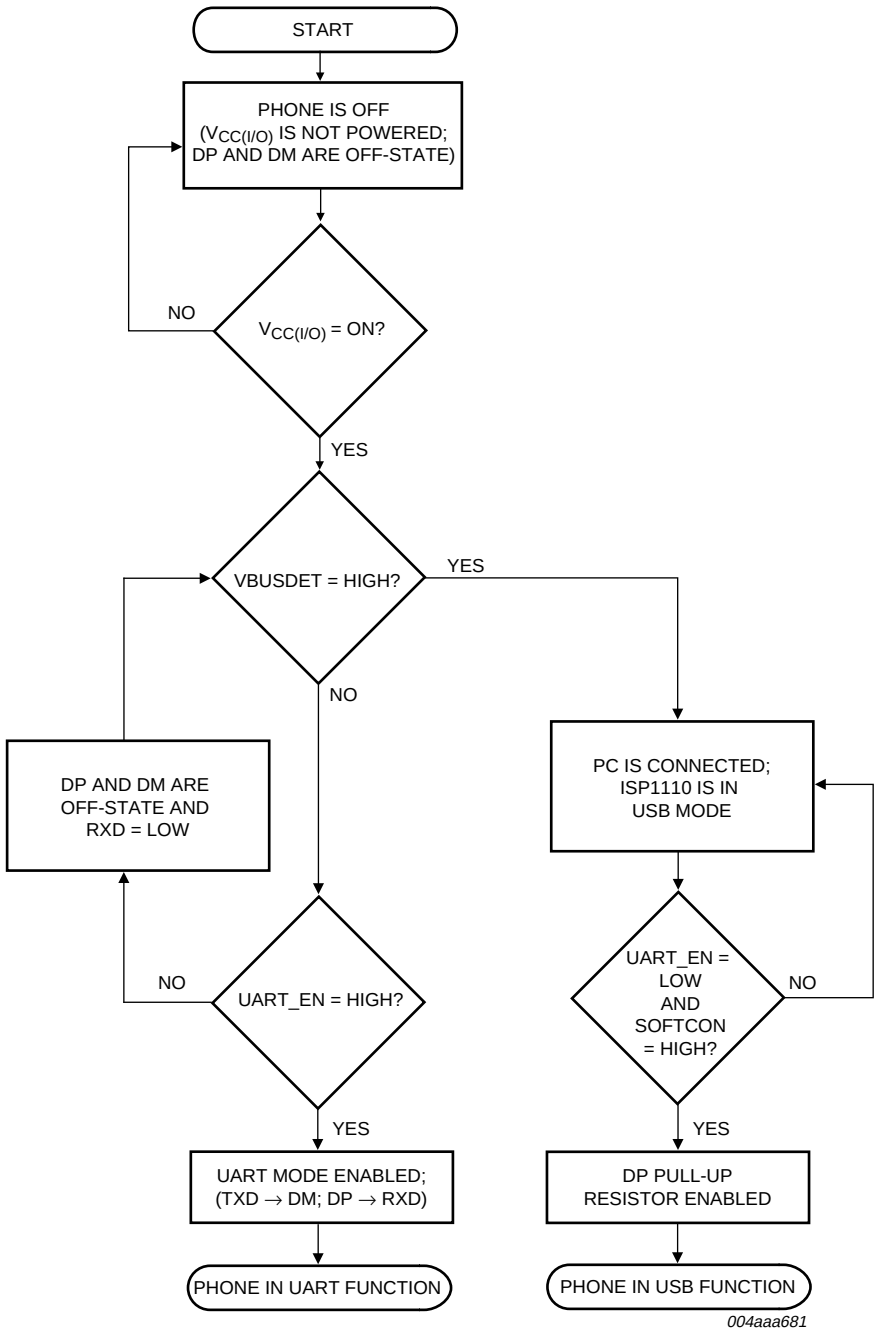


Fig 4. ISP1110 mode detection flowchart

7.1.4 Mode switching time

When the USB cable is connected, the ISP1110 is in USB mode. When the USB cable is removed and the UART cable is connected, the ISP1110 may switch to UART mode as long as the VBUSDET output is LOW. On the other hand, if the UART cable is removed and the USB cable is connected, the ISP1110 can switch to USB mode.

UART mode cannot be enabled until the voltage on $V_{CC(5V0)}$ drops below the VBUSDET threshold (0.8 V to 4.0 V). Therefore, the time required to switch from USB mode to UART mode is determined by the RC discharge time on the V_{BUS} line. Given that $V_{CC(5V0)}$ = 5.0 V, R = 100 kΩ and C = 1 μF, the discharge time is less than 200 ms (from 5 V to 0.8 V). Assume the detection of the UART cable connect or disconnect is very fast (within 1 ms), the total switching time from the USB cable removal to entering UART mode can be less than 200 ms. The total switching time from the UART cable removal to entering USB mode can be less than 200 ms.

When VBUSDET becomes LOW, it is recommended that you wait for 50 ms before asserting UART_EN. This is because there is no hysteresis built for the VBUSDET threshold detector.

The time between VBUSDET going HIGH and SOFTCON assertion is 0 ms to 100 ms, according to *Universal Serial Bus Specification Rev. 2.0, Section 7.1.7.3*.

7.2 Analog USB Transceiver (ATX)

The ISP1110 ATX supports USB full-speed (12 Mbit/s) signaling. The ATX function is compatible with the ISP1102 transceiver. Table 4 shows the function of the ATX.

Table 4: USB function

SUSPEND	OE_N	DP and DM	RCV	VP/VPO	VM/VMO	Function
LOW	LOW	driving/receiving	active	VPO input	VMO input	normal driving (differential receiver active)
LOW	HIGH	receiving [1]	active	VP output	VM output	receiving
HIGH	LOW	driving	inactive [2]	VPO input	VMO input	driving during suspend (differential receiver inactive)
HIGH	HIGH	high-Z [1]	inactive [2]	VP output	VM output	low-power state

[1] Signal levels on the DP and DM pins are determined by other USB devices and external pull-up or pull-down resistors.

[2] In Suspend mode (SUSPEND = HIGH), the differential receiver is inactive and output RCV is always LOW. The resume signaling is detected through single-ended receivers VP/VPO and VM/VMO.

Table 5: USB driving function (pin OE_N = LOW)

VM/VMO	VP/VPO	Data
LOW	LOW	SE0
LOW	HIGH	differential logic 1
HIGH	LOW	differential logic 0
HIGH	HIGH	illegal state

Table 6: USB receiving function (pin OE_N = HIGH)

DP, DM	RCV	VP/VPO	VM/VMO
Differential logic 0	LOW	LOW	HIGH
Differential logic 1	HIGH	HIGH	LOW
SE0	RCV* [1]	LOW	LOW

[1] RCV* denotes the signal level on output RCV just before the SE0 state occurs. This level is stable during the SE0 period.

7.3 V_{BUS} detector

The V_{BUS} detector provides voltage level detection on V_{BUS}, if V_{BUS} is connected to $V_{CC(5V0)}$. If V_{BUS} is greater than the V_{BUS} valid threshold $V_{CC(5V0)th}$, pin VBUSDET will output a HIGH level. Otherwise, pin VBUSDET will output a LOW level.

The V_{BUS} detector is powered by $V_{CC(I/O)}$.

7.4 DP pull-up resistor

The internal DP pull-up resistor is connected between the VREG and DP pins, if pin SOFTCON is a HIGH level.

The pull-up resistor is context variable, as described in document *ECN_27%_Resistor*. The variable pull-up resistor hardware is implemented here to meet the *ECN_27%_Resistor* specification.

7.5 DC-DC regulator

In USB mode, when $V_{CC(5V0)}$ = 4.0 V to 5.5 V, the regulator will output 3.0 V to 3.6 V. In UART mode, when $V_{CC(UART)}$ = 2.7 V to 4.5 V, the regulator will output 2.35 V to 2.85 V.

A 0.1 μF capacitor is required to connect to the VREG pin.

7.6 Power selector

When VBUSDET = HIGH, the regulator will be powered by $V_{CC(5V0)}$. When VBUSDET = LOW and UART_EN = HIGH, the regulator will be powered by $V_{CC(UART)}$.

When $V_{CC(I/O)}$ is not connected, the DP and DM output will be in off-state.

For proper operation, the $V_{CC(I/O)}$ voltage must not exceed VREG.

8. Limiting values

Table 7: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)			–0.5	+6.0	V
$V_{CC(UART)}$	supply voltage (UART)			–0.5	+5.5	V
$V_{CC(I/O)}$	input/output supply voltage			–0.5	+4.6	V
V_I	input voltage			–0.5	$V_{CC(I/O)}$ + 0.5 V	V
I_{lu}	latch-up current	V_I = –1.8 V to +5.4 V		-	100	mA
V_{ESD}	electrostatic discharge voltage	all pins; I_{LI} < 1 µA	[1]	–2000	+2000	V
		pins DP, DM, $V_{CC(5V0)}$, GND; I_{LI} < 3 µA; 1 µF capacitor on $V_{CC(5V0)}$	[1]	–3000	+3000	V
T_{stg}	storage temperature			–40	+125	°C

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor (Human Body Model).

9. Recommended operating conditions

Table 8: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		4.0	5.0	5.5	V
$V_{CC(UART)}$	supply voltage (UART)		2.7	-	4.5	V
$V_{CC(I/O)}$	input/output supply voltage		1.65	1.8	2.85	V
V_I	input voltage		0	-	$V_{CC(I/O)}$	V
$V_{IA(I/O)}$	input voltage on analog I/O pins	pins DP and DM	0	-	3.6	V
T_{amb}	ambient temperature		–40	-	+85	°C

10. Static characteristics

Table 9: Static characteristics: supply pins

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = –40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{O(VREG)}$	output voltage on pin VREG	USB mode	[1]	3.0	3.3	3.6	V
		UART mode		2.35	2.6	2.85	V
$I_{CC(5V0)}$	supply current (5.0 V)	USB mode; transmitting and receiving at 12 Mbit/s; C_L = 50 pF on pins DP and DM	[2]	-	4	8	mA
$I_{CC(UART)}$	supply current (UART)	UART mode; 921.6 kbit/s		-	-	4	mA
$I_{CC(I/O)}$	supply current on pin $V_{CC(I/O)}$	transmitting and receiving at 12 Mbit/s	[2]	-	1	2	mA
$I_{CC(5V0)(idle)}$	idle and SE0 supply current (5.0 V)	USB mode; idle: V_{DP} > 2.7 V, V_{DM} < 0.3 V; SE0: V_{DP} < 0.3 V, V_{DM} < 0.3 V	[3]	-	-	300	µA

Table 9: Static characteristics: supply pins *...continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{CC(I/O)(static)}$	static supply current on pin $V_{CC(I/O)}$			-	-	3	µA
$I_{CC(5V0)(susp)}$	Suspend mode supply current (5.0 V)	USB mode SUSPEND = HIGH	[3]	-	-	35	µA
$I_{CC(UART)(off)}$	off-state supply current (UART)	USB mode or UART_EN = LOW		-	-	3	µA
$V_{CC(5V0)th}$	supply voltage detection threshold (5.0 V)	1.65 V ≤ $V_{CC(I/O)}$ ≤ 2.85 V		0.8	-	4.0	V
$V_{CC(I/O)th}$	supply voltage detection threshold (I/O)			0.5	-	1.4	V

[1] The minimum voltage is 2.7 V in Suspend mode.

[2] Maximum value characterized only, not tested in production.

[3] Excluding any load current and source current to the DP/DM pull-up and pull-down resistors (200 µA typical).

Table 10: Static characteristics: digital pins

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{CC(I/O)}$ = 1.65 V to 2.85 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{CC(I/O)}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{CC(I/O)}$	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA		$V_{CC(I/O)}$ − 0.15 V	-	-	V
		I_{OH} = 2 mA		$V_{CC(I/O)}$ − 0.4 V	-	-	V
Leakage current							
I_{LI}	input leakage current		[1]	−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	10	pF
Example 1: $V_{CC(I/O)}$ = 1.8 V ± 0.15 V							
Input levels							
V_{IL}	LOW-level input voltage			-	-	0.5	V
V_{IH}	HIGH-level input voltage			1.2	-	-	V
Output levels							
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA		-	-	0.15	V
		I_{OL} = 2 mA		-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA		1.5	-	-	V
		I_{OH} = 2 mA		1.25	-	-	V

Table 10: Static characteristics: digital pins *...continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Example 2: $V_{CC(I/O)}$ = 2.775 V ± 0.075 V						
Input levels						
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{IH}	HIGH-level input voltage		3.0	-	-	V
Output levels						
V_{OL}	LOW-level output voltage	I_{OL} = 100 µA	-	-	0.15	V
		I_{OL} = 2 mA	-	-	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = 100 µA	2.55	-	-	V
		I_{OH} = 2 mA	2.3	-	-	V

[1] If $V_{CC(I/O)} \geq V_{CC(UART)}$, then the leakage current will be higher than the specified value when in UART mode.

Table 11: Static characteristics: analog I/O pins DP and DM

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input levels (USB mode)							
Differential receiver							
V_{DI}	differential input sensitivity	$\|V_{DP} - V_{DM}\|$		0.2	-	-	V
V_{CM}	differential common-mode range	includes V_{DI} range		0.8	-	2.5	V
Single-ended receiver							
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Input levels (UART mode)							
V_{IL}	LOW-level input voltage			−0.3	-	+0.8	V
V_{IH}	HIGH-level input voltage			2.0	-	3.0	V
V_{hys}	hysteresis voltage			0.4	-	0.7	V
Output levels (USB mode)							
V_{OL}	LOW-level output voltage	R_L = 1.5 kΩ to 3.6 V		-	-	0.3	V
V_{OH}	HIGH-level output voltage	R_L = 15 kΩ to GND	[1]	2.8	-	3.6	V
Output levels (UART mode)							
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		−0.1	-	+0.37	V
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		2.16	-	2.85	V
Leakage current							
I_{LZ}	off-state leakage current			−1	-	+1	µA
Capacitance							
C_{in}	input capacitance	pin to GND		-	-	10	pF
Resistance							
Z_{DRV}	driver output impedance	steady-state drive	[2]	34	39	44	Ω

Table 11: Static characteristics: analog I/O pins DP and DM...*continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Z_{INP}	input impedance			10	-	-	MΩ
$R_{PU(DP)}$	pull-up resistance on pin DP	bus idle		900	-	1575	Ω
		bus active		1425	-	3090	Ω
Termination							
V_{TERM}	termination voltage	for upstream port pull-up ($R_{PU(DP)}$)	[3] [4]	3.0	-	3.6	V

[1] $V_{OH(min)}$ = VREG − 0.2 V.

[2] Includes external resistors of 33 Ω ± 1 % on pins DP and DM.

[3] This voltage is available at pin VREG.

[4] The minimum voltage is 2.7 V in Suspend mode.

11. Dynamic characteristics

Table 12: Dynamic characteristics: analog I/O pins DP and DM

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Driver characteristics (UART mode)							
t_{LR}	rise time	C_L < 250 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 5	[1]	50	-	200	ns
t_{LF}	fall time	C_L < 250 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 5	[1]	50	-	200	ns
Driver characteristics (USB mode)							
t_{FR}	rise time	C_L = 50 pF to 125 pF; 10 % to 90 % of $\|V_{OH} - V_{OL}\|$; see Figure 5		4	-	20	ns
t_{FF}	fall time	C_L = 50 pF to 125 pF; 90 % to 10 % of $\|V_{OH} - V_{OL}\|$; see Figure 5		4	-	20	ns
FRFM	differential rise time/fall time matching	excluding the first transition from Idle state	[2]	90	-	111.1	%
V_{CRS}	output signal crossover voltage	excluding the first transition from Idle state; see Figure 6	[3]	1.3	-	2.0	V
Driver timing							
$t_{PLH(drv)}$	driver propagation delay (LOW to HIGH)	VPO, VMO to DP, DM; see Figure 6 and Figure 9		-	-	18	ns
$t_{PHL(drv)}$	driver propagation delay (HIGH to LOW)	VPO, VMO to DP, DM; see Figure 6 and Figure 9		-	-	18	ns
t_{PHZ}	driver disable delay from HIGH level	OE_N to DP, DM; see Figure 7 and Figure 10		-	-	15	ns
t_{PLZ}	driver disable delay from LOW level	OE_N to DP, DM; see Figure 7 and Figure 10		-	-	15	ns
t_{PZH}	driver enable delay to HIGH level	OE_N to DP, DM; see Figure 7 and Figure 10		-	-	15	ns

Table 12: Dynamic characteristics: analog I/O pins DP and DM...*continued*

$V_{CC(5V0)}$ = 4.0 V to 5.5 V; $V_{CC(UART)}$ = 2.7 V to 4.5 V; $V_{CC(I/O)}$ = 1.65 V to 2.85 V; T_{amb} = −40 °C to +85 °C.
Typical values are at $V_{CC(5V0)}$ = 5.0 V; $V_{CC(UART)}$ = 2.8 V; $V_{CC(I/O)}$ = 1.8 V; T_{amb} = +25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZL}	driver enable delay to LOW level	OE_N to DP, DM; see Figure 7 and Figure 10	-	-	15	ns
Receiver timings						
Differential receiver						
$t_{PLH(rcv)}$	receiver propagation delay (LOW to HIGH)	DP, DM to RCV; see Figure 8 and Figure 11	-	-	15	ns
$t_{PHL(rcv)}$	receiver propagation delay (HIGH to LOW)	DP, DM to RCV; see Figure 8 and Figure 11	-	-	15	ns
Single-ended receiver						
$t_{PLH(se)}$	single-ended propagation delay (LOW to HIGH)	DP, DM to VP/VPO, VM/VMO; see Figure 8 and Figure 11	-	-	18	ns
$t_{PHL(se)}$	single-ended propagation delay (HIGH to LOW)	DP, DM to VP/VPO, VM/VMO; see Figure 8 and Figure 11	-	-	18	ns

[1] For UART TXD on pin DM.

[2] t_{FR} / t_{FF}.

[3] Characterized only, not tested. Limits guaranteed by design.

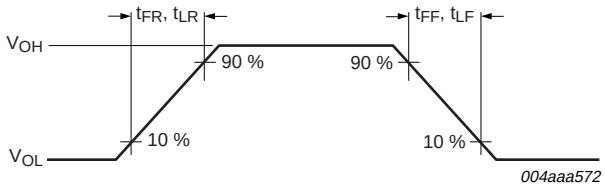


Fig 5. Rise time and fall time

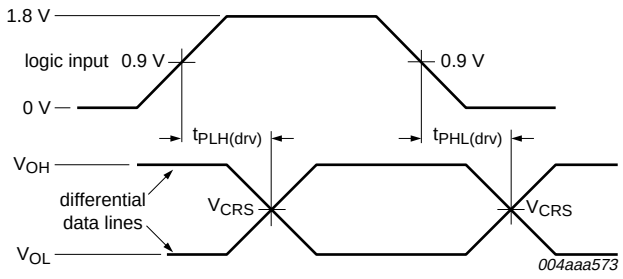


Fig 6. Timing of VPO and VMO to DP and DM

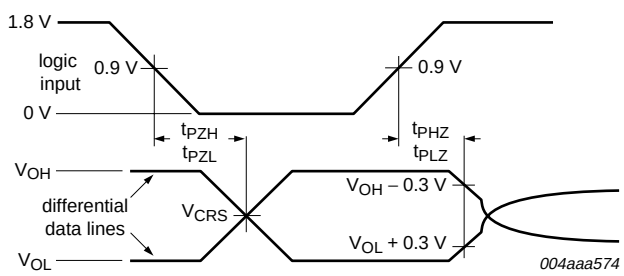


Fig 7. Timing of OE_N to DP and DM

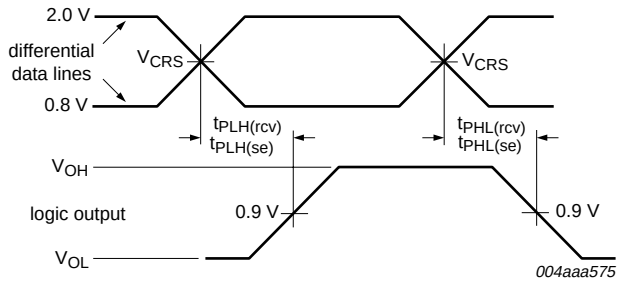
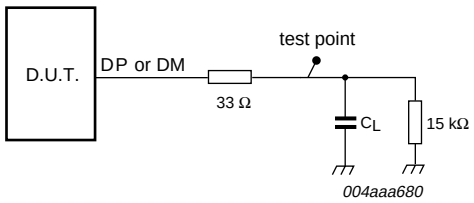


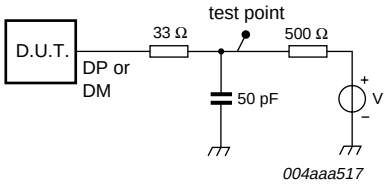
Fig 8. Timing of DP and DM to RCV, VP/VPO and VM/VMO

12. Test information



Load capacitance C_L = 50 pF (minimum or maximum timing)

Fig 9. Load on pins DP and DM



V = 0 V for t_{PZH} and t_{PHZ}

V = VREG for t_{PZL} and t_{PLZ}.

Fig 10. Load on pins DP and DM for enable time and disable time

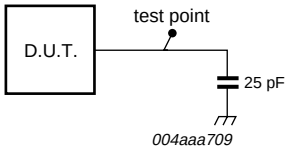
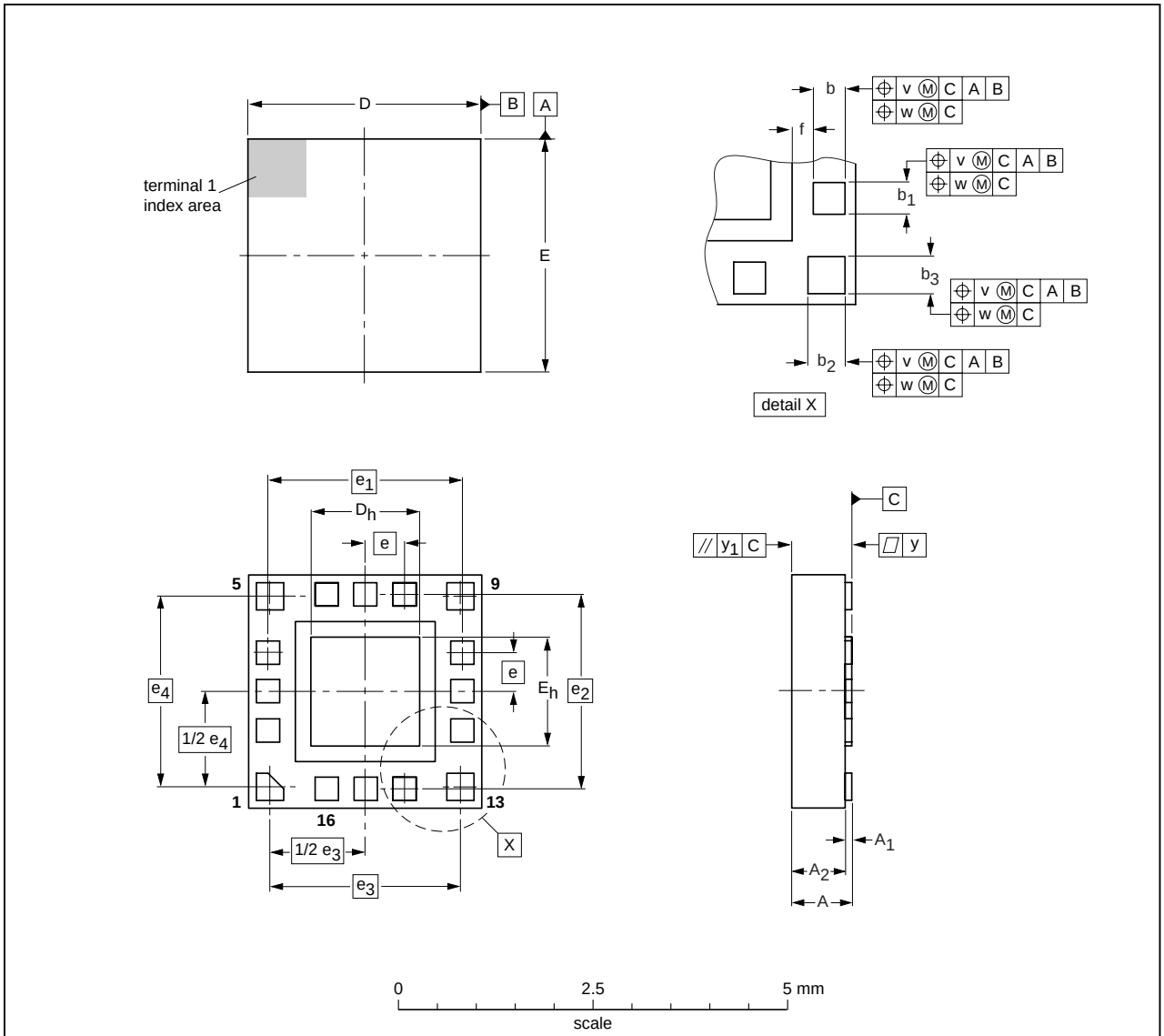


Fig 11. Load on pins VM/VMO, VP/VPO and RCV

13. Package outline

HBCC16: plastic thermal enhanced bottom chip carrier; 16 terminals; body 3 x 3 x 0.65 mm **SOT639-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	b_1	b_2	b_3	D	D_h	E	E_h	e	e_1	e_2	e_3	e_4	f	v	w	y	y_1
mm	0.8	0.10 0.05	0.7 0.6	0.33 0.27	0.33 0.27	0.38 0.32	0.38 0.32	3.1 2.9	1.45 1.35	3.1 2.9	1.45 1.35	0.5	2.5	2.5	2.45	2.45	0.23 0.17	0.08	0.1	0.05	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT639-2		MO-217				01-11-13 03-03-12

Fig 12. Package outline SOT639-2 (HBCC16)

14. Packing information

The ISP1110VH (HBCC16 package) is delivered on a Type A carrier tape, see Figure 13. The tape dimensions are given in Table 13.

The reel diameter is 330 mm. The reel is made of polystyrene and is not designed for use in a baking process.

The cumulative tolerance of 10 successive sprocket holes is ±0.02 mm. The camber must not exceed 1 mm in 100 mm.

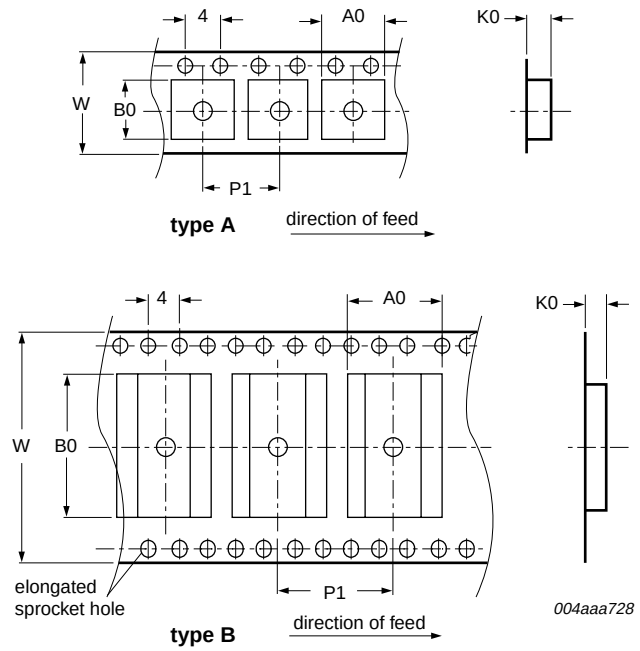


Fig 13. Carrier tape dimensions

Table 13: Type A carrier tape dimensions for the ISP1110VH

Dimension	Value	Unit
A0	3.3	mm
B0	3.3	mm
K0	1.1	mm
P1	8.0	mm
W	12.0 ± 0.3	mm

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 14: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	Soldering method	
	Wave	Reflow [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Abbreviations

Table 15: Abbreviations

Acronym	Description
ASIC	Application Specific Integrated Circuits
ATX	Analog USB Transceiver
CMOS	Complementary Metal-Oxide Semiconductor
HBM	Human Body Model
PC	Personal Computer
PDA	Personal Digital Assistant
RXD	Receive Data
SE0	Single-Ended Zero
TXD	Transmit Data
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus

17. References

[1] Universal Serial Bus Specification Rev. 2.0

[2] ECN_27%_Resistor (Pull-up/pull-down Resistors ECN)

18. Revision history

Table 16: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
ISP1110_1	20060323	Product data sheet	-	-	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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