

CMOS Image Resampling Sequencer

15, 18MHz

The TMC2301 is a VLSI circuit which supports image resampling, rotation, rescaling, and filtering by generating input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with external multiplier-accumulator control signals. The TMC2301 can process data fields of up to 4096 x 4096 multibit words at a clock rate of up to 18MHz. An IRS-based system can nearest-neighbor resample a 512 x 512 image in 15 milliseconds, translating, zooming, rotating, or warping it, depending on the transform parameter set loaded. A complete bilinear interpolation of the same image can be completed in 60 milliseconds. Image resampling speed is independent of the angle of rotation, degree of warp, or amount of zoom specified.

A high performance, TMC2301-based system can execute bilinear and cubic convolution algorithms that rotate images accurately and in real time. Keystone or other perspective correction, image plane distortion, and numerous other second order polynomial transformations can be programmed and executed under direct user control. Direct access to the interpolation coefficient lookup table allows dynamic modification of the algorithm.

Following an initialization with the transform parameters and control bits defining the operation to be executed, the IRS assumes control of the input and output data fields and executes unattended. Data word size is user selectable. All inputs except INTER and all outputs are registered on the rising edge of clock. All outputs are three-state controlled except ACC, CZERO, END, and DONE.

Fabricated in TRW's OMICRON-C™ one micron CMOS process, the TMC2301 operates at clock rates of up to 18MHz over the full commercial (0 to 70°C) temperature and 15MHz over the extended (-55 to +125°C) temperature and supply voltage ranges. All signals are TTL compatible.

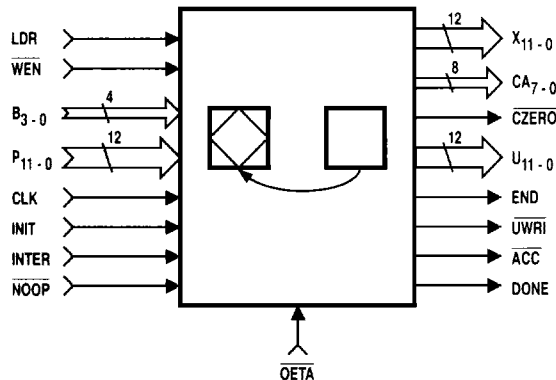
Features

- Rotation, Warping, Panning, Zooming, And Compression Of Images In Real Time
- 18MHz Clock Rate
- 4096 x 4096 Image Field Addressing Capability
- User-Selectable Nearest-Neighbor, Bilinear Interpolation, And Cubic Convolution Resampling Algorithms
- Static Convolutional Filtering Of Up To 16 x 16 Pixel Windows
- Single-Pass Or Two-Pass Convolution Operations
- Low Power-Consumption CMOS Process
- Single 5V Power Supply
- Available In A 68 Pin Grid Array And Low-Cost Plastic Leaded Chip Carrier (J-Bend)

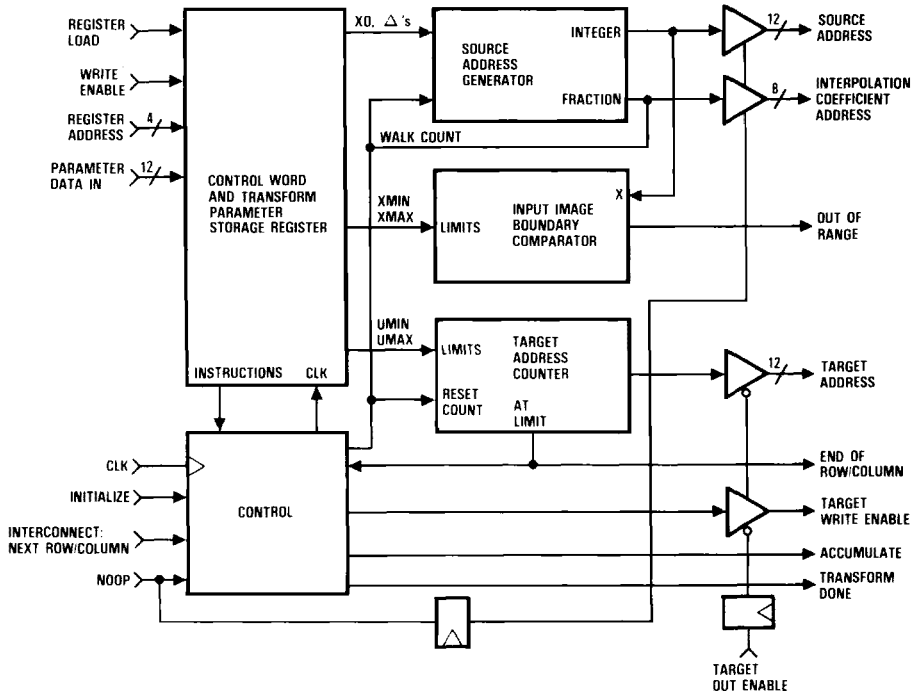
Applications

- Video Special-Effects Generators
- Image Recognition Systems, Robotics
- Artificial Intelligence
- High-Precision Image Registration (LANDSAT Processing)
- High-Speed Data Encoding/Decoding
- General Purpose Image Processing
- Image Data Compression

Logic Symbol



Functional Block Diagram



Pin Assignments — 68 Pin Grid Array, G8 or H8 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name
B2	INIT	K2	U ₁₀	K10	X ₁	B10	P ₆
B1	QETA	L2	U ₁₁	K11	X ₂	A10	P ₅
C2	INTER	K3	UWRI	J10	X ₃	B9	P ₄
C1	END	L3	ACC	J11	X ₄	A9	P ₃
D2	DONE	K4	CZERO	H10	X ₅	B8	P ₂
D1	U ₀	L4	CA ₀	H11	X ₆	A8	P ₁
E2	U ₁	K5	CA ₁	G10	X ₇	B7	P ₀
E1	U ₂	L5	V _{DD}	G11	X ₈	A7	CLK
F2	GND	K6	GND	F10	GND	B6	GND
F1	U ₃	L6	CA ₂	F11	X ₉	A6	V _{DD}
G2	U ₄	K7	CA ₃	E10	X ₁₀	B5	NOOP
G1	U ₅	L7	CA ₄	E11	X ₁₁	A5	LDR
H2	U ₆	K8	CA ₅	D10	P ₁₁	B4	B ₀
H1	U ₇	L8	CA ₆	D11	P ₁₀	A4	B ₁
J2	U ₈	K9	CA ₇	C10	P ₉	B3	B ₂
J1	U ₉	L9	X ₀	C11	P ₈	A3	B ₃
K1	GND	L10	GND	B11	P ₇	A2	WEN

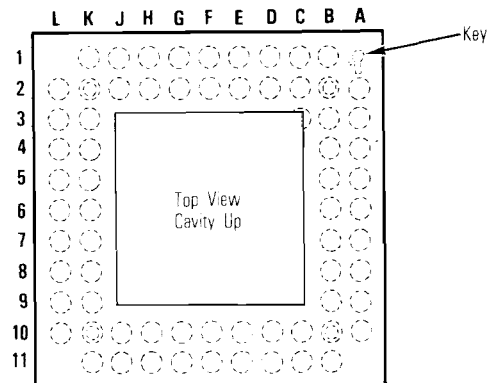
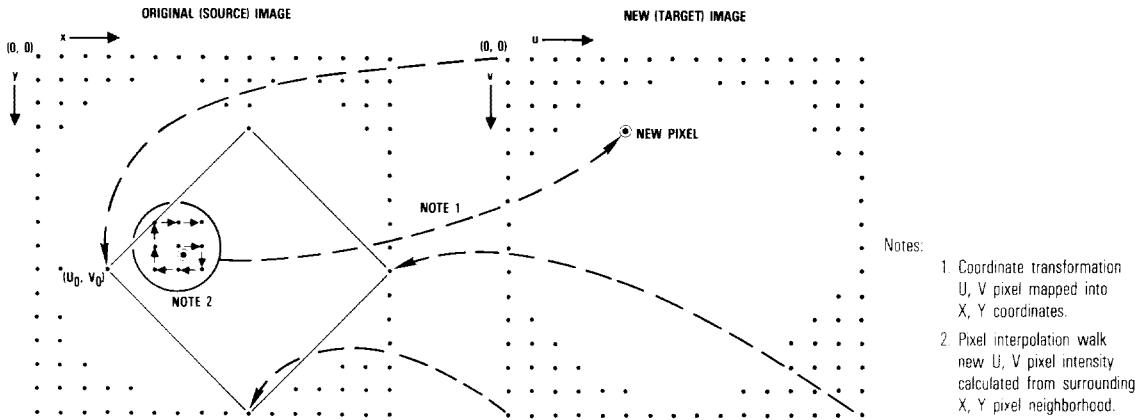


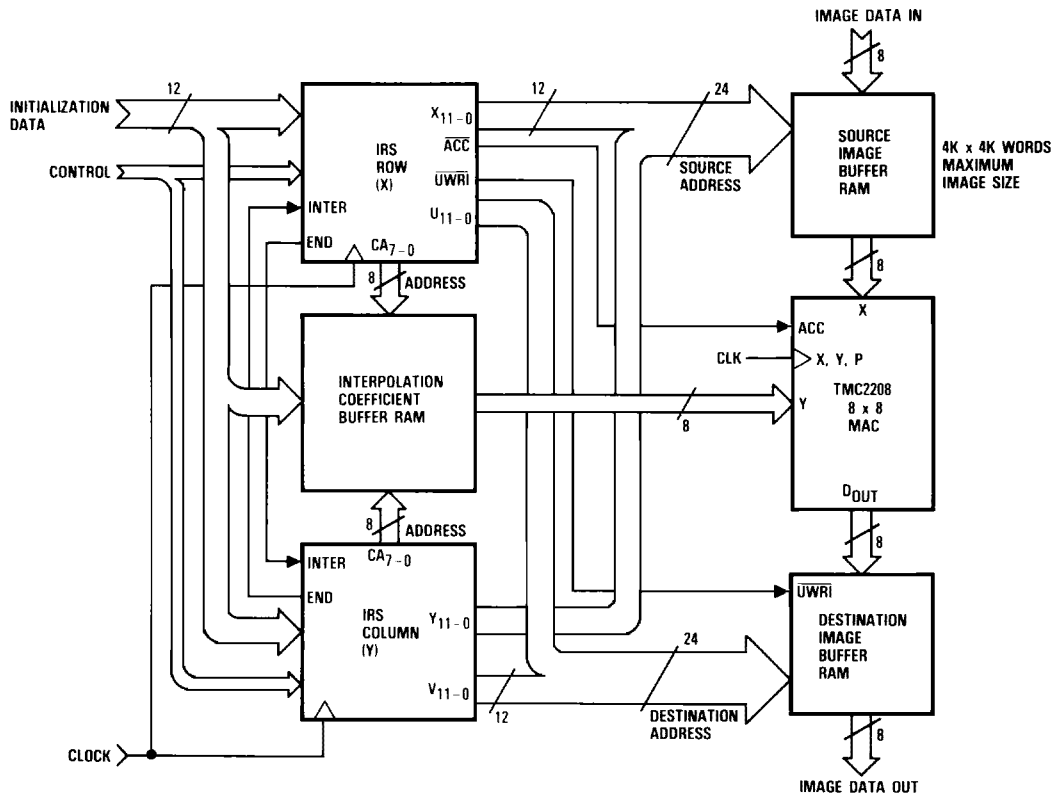
Figure 1. Image Resampling Geometry Showing Image Rotation and Expansion



A basic TMC2301-based system is shown in Figure 2. In this typical system, two Image Resampling Sequencers process the image. The only other external parts needed are a

multiplier-accumulator, external interpolation coefficient lookup table RAM, and the user-specified Source and Destination Image Memory.

Figure 2. Basic 2-D Image Convolver Using TMC2301 Image Resampling Sequencer Utilizing Typical 8-Bit Data Path



Signal Definitions

Power

V_{DD} , GND The TMC2301 operates from a single +5V supply. All pins must be connected.

Clock

CLK The TMC2301 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

P_{11-0} The coordinate transformation parameters are loaded through the registered 12-bit P input port. P_{11} is the Most Significant Bit.

B_3-0 The write addresses for the individual coordinate transform parameters are presented at the registered 4-bit B input port. B_3 is the Most Significant Bit.

Outputs

X_{11-0} The current X (or Y) source pixel address of the image being resampled is indicated by the registered 12-bit X_{11-0} output bus. This output is forced to the high impedance state when \overline{NOOP} is LOW. X_{11} is the Most Significant Bit.

CA_7-0 The current interpolation kernel coefficient lookup table address is indicated by the registered 8-bit CA_7-0 output bus. This output is forced to the high impedance state when \overline{NOOP} is LOW. CA_7 is the Most Significant Bit.

U_{11-0} The U (or V) target address of the image being generated is indicated by the registered 12-bit U_{11-0} output bus. This output is forced to the high impedance state when \overline{OETA} is HIGH. U_{11} is the Most Significant Bit.

Controls

INIT The control logic is cleared and initialized for the start of a new image transformation when the registered INIT input is HIGH for a minimum of two clock cycles. Normal operation begins after INIT goes LOW.

\overline{WEN}

The registered Write Enable input allows the transformation parameters to be written into the preload register indicated by the address at the B input port when LOW. See Figure 4.

LDR

The data held in all transformation parameter preload registers is latched into the storage registers when the registered input LDR is HIGH. When LDR is LOW, the parameters remain unchanged. See Figure 4.

\overline{ACC}

The accumulation register of the external multiplier-accumulator is initialized by the registered \overline{ACC} output. \overline{ACC} goes LOW for one cycle at the start of each interpolation "walk," effectively clearing the storage register by loading in only the new first product. See Figure 9.

\overline{UWRI}

After the end of each interpolation "walk," the Target Memory (U or V) Write Enable goes LOW for one clock cycle. See Figure 9. This registered output is forced to the high impedance state when \overline{OETA} is HIGH.

INTER

In the common two-device system configuration, the Interconnect inputs are connected to the END flag outputs. The END flag from the row (X) sequencer thus indicates an "end of line" to the column (Y) device, while the column sequencer in turn sends a "bottom of frame" signal to the row device, forcing a reset of the address counter.

\overline{NOOP}

The Clock is overridden when the registered input \overline{NOOP} is LOW, holding all address generators in their current state. Also, the output buffers for the address busses X_{11-0} and CA_7-0 are forced to the high impedance state. This allows the user access to all external memory. When \overline{NOOP} goes HIGH, normal operation resumes on the next clock cycle.

\overline{OETA}

The target memory outputs \overline{UWRI} and address bus U_{11-0} are in the high-impedance state when the registered Output Enable input is HIGH. When \overline{OETA} is LOW, they are enabled on the next clock cycle.



Flags

CZERO

The registered CZERO flag of a horizontal dimension TMC2301 goes HIGH if $X < 0$, $X_{MIN} \leq X \leq X_{MAX}$, or $X \geq 4096$ (1000 hex). It goes LOW if $0 \leq X < X_{MIN}$ or $X_{MAX} < X < 4096$. The logical AND of the CZERO flags of a two-dimensional pair of TMC2301s will go LOW when the source address falls outside a rectangle with vertices (XMIN, YMIN), (XMAX, YMIN), (XMIN, YMAX), and (XMAX, YMAX), denoting an invalid address. The external data path can be wired to substitute a selected background value whenever this AND = 0.

END

The registered END flag goes HIGH during the last pixel of the last walk in a row in the case of the row chip, and the last pixel of the last walk in a column in the column chip, in the two-device architecture. This output is used as the end-of-line and end-of-frame indicator in conjunction with the INTER inputs of both TMC2301s.

DONE

In the standard two-device system, a row sequencer DONE flag HIGH after the last walk at the end of the last row of an image (during UWRI LOW) indicates the end of the transform. This registered output is usually ignored on the column device. See the Transformation Control Parameters, AUTOINIT.

Package Interconnections

Signal Type	Signal Name	Function	G8, H8 Package Pins	L1, R1 Package Pins
Power	V _{DD}	Supply Voltage	L5, A6	36, 68
	GND	Ground	F2, K1, K6, L10, F10, B6	1, 9, 18, 35, 52, 60
Clock	CLK	System Clock	A7	34
Inputs	P ₁₁₋₀	Parameter Register Data	D10, D11, C10, C11, B11, B10, A10, B9, A9, B8, A8, B7	22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33
	B ₃₋₀	Parameter Register Address	A3, B3, A4, B4	42, 41, 40, 39
Outputs	X ₁₁₋₀	Source Address	E11, E10, F11, G11, G10, H11, H10, J11, J10, K11, K10, L9	21, 20, 19, 17, 16, 15, 14, 13, 12, 11, 10, 8
	CA ₇₋₀	Coefficient Address	K9, L8, K8, L7, K7, L6, K5, L4	7, 6, 5, 4, 3, 2, 67, 66
	U ₁₁₋₀	Target Address	L2, K2, J1, J2, H1, H2, G1, G2, F1, E1, E2, D1	62, 61, 59, 58, 57, 56, 55, 54, 53, 51, 50, 49
Controls	INIT	Initialize	B2	44
	NOOP	No Operation	B5	37
	WEN	Parameter Write Enable	A2	43
	LDR	Lead Parameter Data Registers	A5	38
	ACC	Accumulate	L3	64
	OETA	Target Memory Output Enable	B1	45
	UWRI	Target Memory Write Enable	K3	63
	INTER	Interconnect	C2	46
Flags	CZERO	Coefficient Zero	K4	65
	END	End of Row/Page	C1	47
	DONE	End of Transform	D2	48

Transformation Control Parameters

The TMC2301 is a self-sequencing device which requires no cycle-to-cycle intervention from the host system. To program the device, the user loads the 16 operating parameters, which define the transformation to be performed, which sections of the original and resampled image spaces are to be utilized, and various control words. Filtering operations are further defined by the values the user loads into the external coefficient memory. The transform parameters are described below. See also Tables 1 through 3.

XMIN, XMAX, YMIN, YMAX These four parameters outline the “source” rectangular region of the original image. Whenever the IRS pair generates an (X, Y) address within this boundary the $\overline{\text{CZERO}}$ flags will denote a valid memory read. In the most common case, $\text{XMIN} < \text{XMAX}$, $\text{YMIN} < \text{YMAX}$, $000\text{h} < \text{X} < \text{FFFh}$, and $000\text{h} < \text{Y} < \text{FFFh}$. In this case, addresses out-of-bounds cause one or both $\overline{\text{CZERO}}$ s to go LOW. Refer to Application Note TP-38 for further information on other boundary violation cases. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.

UMIN, UMAX, VMIN, VMAX These four parameters outline the “target” region of the (u, v) plane, into which the resampled image will be written. The IRS will generate, line by line, a scan that fills only this portion of the plane, permitting the user to assemble a mosaic of multiple rectangular subimages. Care must be taken to ensure that $\text{UMAX} > \text{UMIN}$ and $\text{VMAX} > \text{VMIN}$. Each parameter is expressed in 12-bit unsigned binary integer notation. See Figure 12.

(X₀, Y₀) These are the coordinates of the first pixel to be read from the original image. In many applications, this point will be one of the four corners of the original image to be resampled. The pixels near (X₀, Y₀) in the original image will be used to compute the upper left pixel of the transformed image. In non-inverting, non-reversing applications (X₀, Y₀) will be the upper left corner of the original subimage. Each coordinate is expressed in 13-bit integer plus 5-bit fraction, two's complement notation.

dX/dU₀ Is the initial horizontal partial first derivative indicating the displacement along the X axis which corresponds to each one-pixel movement along the U axis. Usually, $0 < \text{dX/dU}_0 < 1$ corresponds to magnification, whereas $\text{dX/dU}_0 > 1$ represents reduction and $\text{dX/dU}_0 < 0$ denotes reflection about a vertical axis. The first derivatives are expressed in 8-bit integer, 12-bit fraction two's complement notation.

dX/dV₀ Is the initial horizontal-vertical partial first derivative. It indicates the displacement along the X axis corresponding to each one-pixel movement along the V axis. The coefficients dX/dV₀ and dY/dU₀ define image rotation and shear.

dY/dU₀ Is the initial vertical-horizontal partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel movement along the U axis.

dY/dV₀ Is the initial vertical partial first derivative. It indicates the displacement along the Y axis corresponding to each one-pixel step along the V axis. Since dX/dU₀ and dY/dV₀ are separate parameters, vertical magnification and reflection need not match their horizontal counterparts.

NOTE: For each incremental move along the U axis, the starting point of the new “walk around spiral” is indexed to the ENDING point of the previous walk around spiral, rather than to its center. Therefore, the terms dX/dU₀ and dY/dU₀ must be adjusted accordingly. Since each new line is referenced back to the previous line's initial spiral starting point, no similar dX/dV₀ or dY/dV₀ correction is needed.

d²X/dU² Is the second order horizontal derivative. It indicates the rate of change of the horizontal-horizontal first derivative with each step along a line in the output image space. All six second-order derivatives are 4-bit integer, 20-bit fractional two's complement parameters.



d^2X/dV^2 Is the second order horizontal-vertical-vertical derivative. It indicates the rate of change of the horizontal-vertical first derivative with each step down a column in the output image space.

d^2Y/dU^2 Is the second order vertical-horizontal-horizontal derivative. It indicates the rate of change of the the vertical-horizontal first derivative with each step along a line of the output image space.

d^2Y/dV^2 Is the second order vertical derivative. It indicates the rate of change of the vertical-vertical first derivative with each step down a column of the output image space.

$d^2X/dUdV$ Is the mixed second order derivative indicating the rate of change of the first order horizontal derivative as one proceeds downwards through the output image space. This is also the rate of change of the first order horizontal-vertical derivative during horizontal sweeps in the output image space.

$d^2Y/dUdV$ Is the mixed second order derivative indicating the rate of change of the first order vertical derivative as one moves horizontally across the output space, or, equivalently, the rate of change of the first order vertical-horizontal derivative as one moves vertically in the output image space.

Row/Column Select Sets the mode to either Row (0) or Column (1) operation.

Mode This 2-bit control word defines three unique instructions:

Code	Instruction
00, 01	single-pass operation
10	pass 1 of two-pass operation
11	pass 2 of two-pass operation

In single-pass operation, the device walks through the entire $(k + 1) \times (k + 1)$ kernel for each output pixel, where k is the value written into the Kernel section (see below) of the parameter register. Two-pass operation, which requires a dimensionally separable kernel, is executed first for a $(k + 1)$

element kernel in one direction, then for a $(k + 1)$ element kernel in the other direction. For kernel sizes exceeding 2×2 , the two-pass algorithm is obviously beneficial, requiring $2n$ samples per output point instead of $n \times n$. In this case, the intermediate image data stored in the destination image memory following the first pass is used as the source image data on the second pass. The user may design his system to switch source and destination memory bank addresses in place, or could utilize a second TMC2301 pair in a pipelined architecture. This would require a third image buffer for the final destination image. Both devices of a system pair are usually set to the same mode.

Kernel The effective kernel width (height) exceeds this 4-bit unsigned number by 1, thereby providing kernels of 1×1 to 16×16 source pixels per output, for either resampling or filtering. Simple static filters can be implemented with kernels of up to 16×16 pixels (Kernel = 15), while resampling interpolation kernels are limited to 4×4 pixels (Kernel = 3), due to the four bits of fractional X (or Y) address generated by the TMC2301. See the Applications Discussion, below. Again, both devices in a pair are generally initialized with equal Kernel values.

Field of View (FOV) As the device walks through its kernel coefficients, each corresponding step in (x, y) space is normally one pixel length or height; this is a field of view of 1. However, the user can subsample the original space before filtering or resampling, by applying the coefficient kernel over a view field of up to 7 units. At a field of view of F , the pixels selected for each kernel operation are F pixels apart. This is useful in oversampled pictures, whose intensity changes only slowly from pixel to pixel.

Autoload (ALR) When set to 1 (HIGH), the LDR control is automatically asserted when INIT is strobed, loading the coefficient set currently stored in the preload registers.

Autoinit (AIN) At the end of an image, if the AIN bit is 1 (HIGH) the DONE flag goes HIGH for one clock cycle and a new transform begins. If 0 (LOW), \overline{UWR} and the DONE flag remain HIGH during the sequence until the user strobes the INIT control to begin a new image transformation.

Pipe (PIPE) Adjusts the timing of the target memory write controls, to compensate for buffered source image RAM. If the PIPE bit is 1 (HIGH), outputs ACC and UWRI will be delayed one clock cycle relative to the generation of the target address (U or V). See Figure 9.

Test Mode (TM) This mode is available for user inspection of the coefficient data. The source image and coefficient addresses are calculated by an internal 28-bit accumulator. When TM is 1 (HIGH), the sign bit, normally discarded, and the lower 11 bits of internal data are substituted for the upper 12 bits appearing at the source address port (X) during a standard transform cycle. This allows user verification of algorithm mathematics during debug. Since the TM bit is registered and cannot be changed during a single clock cycle, two distinct clock cycles are required to access both the MSW and LSW of the internal accumulator. See Figure 3.

Table 1. Parameter Registers – Row Sequencer

Address	Name	Description
0000	XMIN	Left side of Source Window
0001	XMAX	Right side of Source Window
0010	X ₀ (LSW)	Source starting point – X coordinate
0011	X ₀ (MSW)	Source starting point – X coordinate
0011	Controls	Mode Select Bits
0100	dX/dU ₀ (LSW)	Row/Row first differential
0101	dX/dU ₀ (MSW)	Row/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dX/dV ₀ (LSW)	Row/Column first differential
0111	dX/dV ₀ (MSW)	Row/Column first differential
0111	Kernel	Resampling/Filtering Kernel
1000	d ² X/dUdV (LSW)	Mixed second differential
1001	d ² X/dUdV (MSW)	Mixed second differential
1010	d ² X/dU ² (LSW)	Row second differential
1011	d ² X/dU ² (MSW)	Row second differential
1100	d ² X/dV ² (LSW)	Row/Column second differential
1101	d ² X/dV ² (MSW)	Row/Column second differential
1110	UMIN	Left edge of Final Image
1111	UMAX	Right edge of Final Image



Figure 3. Test Mode Data Routing

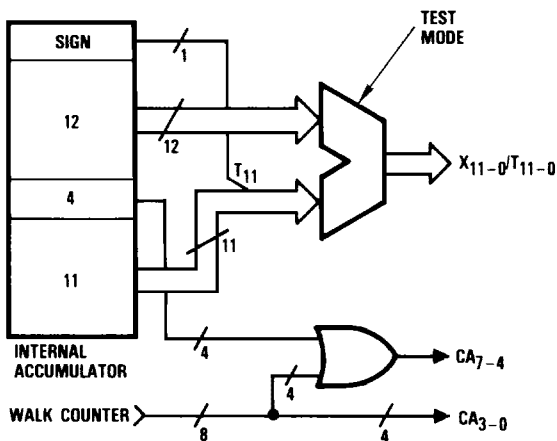


Table 2. Parameter Registers – Column Sequencer

Address	Name	Description
0000	YMIN	Top of Source Window
0001	YMAX	Bottom of Source Window
0010	Y ₀ (LSW)	Source starting point – Y coordinate
0011	Y ₀ (MSW)	Source starting point – Y coordinate
0011	Controls	Mode Select Bits
0100	dY/dU ₀ (LSW)	Column/Row first differential
0101	dY/dU ₀ (MSW)	Column/Row first differential
0101	TM, FOV	Test Mode, Field of View
0110	dY/dV ₀ (LSW)	Column/Column first differential
0111	dY/dV ₀ (MSW)	Column/Column first differential
0111	Kernel	Resampling/Filtering Kernel Size
1000	d ² Y/dUdV (LSW)	Mixed second differential
1001	d ² Y/dUdV (MSW)	Mixed second differential
1010	d ² Y/dU ² (LSW)	Column/Row second differential
1011	d ² Y/dU ² (MSW)	Column/Row second differential
1100	d ² Y/dV ² (LSW)	Column second differential
1101	d ² Y/dV ² (MSW)	Column second differential
1110	VMIN	Top edge of Final Image
1111	VMAX	Bottom edge of Final Image

Table 3. Parameter Registers Binary Format (Row Or Column Sequencer)

Addr	Format												Limits	
	MSB											LSB	Dec	Hex
0000*	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	4095 0	FFF 000
0001*	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	4095 0	FFF 000
0010	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	4096-2 ⁻⁵ -4096	0FFF.F8 F000.00
0011							2 ⁻¹²	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷		
0011 (Control)	ALR	AIN	PIPE	R/C	M ₁	M ₀								
0100	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	128-2 ⁻¹² -128	007F.FFF FF80.000
0101					2 ⁻⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰		
0101* (TM, FOV)	TM	2 ²	2 ¹	2 ⁰										
0110	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	128-2 ⁻¹² -128	007F.FFF FF80.000
0111					2 ⁻⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰		
0111* (Kernel)	2 ³	2 ²	2 ¹	2 ⁰										
1000	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	8-2 ⁻²⁰ -8	0007.FFFFF FFF8.00000
1001	2 ⁻³	2 ²	2 ¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸		
1010	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	8-2 ⁻²⁰ -8	0007.FFFFF FFF8.00000
1011	2 ⁻³	2 ²	2 ¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸		
1100	2 ⁻⁹	2 ⁻¹⁰	2 ⁻¹¹	2 ⁻¹²	2 ⁻¹³	2 ⁻¹⁴	2 ⁻¹⁵	2 ⁻¹⁶	2 ⁻¹⁷	2 ⁻¹⁸	2 ⁻¹⁹	2 ⁻²⁰	8-2 ⁻²⁰ -8	0007.FFFFF FFF8.00000
1101	2 ⁻³	2 ²	2 ¹	2 ⁰	2 ⁻¹	2 ⁻²	2 ⁻³	2 ⁻⁴	2 ⁻⁵	2 ⁻⁶	2 ⁻⁷	2 ⁻⁸		
1110*	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	4095 0	FFF 000
1111*	2 ¹¹	2 ¹⁰	2 ⁹	2 ⁸	2 ⁷	2 ⁶	2 ⁵	2 ⁴	2 ³	2 ²	2 ¹	2 ⁰	4095 0	FFF 000

* unsigned binary notation
A "-" indicates MSB is sign bit

Operation of the Transformation Parameter Registers

Numerous applications require the ability to update the coordinate transformation parameters "on the fly." Because the parameters are double-buffered, the user can load any or all of them into the preload registers without upsetting the operation in progress. Then LDR (load data registers) will update all transform parameters to the new values simultaneously. This feature is particularly valuable for "pin cushion" and "fish eye" transformations, or polar-to-rectangular conversions, which cannot be performed with constant second derivatives. The Autoload function updates the preload registers at the beginning of a new image automatically. See the Transformation Control Parameters section. Note also that data can be loaded in to the registers while $\overline{\text{NOOP}}$ is active (LOW).

Figure 4. Operation of LDR Control for Parameter Update

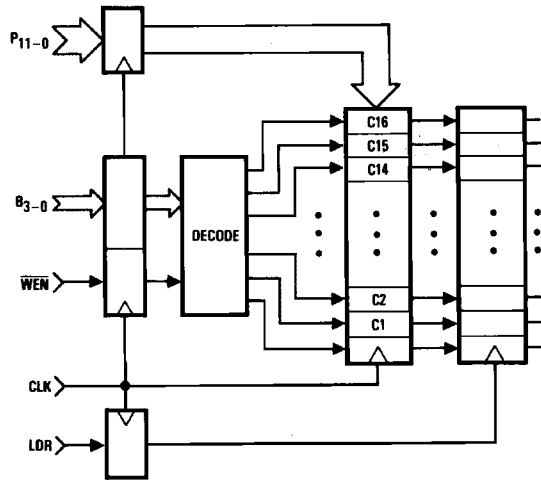
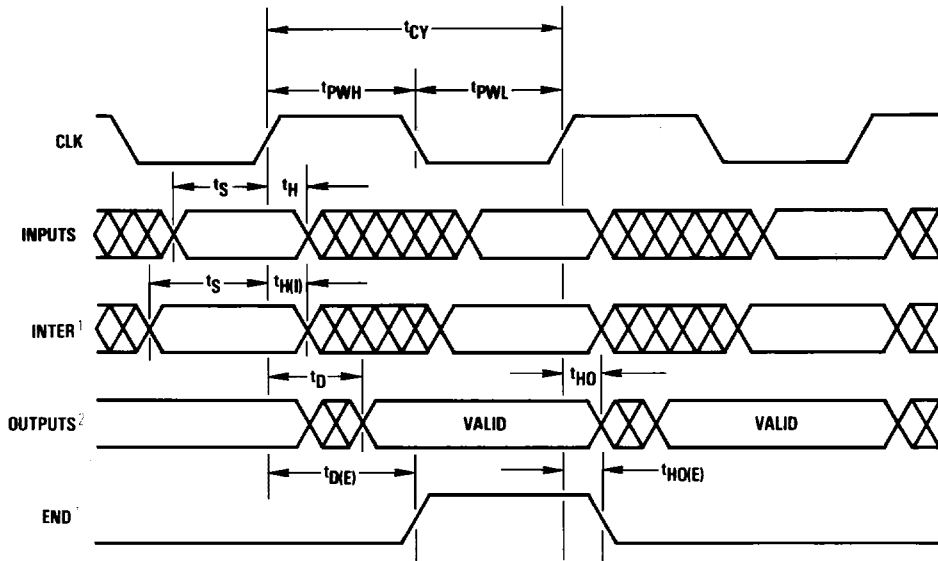


Figure 5. Timing Diagram



Notes:

1. t_S and t_{DE} are guaranteed to allow full speed operation in the standard two-device architecture. See text.

2. All outputs except END. See text.

Figure 6. Equivalent Input Circuit

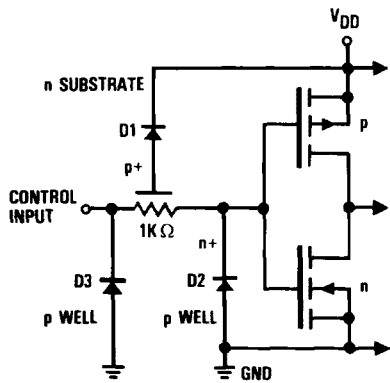


Figure 7. Equivalent Output Circuit

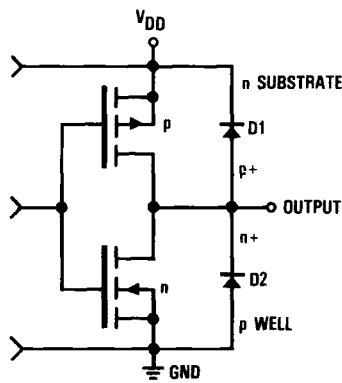
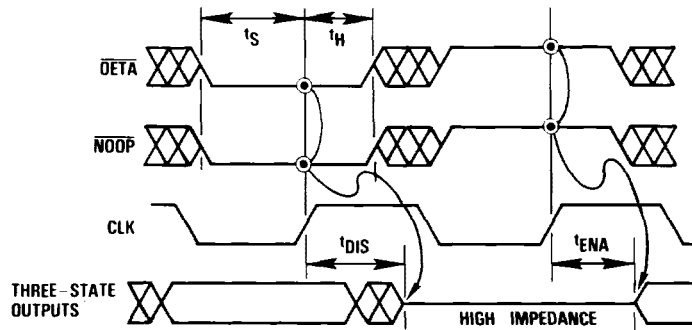


Figure 8. Transition Level for Three-State Measurement



Note:
1. All outputs except \overline{CZERO} , \overline{ACC} , \overline{END} and \overline{DONE} .

Absolute maximum ratings (beyond which the device may be damaged)¹

Supply Voltage	-0.5 to +7.0V
Input Voltage	-0.5 to (V _{DD} +0.5)V
Output	
Applied voltage ²	-0.5 to (V _{DD} +0.5)V
Forced current ^{3,4}	-1.0 to +6.0mA
Short-circuit duration (single output in HIGH state to ground)	1 sec
Temperature	
Operating, case	-60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	-65 to +150°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Temperature Range						Units
		Standard			Extended			
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH			-4.0			-4.0	mA
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				-55		125	°C

DC characteristics within specified operating conditions¹

Parameter	Test Conditions	Temperature Range				Units		
		Standard		Extended				
		Min	Max	Min	Max			
I_{DDQ}	Supply Current, Quiescent	$V_{DD} = \text{Max}, V_{IN} = 0V$			5	5	mA	
I_{DDU}	Supply Current, Unloaded	$V_{DD} = \text{Max}, f = 15\text{MHz}$			75	75	mA	
I_{IL}	Input Current, Logic LOW	$V_{DD} = \text{Max}, V_{IN} = 0V$		-10	+10	-75	+75	μA
I_{IH}	Input Current, Logic HIGH	$V_{DD} = \text{Min}, V_{IN} = V_{DD}$		-10	+10	-75	+75	μA
V_{OL}	Output Voltage, Logic LOW	$V_{DD} = \text{Min}, I_{OL} = \text{Max}$			0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	$V_{DD} = \text{Min}, I_{OH} = \text{Max}$		2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	$V_{DD} = \text{Min}, V_{IN} = 0V$		-40	+40	-40	+40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	$V_{DD} = \text{Min}, V_{IN} = V_{DD}$		-40	+40	-40	+40	μA
I_{OS}	Short-Circuit Output Current ²	$V_{DD} = \text{Max}, \text{Output HIGH, one pin to ground, one second duration max.}$			-100		-100	mA
C_I	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1\text{MHz}$			10		10	pF
C_O	Output Capacitance	$T_A = 25^\circ\text{C}, f = 1\text{MHz}$			10		10	pF

Notes:

- Actual test conditions may vary from those shown, but guarantee operation as specified.
- Guaranteed but not tested.

AC characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range						Units
		Standard		Extended				
		-1		Min	Max	Min	Max	
t_{CY} Cycle Time	$V_{DD} - \text{Min}$	55		66		66		ns
t_{PWL} Clock Pulse Width LOW	$V_{DD} - \text{Min}$	25		30		30		ns
t_{PWH} Clock Pulse Width HIGH	$V_{DD} - \text{Min}$	25		30		30		ns
t_S Input Setup Time ¹		18		20		20		ns
t_H Input Hold Time		2		2		2		ns
$t_{H(I)}$ Input Hold Time, INTER		10		10		10		ns
t_D Output Delay ²	$V_{DD} - \text{Min}, C_{LOAD} = 40\text{pF}$		27		35		35	ns
$t_{D(E)}$ Output Delay, END ¹	$V_{DD} - \text{Min}, C_{LOAD} = 10\text{pF}$		37		45		45	ns
t_{HO} Output Hold Time ²	$V_{DD} - \text{Max}, C_{LOAD} = 40\text{pF}$	5		5		5		ns
$t_{HO(E)}$ Output Hold Time, END	$V_{DD} - \text{Max}, C_{LOAD} = 10\text{pF}$	10		10		10		ns
t_{DIS} Three-State Disable Delay	$V_{DD} - \text{Min}, C_{LOAD} = 40\text{pF}$		18		20		20	ns
t_{ENA} Three-State Enable Delay	$V_{DD} - \text{Min}, C_{LOAD} = 40\text{pF}$	27		35		35		ns

Notes:

1. $t_S + t_{D(E)} = t_{CY}$ max.
2. Excluding output pin END.

Applications Discussion

Basic Operation

Each TMC2301 pair contains address controllers which execute patterns much like the following FORTRAN 3-level nested DO loop:

1. The inner loop is a clockwise outgoing spiral "walk" through the N-element coefficient kernel.
2. The middle loop is a left-to-right "scan" along each row of the output image space.
3. Finally, the outer loop is a top-to-bottom "scan" down each column of the output image space.

A typical one-pass image transformation proceeds as follows:

1. The device pair outputs the addresses (X₀, Y₀), which is the first point in the source image, and (CAX, CAY), the interpolation lookup table address for the first pixel in the kernel. The output \overline{ACC} goes LOW, causing the external accumulator to load the first product without summation,

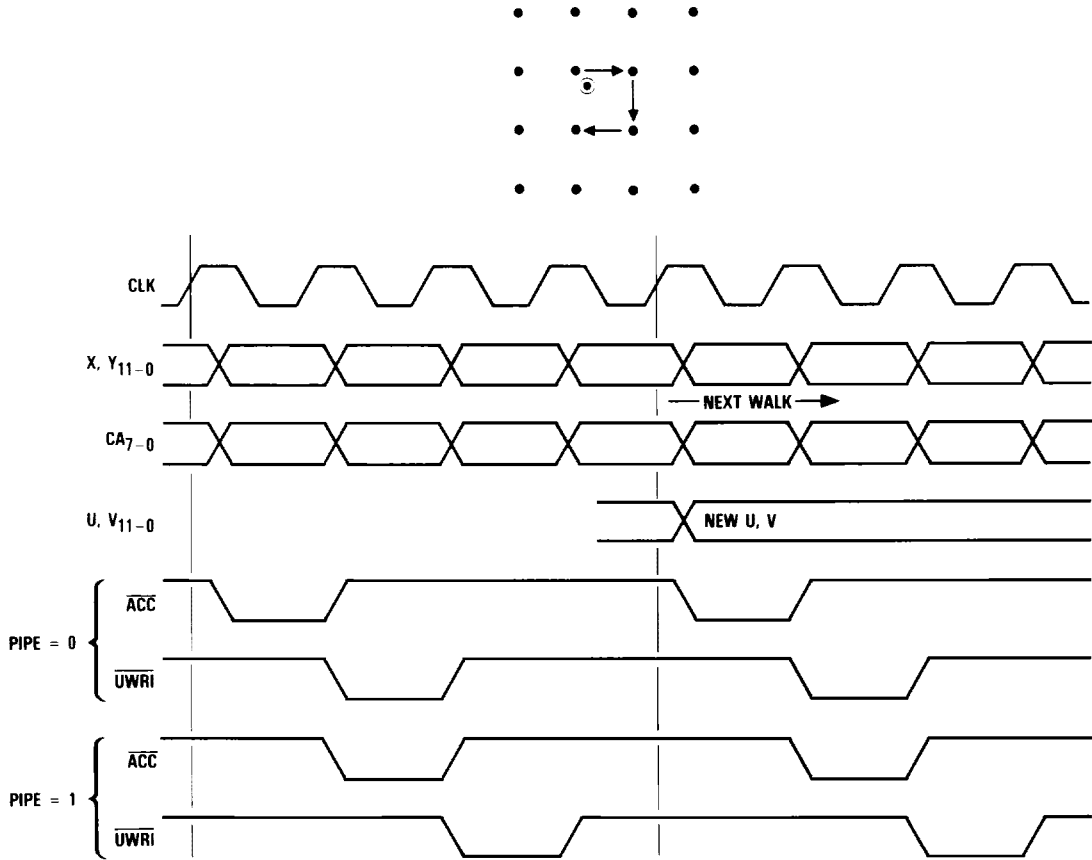
clearing the accumulator.

2. For the next N cycles, the IRS walks through an outward clockwise spiral in (x, y) space, accumulating pixel-interpolation coefficient products. The spiral sequence is depicted in Figure 9.
3. After the completion of the first spiral walk, the IRS outputs the target address of the first pixel, (UMIN, VMIN) and the control \overline{UWRI} , along with the initial (X, Y) values of the next spiral walk. \overline{ACC} and \overline{UWRI} can be delayed by one clock cycle by setting the control bit PIPE to 1 (HIGH), simplifying the task of interfacing the TMC2301 to buffered source image memory.
4. After the last cycle of the next spiral, \overline{UWRI} again goes LOW for one clock, and the target address outputs are updated, pointing to the location of the pixel calculation just completed, (UMIN + 1, VMIN).

5. The third spiral walk begins with \overline{ACC} going LOW, and ends with $(UMIN + 2, VMIN)$ output and \overline{UWRI} going LOW.
6. The procedure continues until $(UMAX + 1, VMIN)$ is reached, at which point the device resets to U (position within row) and increments V (number of row). Thus, the next (U, V) set

- after $(UMAX + 1, VMIN)$ will be $(UMIN, VMIN + 1)$, followed by $(UMIN + 1, VMIN + 1)$, etc.
7. Upon completion of the walk corresponding to $(UMAX + 1, VMAX + 1)$, the TMC2301 will generate a DONE flag with the final $UWRI$, and begin a new sequence.

Figure 9. Timing Diagram and Pixel Map Showing Outward Clockwise Spiral Walk Generated by TMC2301 (2 x 2 Kernel Shown)



E

- Notes:
1. Assumes that \overline{OETA} is LOW and \overline{NDOP} is HIGH.
 2. Timing Parameters are not shown on this diagram.

On any given clock cycle, the actual (X, Y) and (U, V) outputs of the IRS are given by the following equations:

$$\begin{aligned}
 x &= X_0 + dX/dU_0 * m + dX/dV_0 * n + d^2X/dUdV * m * n \\
 &\quad + d^2X/dU^2 * (m^2 - m)/2 + d^2X/dV^2 * (n^2 - n)/2^0 \\
 &\quad + FOV * CAX(w) + FOV * m * CAX(Ker) \\
 y &= Y_0 + dY/dU_0 * m + dY/dV_0 * n + d^2Y/dUdV * m * n \\
 &\quad + d^2Y/dU^2 * (m^2 - m)/2 + d^2Y/dV^2 * (n^2 - n)/2^0 \\
 &\quad + FOV * CAY(w) + FOV * m * CAY(Ker) \\
 u &= UMIN + m \\
 v &= VMIN + n
 \end{aligned}$$

where FOV is the 4-bit field of view parameter, normally set to 1 so that the spiral walk proceeds in single-pixel steps. Setting FOV to 4 would expand the spiral walk, allowing the user to trade two bits of image size for two bits of additional interpixel positioning resolution. CAX(w) and CAY(w) are the current value of the coefficient address outputs, and CAX(KER) and CAY(KER) are the terminal values of each pixel walk. The CA(KER) terms arise because the IRS computes each new walk's starting point from the previous spiral walk's end point, rather than its starting point.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, all 8 bits of coefficient address are available to access up to 256 interpolation coefficients, for kernels of 16 x 16 pixels. This address is generated by the internal walk counter of the TMC2301. In most applications, the same Kernel parameter value is selected in both IRS devices; thus, the Coefficient Address outputs CA7_0 for the X and Y devices are identical, and the user needs only one of the 8-bit buses for memory access.

Applications executing a coordinate transformation, however, will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and fractional address components are generated. The user then must account for this spatial offset in both dimensions by storing the appropriate corrected interpolation kernel values in the lookup table. The 8-bit address bus is broken up into two parts: the fractional portion (upper 4 bits), and the walk counter (lower 4 bits). Thus, in

resampling applications, the maximum kernel size is 4 x 4 pixels, or 16 locations. As in the filtering example, assuming that the user has selected the same kernel size for both IRS devices, the 4 bits of least-significant address generated by both devices will be identical, and redundant. The four most significant address bits, however, will reflect the current fractional offsets of the resampled pixel from the nearest X (Y) location, to a spatial resolution of 4 bits, in the X (or Y) directions. Utilization of the 12 bits (total) of lookup table address is left to the user, to be arranged as desired for memory access. See Figure 3.

Application Examples

One of the more common applications for the TMC2301 is simple static filtering. In this case the source and target memories locations are identical and no coordinate transformation is performed. The (X, Y) and (U, V) outputs listed in Table 4 show the address sequencing generated by the TMC2301 to execute the walk of a 5 x 5 pixel interpolation kernel. The normalized coefficients shown implement a first-order Butterworth Low Pass Filter with cutoff radius of 1/√2. Note that the (U, V) output address is updated following the completion of the walk for that location.

Figure 10. Pixel Map Showing Walk Sequence for 5 x 5 Static Filter

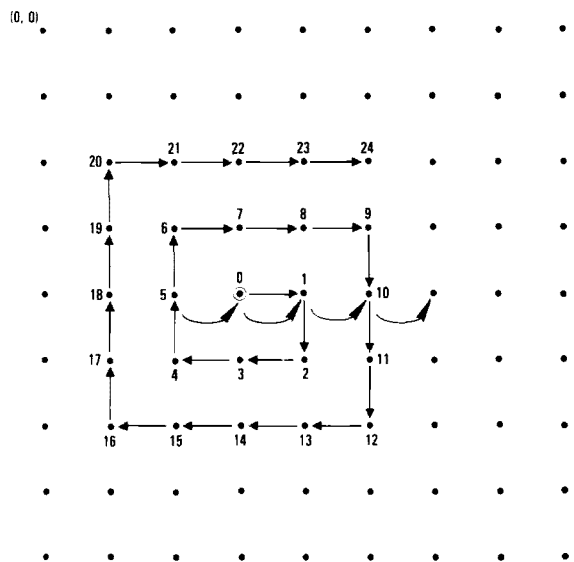


Table 4. IRS Outputs for Static Filter Illustrated in Figure 10

Cycle	X	Y	Index (CA)	Coefficient	U	V
1	3	4	0	0.2176	2	4
2	4	4	1	0.0725	2	4
3	4	5	2	0.0435	2	4
4	3	5	3	0.0725	2	4
5	2	5	4	0.0435	2	4
6	2	4	5	0.0725	2	4
7	2	3	6	0.0435	2	4
8	3	3	7	0.0725	2	4
9	4	3	8	0.0435	2	4
10	5	3	9	0.0198	2	4
11	5	4	10	0.0272	2	4
12	5	5	11	0.0198	2	4
13	5	6	12	0.0128	2	4
14	4	6	13	0.0198	2	4
15	3	6	14	0.0272	2	4
16	2	6	15	0.0198	2	4
17	1	6	16	0.0128	2	4
18	1	5	17	0.0198	2	4
19	1	4	18	0.0272	2	4
20	1	3	19	0.0198	2	4
21	1	2	20	0.0128	2	4
22	2	2	21	0.0198	2	4
23	3	2	22	0.0272	2	4
24	4	2	23	0.0198	2	4
25	5	2	24	0.0128	2	4
26	4	4	0	0.2175	3	4

However, we have included a linear compression factor of 5:1, and must accommodate the fact that each time u is incremented, the start of the new walk is referenced to the END of the previous walk. Given these corrections, the rotation matrix becomes:

$$\begin{aligned}
 dX/dU_0 &= 5\cos(a) = 3 & dY/dU_0 &= 5\sin(a) - FOV = 3 \\
 dX/dV_0 &= -5\sin(a) = -4 & dY/dV_0 &= 5\cos(a) = 3 \\
 \text{Kernel} &= 1
 \end{aligned}$$

Figure 11. Pixel Map Showing Parameters for 63° Rotation and 5:1 Compression Listed in Table 5

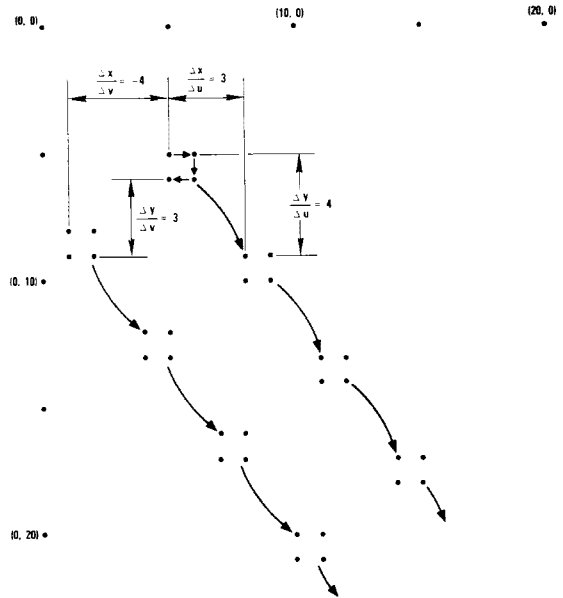


Figure 11 illustrates the sequence for a bilinear resampling of a 63° rotation. The starting point is translated +1 in the Y-direction. A common rotation matrix might be:

$$\begin{aligned}
 dX/dU_0 &= \cos(a) = .6 & dY/dU_0 &= \sin(a) = .8 \\
 dX/dV_0 &= -\sin(a) = -.8 & dY/dV_0 &= \cos(a) = .6
 \end{aligned}$$

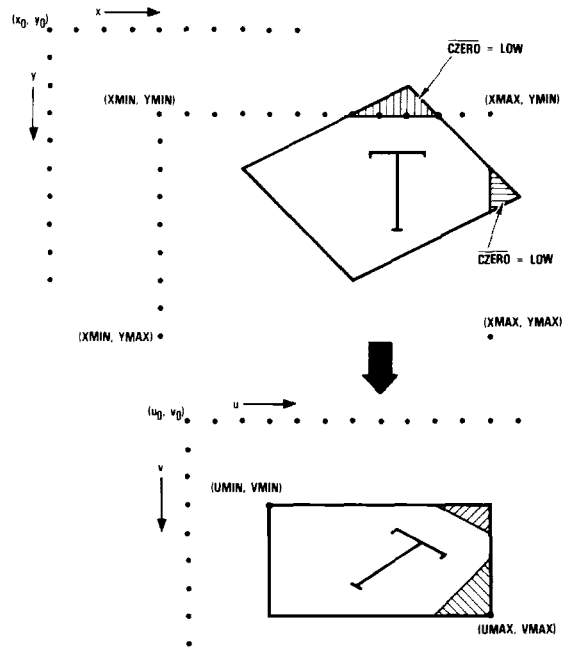
Table 5. IRS Outputs for Operation Illustrated in Figure 11

Cycle	X	Y	Index	U	V
1	5	5	0	4	5
2	6	5	1	4	5
3	6	6	2	4	5
4	5	6	3	4	5
5	8	9	0	5	5
6	9	9	1	5	5
7	9	10	2	5	5
8	8	10	3	5	5
9	11	13	0	6	5
10	12	13	1	6	5
11	12	14	2	6	5
12	11	14	3	6	5
13	14	17	0	7	5
14	15	17	1	7	5
15	15	18	2	7	5
16	14	18	3	7	5
17	1	8	0	8	5
18	2	8	1	8	5
19	2	9	2	8	5
20	1	9	3	8	5
21	4	12	0	5	6
22	5	12	1	5	6
23	5	13	2	5	6
24	4	13	3	5	6
25	7	16	0	6	6
26	8	16	1	6	6
27	8	17	2	6	6
28	7	17	3	6	6
29	10	20	0	7	6
30	11	20	1	7	6
31	11	21	2	7	6
32	10	21	3	7	6
33	0	15	0	8	6

Figure 12 may help clarify the relationships among (X_0, Y_0) , (X_{MIN}, Y_{MIN}) , (X_{MAX}, Y_{MAX}) , (U_{MIN}, V_{MIN}) , and (U_{MAX}, V_{MAX}) . With positive first derivatives, (X_0, Y_0) and (U_{MIN}, V_{MIN}) represent the upper left corners of the original image and the new destination field, respectively. The lower

right corner of the transformed image is located at $(U_{MAX} + 1, V_{MAX} + 1)$; the location of the corresponding corner of the original image depends on the values of the derivatives. Not to be confused with (X_0, Y_0) , the points (X_{MIN}, Y_{MIN}) and (X_{MAX}, Y_{MAX}) define the "usable" rectangular portion of the original image; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. This feature permits one to construct a mosaic of several abutting subimages in the (x, y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper left and lower left corners of the original image lie outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums.

Figure 12. Pixel Maps Demonstrating Source and Destination Image Boundaries and Image Clipping (Note Shaded Area)



Note: Assume $000h < X < FFFh$
 $000h < Y < FFFh$

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2301G8C2	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Pin Grid Array	2301G8C2
TMC2301G8V	EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	MIL-STD-883	68 Pin Grid Array	2301G8V
TMC2301G8V1	EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	MIL-STD-883	68 Pin Grid Array	2301G8V1
TMC2301H8C	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Pin Grid Array	2301H8C
TMC2301H8C1	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Pin Grid Array	2301H8C1
TMC2301L1V	EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	MIL-STD-883	68 Leaded Hermetic Ceramic Chip Carrier	2301L1V
TMC2301L1V1	EXT- $T_C = -55^{\circ}\text{C}$ to 125°C	MIL-STD-883	68 Leaded Hermetic Ceramic Chip Carrier	2301L1V1
TMC2301R1C	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C
TMC2301R1C1	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C1
TMC2301R1C2	STD- $T_A = 0^{\circ}\text{C}$ to 70°C	Commercial	68 Lead Plastic J-Leaded Chip Carrier	2301R1C2

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