DATA SHEET

NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6902C

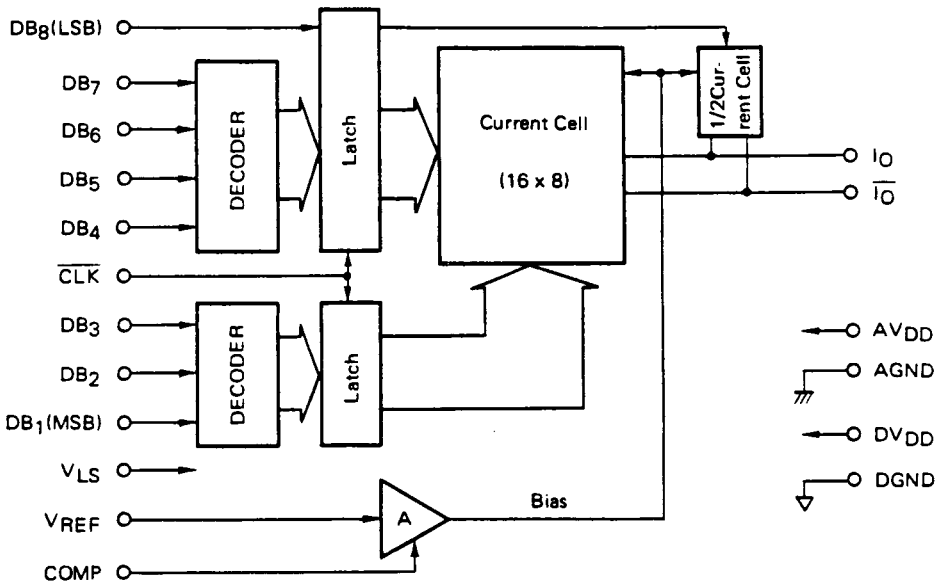
8 bit 50MSPS D/A Converter
CMOS

The μPD6902C is an 8 bit D/A converter for use in video applications. The high-speed CMOS processing technology and the matrix current cell method adopted for this CMOS device have enabled fast conversion rates to be achieved. Conversion rates of up to 50 Msps can be attained while operating at low power consumption, making this device ideal for a wide range of applications including digital TV systems and video systems. ★

FEATURES

- Resolution: 8 bits
- Conversion rate: 50 Msps
- Liniarity: ±1.0 LSB TYP.
- Reference voltage: 2.5 V TYP.
- Power supply voltage: +5 V single
- Low power comsumption (400 mW TYP.)
- TTL/CMOS selectable (Digital data input level.)
- 22 pin plastic DIP

BLOCK DIAGRAM



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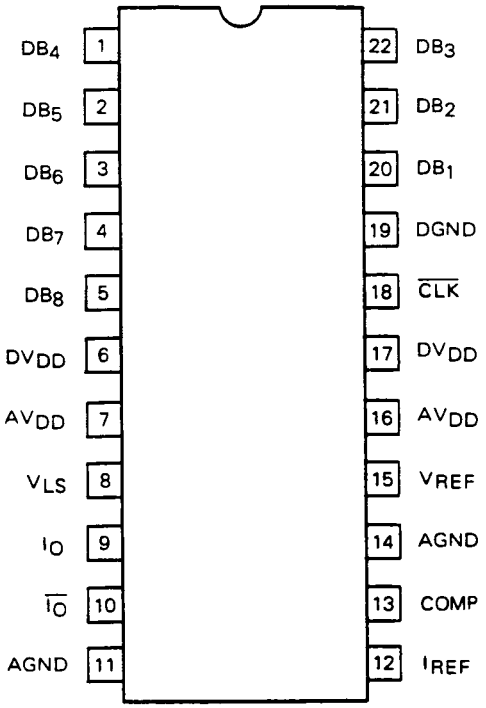
The * mark outside the columns denotes major points where revisions or additions are made in this edition.

★ CONNECTION DIAGRAM (Top View)



1	DB_4	Digital input (4th)
2	DB_5	Digital input (5th)
3	DB_6	Digital input (6th)
4	DB_7	Digital input (7th)
5	DB_8	Digital input (LSB)
6	DV_{DD}	Digital power supply
7	AV_{DD}	Analog power supply
8	V_{LS}	Digital input level select (TTL/CMOS)
9	I_O	Current output
10	$\overline{I_O}$	Complementary current output
11	AGND	Analog GND
12	I_{REF}	Full-scale current adjustment
13	COMP	Amp compensation
14	AGND	Analog GND
15	V_{REF}	Reference voltage input
16	AV_{DD}	Analog power supply
17	DV_{DD}	Digital power supply
18	$\overline{CLK}$	Sampling clock input
19	DGND	Digital GND
20	DB_1	Digital input (MSB)
21	DB_2	Digital input (2nd)
22	DB_3	Digital input (3rd)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C) ★

Power supply voltage	−0.3 to +7.0	V
Input terminal voltage	−0.3 to AV_{DD}+0.3 or DV_{DD}+0.3	V
Output terminal voltage	−0.3 to AV_{DD}+0.3 or DV_{DD}+0.3	V
Analog power supply voltage	DV_{DD}−0.3 to DV_{DD}+0.3	V
Analog GND voltage	DGND−0.3 to DGND+0.3	V
Operating temperature range	−20 to +75	°C
Storage temperature range	−40 to +125	°C

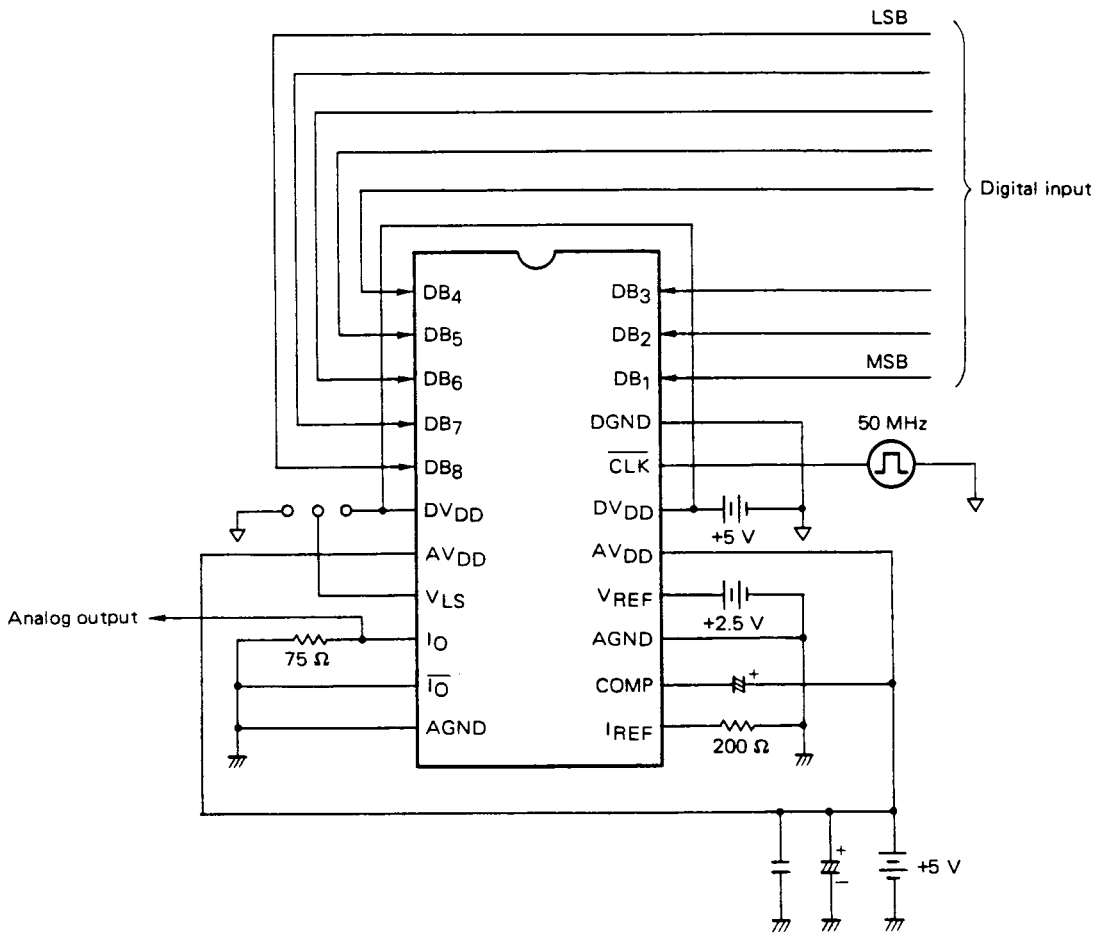
RECOMMENDED OPERATING CONDITIONS (T_a = −20 to +75 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply voltage	AV_{DD}, DV_{DD}	4.75	5.0	5.25	V	
Reference voltage	V_{REF}		2.5		V	
Reference resistance	R_{REF}		200		Ω	
Sampling clock	f_{samp}	0.1		50	MHz	
Sampling clock low level pulse width	t_{PWL}	8			ns	
Sampling clock high level pulse width	t_{PWH}	8			ns	
Data set up time	t_S	8			ns	
Data hold time	t_H	5			ns	
Digital input high level 1	V_{IH1}	2.7			V	VLS=GND
Digital input low level 1	V_{IL1}			0.6	V	VLS=GND
Digital input high level 2	V_{IH2}	0.7V_{DD}			V	V_{LS}=DV_{DD}
Digital input low level 2	V_{IL2}			0.3V_{DD}	V	V_{LS}=DV_{DD}
Compensation capacity	C_{comp}		1.0		μF	

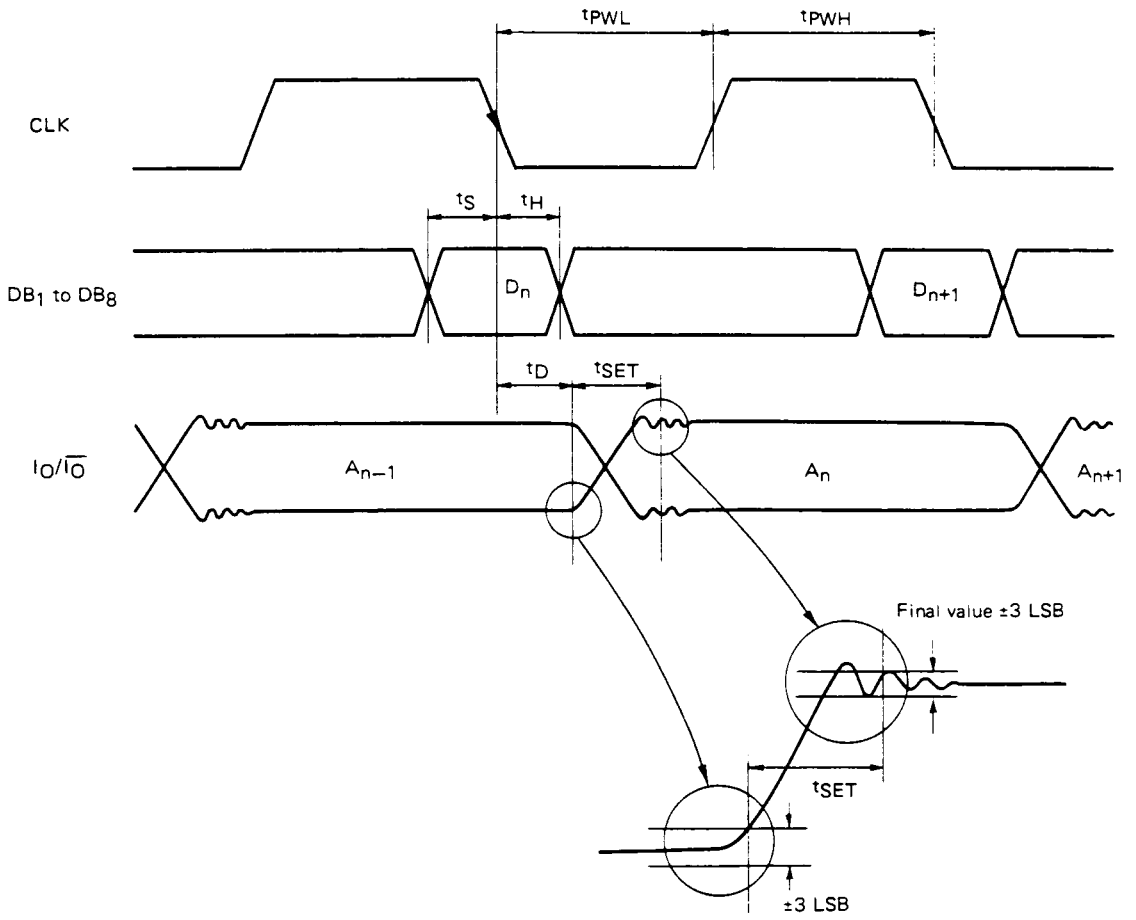
ELECTRICAL CHARACTERISTICS (T_a = −20 to +75 °C, V_{DD} = 5 V ±0.25 V, f_{samp} = 50 MHz)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Power supply current	I_{DD}		100	160	mA	f_{samp}=50 MHz, T_a=25 °C, V_{CC}=5.25 V
Resolution	RES		8		bit	
Non-linearity error	NL		±0.25	±1	LSB	T_a=0 to 60 °C, V_{DD}=5 V
Differential non-linearity	DNL		±0.25	±0.5	LSB	T_a=0 to 60 °C, V_{DD}=5 V
Output compliance	V_O	1.0	1.5		V	V_{DD}=5.0±0.25 V, T_a=0 to 70 °C
Full-scale current	I_{FS}	18	20.4	22	mA	V_{REF}=2.5 V, R_{REF}=200 Ω
Settling time	t_{SET}		32		ns	Final I_O value ≦ ±3 LSB
Analog output delay time	t_D		12		ns	I_O value ≦ ±3 LSB

★ TEST CIRCUIT



TIMING CHART ★



PIN DESCRIPTIONS

DGND (Pin 19) Digital system ground

AGND (Pins 11, 14) Analog system ground

DV_{DD} (Pins 6, 17) Digital system power supply (+5 V)

AV_{DD} (Pins 7, 16) Analog system power supply (+5 V)

The digital system power supply and ground is isolated from the analog system power supply and ground in the IC as a precaution against noise. The ground and power supply lines are also isolated on the circuit boards, the analog ground being as wide as possible for better stability.

Insert by-pass capacitors of about 0.01 μF and 47 μF between the analog power line and analog ground, and also between the digital power line and digital ground. These capacitors should be connected as close as possible to the μPD6902C pins. Supply the digital system power from the analog power line through the low path filter to prevent from luch up.

I_{REF} (Pin 12) Full-scale current adjustment pin

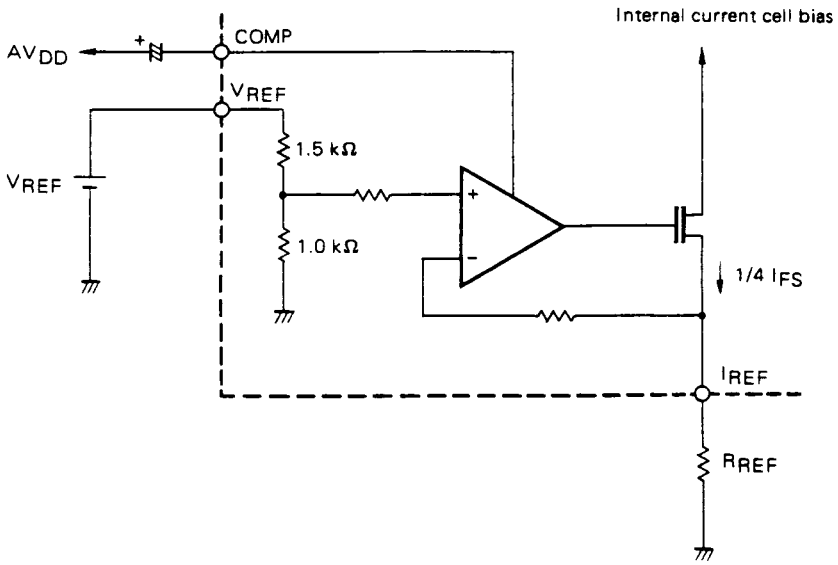
V_{REF} (Pin 15) Reference voltage input pin

These pins are used in adjustment of the analog output current (full-scale current).

The analog output current (full-scale current I_{FS}) is set by the reference voltage V_{REF} and the reference resistance R_{REF} connected between the I_{REF} pin and analog ground.

$$I_{FS} = \frac{4}{2.5} V_{REF} / R_{REF}$$

$$I_{REF} = \frac{1}{2.5} V_{REF} / R_{REF}$$



The recommended reference voltage and reference resistance values are V_{REF} = 2.5 V and R_{REF} = 200 Ω respectively. The output analog current I_{FS} in this case will be 20 mA. Also connect by-pass capacitors of about 0.01 μF and 47 μF between the V_{REF} pin and AGND in the same way as the by-pass capacitors connected to the power pins.

COMP (Pin 13) Phase compensation capacitor connection

A capacitor for phase compensation of the internal amplifier is connected to this pin. Connect a 1.0 μF capacitor between this pin and analog V_{DD}.

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DB_1 to DB_8 (Pins 20 to 22, Pins 1 to 5) Digital data input pins

DB_1 to DB_8 are the 8 bit digital data input pins. The code format is binary.

Digital input code								Analog output current
DB_1 (MSB)	DB_2	DB_3	DB_4	DB_5	DB_6	DB_7	DB_8 (LSB)	
0	0	0	0	0	0	0	0	0 note
0	0	0	0	0	0	0	1	1/256 I_{FS}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	1	253/256 I_{FS}
1	1	1	1	1	1	1	0	254/256 I_{FS}
1	1	1	1	1	1	1	1	255/256 I_{FS}

note : Excluding offset current

Digital data (DB_1 to DB_8) is latched by the falling edge of the sampling clock, and converted to corresponding analog outputs.

$\overline{CLK}$ (Pin 18) Sampling clock input pin

Digital data is latched by the **falling edge** of the clock signal applied to the sampling clock input pin, and is subsequently converted to analog outputs. The maximum clock frequency is 50 MHz.

I_O (Pin 9) Analog signal output pin

$\overline{I/O}$ (Pin 10) Complementary current output pin of I_O pin

These two pins are current output pins. The full-scale output current is determined by the reference resistance R_{REF} and reference voltage V_{REF}.

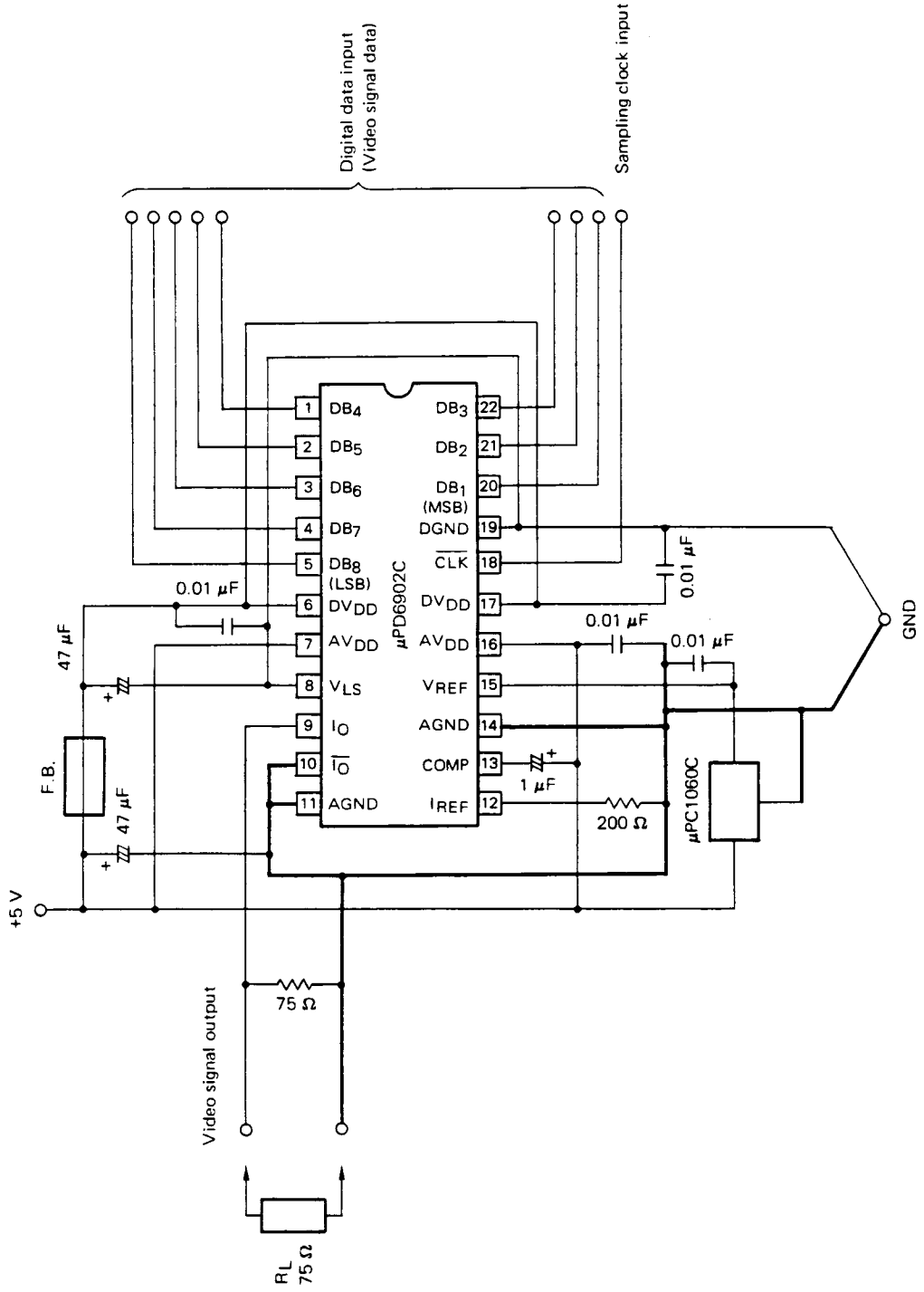
$$I_{FS} = I_O + \overline{I_O} = \frac{4}{2.5} V_{REF} / R_{REF}$$

$\overline{I_O}$ is the complementary current output pin of I_O. The added output current from the I_O and $\overline{I_O}$ pins becomes the full-scale current in accordance with the above equation. Analog output current can be easily converted to an analog output voltage by connecting a resistance between the I_O pin and analog ground. $\overline{I_O}$ pin cannot use for a complementary analog voltage output, because the compliance voltage of $\overline{I_O}$ pin is very low. Then connect $\overline{I_O}$ pin to the AGND directly.

V_{LS} (Pin 8) Digital input level select pin

This pin is used for digital input level selection. If connect to the GND the input level becomes TTL level, and to V_{DD} it becomes CMOS level.

★ APPLICATION CIRCUIT



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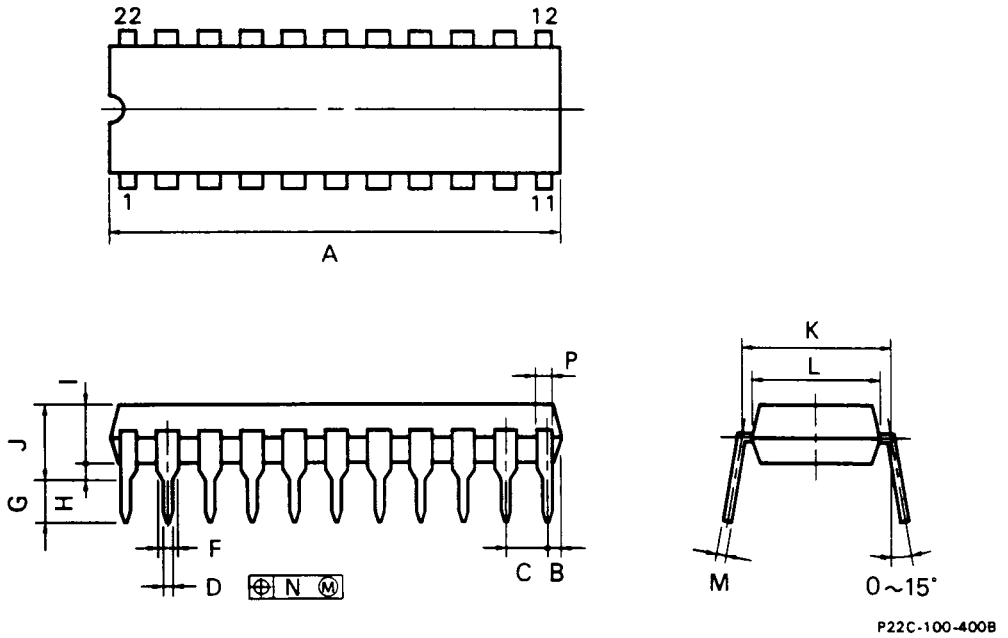
22PIN PLASTIC DIP (400 mil)



P22C-100-400B

NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	27.94 MAX.	1.100 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.72 MAX.	0.226 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
P	0.8 MIN.	0.031 MIN.