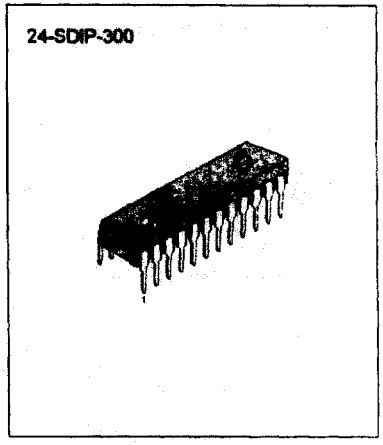
ON SCREEN DISPLAY PROCESSOR

The KS5516-XX is a CMOS LSI with on screen display function, sync separator & expander function.



FUNCTIONS

- On screen display
- Sync separator and sync detector
- General expander

FEATURES

- Character capacity:240(24 column X 10 row)
- Construction of character: 12X18 dots
- 128 kind of character
- Display position : 62 horizontal porizontal position
  : 64 vertical position
- Character size: 4X4 times of normal
- Blinking: character unit
- Back Ground coloring: 8 colors
- Synchronous ways:automatic selection internal or external synchronization
- General output: 4bit (by serial data)
- Built in sncy separator & sync detector
- Built in 4 fsc oscillation circuit
- NTSC/PAL/SECAM mode
- Clamp circuit

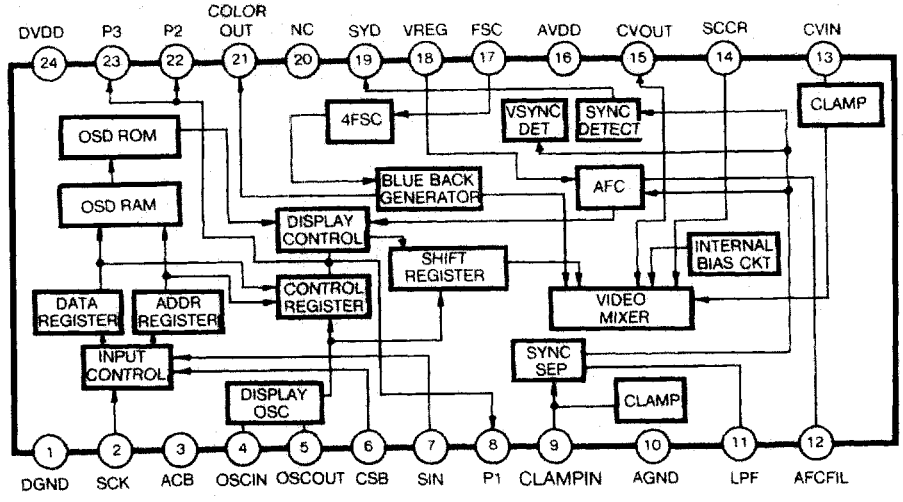
ORDERING INFORMATION

Device	Package	Operating Temperature
KS5516-XX	24-SDIP-300	-20℃~+70℃

OPTION CODE INFORMATION

Code No.	Remark
-01	English, Russian
-04	Chinese
-08	Arabian

BLOCK DIAGRAM



PIN DESCRIPTION

Pin No	Symbol	I/O	Function
1	DGND	—	Digital ground
2	SCK	I	Serial clock input. When CSB pin is "L" then serial data is inputted by micom. Hysteresis input.
3	ACB	I	Auto clear pin. If "L" then all circuit is reset built-in pull up resistor. Hysteresis input.
4 5	OSC IN OSC OUT	I O	LC oscillation pin. Standard frequency is 7MHz & the horizontal start position is controlled by the clock of oscillation block.
6	CSB	I	While pin 6 is low,serial data input is active. Built-in pull up resistor
7	SIN	I	Serial data input pin. Built-in pull up resistor
8	P1	O	General output port1
9	CLAMP IN	I	Clamp input pin of composite video signal
10	AGND	—	Analog ground
11	LPF	—	Low pass filter
12	AFCFIL	—	AFC filter output
13	CVIN	I	Composite video signal input
14	SCCR	I	Secam chroma input
15	CVOUT	O	Composite video output : $2V_{P-P}$
16	AVDD	—	Analog VDD
17	FSC	I	FSC input
18	AFCR	I	VCO oscillation frequency control
19	SYD	O	When sync signal is inputted, then SYD is high.
20	NC	—	No connection
21	COLOR OUT	O	Blueback color signal output
22	P2	O	General output port2
23	P3	O	General output port3
24	DVDD	—	Digital VDD

ABSOLUTE MAXIMUM RATINGS (T_A=25℃)

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3~6.0	V
Input voltage	V_I	V_{SS}-0.3≤V_{IN}≤V_{DD}+0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{OPR}	-20~+70	℃
Storage Temperature	T_{STG}	-40~+125	℃

ELECTRICAL CHARACTERISTICS (T_A=25℃ AV_{DD}=DV_{DD}=5V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	DV_{DD}	4.5	5.0	5.5	V
Operating Voltage	AV_{DD}	4.5	5.0	5.5	V
Operating Current	I_{CC}	10	18	25	mA
PIN 12 DC Voltage	V_{P12}	2.25	2.5	2.75	V
PIN 13 DC Voltage	V_{P13}	1.3	1.45	1.6	V
AFC Freerun Frequency	F_{FR}	15.5	15.7	15.9	KHz
AFC Pulse Width	t_{WD}	3.7	4.0	4.3	usec
AFC Delay Time	t_D	1.0	2.5	4.0	usec
AFC Lock Range H	F_{ALH}	+600	—	—	Hz
AFC Lock Range L	F_{ALL}	—	—	-900	Hz
AFC Capture Range H	F_{ACH}	+400	—	—	Hz
AFC Capture Range L	F_{ACL}	—	—	-700	Hz
SYNC DET. Lock Range H	F_{LH}	143	153	163	KHz
SYNC DET. Lock Range L	F_{LL}	6.7	7.7	8.7	KHz
SYNC DET. Capture Range H	F_{CH}	100	107	114	KHz
SYNC DET. Capture Range L	F_{CL}	14.3	15.3	16.3	KHz
V-SYNC Delay Time	t_{VD}	10	14	—	usec
Oscillation Level	V_{OSC}	3.0	3.5	4.0	V_{PP}
Oscillation Frequency	F_{OSC}	6.3	7.0	7.7	MHz
Blueback Sync Tip Level	V_{BST}	1.1	1.3	1.5	V
Blueback Pedestal Level	V_{BPD}	1.75	1.95	2.15	V
Blueback Color Burst Level H	V_{BBH}	2.0	2.2	2.4	V
Blueback Color Level H	V_{BCH}	2.55	2.75	2.95	V
FSC Input Level	V_{FSC}	1.2	1.5	2.0	V_{PP}

OPERATION DESCRIPTION

MEMORY STRUCTURE

After recording the serial data from μ-COM to RAM and control register, it is need by H-sync and V-sync that detecting from composite video signal, and then mix the character data of ROM to composite video signal.

When composite video signal is input, KS5516 output the blueback signal by divide and mixture the 4 fsc signal.

The following table is data structure from MICOM.

- Memory address consists of 16 bit
- The datd of address 0-239 is character data which is display on the screen.
- The address 240-244 is the control resister
- The upper 4 bit don't care bit

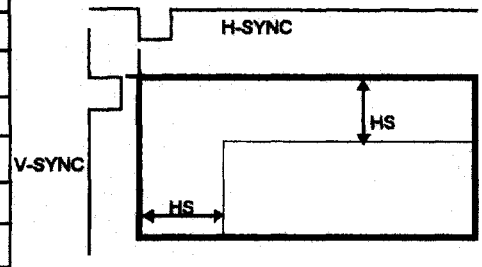
Bit / Addr	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	0	0	0	0	P	CH2	CH1	CH0	BLI	C6	C5	C4	C3	C2	C1	C0
												(ROM Address)				
.			.				.					.				
.			.				.					.				
.			.				.					.				
239	0	0	0	0	P	CH2	CH1	CH0	BLI	C6	C5	C4	C3	C2	C1	C0
240	0	0	0	0	P	INT NON	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0
241	0	0	0	0	P	BLI2	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0
242	0	0	0	0	P	DSP 3	DSP 2	DSP 1	RAM ERS	TEST	TC	LEV 1	LEV 0	PH2	PH1	PH0
243	0	0	0	0	P	—	LE BK	LE CHA	DSP ON	BLK 1	BLK 0	BLI 1	BLI 0	EX	YM	BCO
244	0	0	0	0	P	$\overline{\text{SECAM}}$	NT/ PAL	—	PD3	PD2	—	PD0	PC3	PC2	PC1	PC0

CONTROL REGISTER

1) Register 240

<table>
<tr><th rowspan="2">DA0~
DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>HP0</td><td>0
1</td><td rowspan="8">HS is horizontal display start position
$HS = T_C * \{4 * (\sum_{n=0}^{5} HPn * 2^n) + N\}$
T_C:OSC, Period (1/7MHz=143 nsec)
<table><tr><th>HSZ11
HSZ21</th><th>HSZ10
HSZ20</th><th>N</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="8">Horizontal start position</td></tr>
<tr><td>1</td><td>HP1</td><td>0
1</td></tr>
<tr><td>2</td><td>HP2</td><td>0
1</td></tr>
<tr><td>3</td><td>HP3</td><td>0
1</td></tr>
<tr><td>4</td><td>HP4</td><td>0
1</td></tr>
<tr><td>5</td><td>HP5</td><td>0
1</td></tr>
<tr><td>6</td><td>HSZ10</td><td>0
1</td><td rowspan="2">1st line
<table><tr><th>HSZ11 \ HSZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">1'st line character size control to horizontal direction</td></tr>
<tr><td>7</td><td>HSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>HSZ20</td><td>0
1</td><td rowspan="2">2nd~10th line
<table><tr><th>HSZ21 \ HSZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">2nd-10th line character size control to horizontal direction</td></tr>
<tr><td>9</td><td>HSZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>INT/
NON</td><td>0
1</td><td>Interlace mode
Non interlace mode</td><td>—</td></tr>
</table>

2) Register 241

<table>
<tr><th rowspan="2">DA0~
DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>VP0</td><td>0
1</td><td rowspan="6">VS is Vertical start position
$VS = H*\{4*(\sum_{n=0}^{5} VPn*2^n)+3\}$
H: horizontal synchronous pulse time
 
</td><td rowspan="6">Vertical start position</td></tr>
<tr><td>1</td><td>VP1</td><td>0
1</td></tr>
<tr><td>2</td><td>VP2</td><td>0
1</td></tr>
<tr><td>3</td><td>VP3</td><td>0
1</td></tr>
<tr><td>4</td><td>VP4</td><td>0
1</td></tr>
<tr><td>5</td><td>VP5</td><td>0
1</td></tr>
<tr><td>6</td><td>VSZ10</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ11 \ VSZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">1'st line character size control to vertical direction</td></tr>
<tr><td>7</td><td>VSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>VSZ20</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ21 \ VSZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">2th-10th line character size control to vertical direction</td></tr>
<tr><td>9</td><td>VSZ21</td><td>0
1</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">BLI2</td><td>0</td><td>V-SYNC 64 divide (=1sec)</td><td rowspan="2">Control the blink period</td></tr>
<tr><td>1</td><td>V-SYNC 32 divide (=0.5sec)</td></tr>
</table>

3) Register 242

<table>
<tr><th rowspan="2">DA0~
DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>PH0</td><td>0</td><td rowspan="8"><table><tr><th>P2</th><th>P1</th><th>P0</th><th>NTSC</th><th>PAL</th></tr><tr><td>0</td><td>0</td><td>0</td><td>black</td><td>black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>π/2</td><td>π/2</td></tr><tr><td>0</td><td>1</td><td>0</td><td>7π/4</td><td>+ π/4</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>π</td><td>± π</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3π/4</td><td>3π/4</td></tr><tr><td>1</td><td>1</td><td>0</td><td>3π/2</td><td>3π/2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>white</td><td>white</td></tr></table></td><td rowspan="8">Back ground color control bit</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>1</td><td>PH1</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>2</td><td>PH2</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>3</td><td>LEVEL0</td><td>0</td><td rowspan="4"><table><tr><th>Level 1 \ Level 0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Internal bias 1</td><td>Internal bias 2</td></tr><tr><td>1</td><td>—</td><td>Internal bias 3</td></tr></table></td><td rowspan="4">Color level control</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>4</td><td>LEVEL1</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td></tr>
<tr><td>5</td><td>TC</td><td>0</td><td colspan="2">1H=454T_C T_C=2f_{osc}</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">1H=455T_C</td></tr>
<tr><td>6</td><td>TEST</td><td>0</td><td colspan="2">Active mode</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">Test mode</td></tr>
<tr><td>7</td><td>RAM ERS</td><td>0</td><td colspan="2">RAM no erase</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">RAM erase</td></tr>
<tr><td>8</td><td>DSP1</td><td>0</td><td colspan="2">Display method of the first is fixed by BLK0 & BLK1</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">Display method of the first is variable</td></tr>
<tr><td>9</td><td>DSP2</td><td>0</td><td colspan="2">Display method of 2nd-9th is fixed by BLK0 & BLK1</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">Display method of 2nd-9th is variable</td></tr>
<tr><td>A</td><td>DSP3</td><td>0</td><td colspan="2">Display method of 10th is fixed by BLK0 & BLK1</td></tr>
<tr><td></td><td></td><td>1</td><td colspan="2">Display method of 10th is variable</td></tr>
</table>

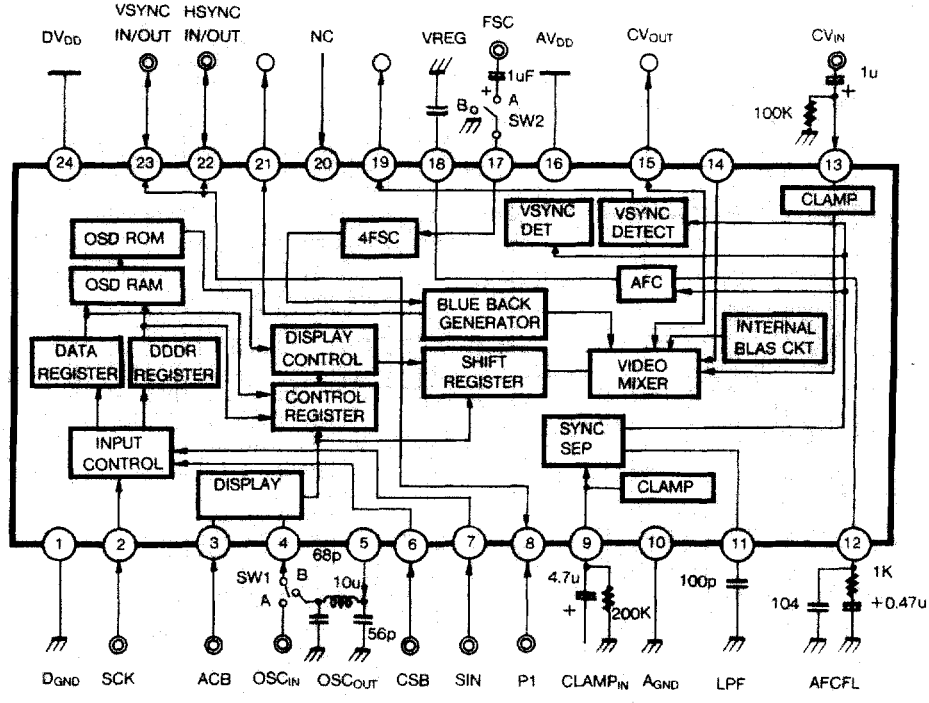
4) Register 243

<table>
<tr><th rowspan="2">DA0~
DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BC0</td><td>0</td><td>Blanking area coloring</td><td rowspan="2">Determined by
BLK0 & BLK1</td></tr>
<tr><td>1</td><td>Full TV screen coloring</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">YM</td><td>0</td><td>The same character & back ground</td><td rowspan="2">Determined by BC0
BLK0 & BLK1</td></tr>
<tr><td>1</td><td>Variable back available</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EX</td><td>0</td><td>External mode available</td><td rowspan="2">–</td></tr>
<tr><td>1</td><td>Internal mode available</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">BLI0</td><td>0</td><td rowspan="3">Blinking mode control
<table><tr><th>BLI1 \ BLI0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Off</td><td>Duty25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty75%</td></tr></table></td><td rowspan="3">Blinking
duty
control</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BLI1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="3">Blinking mode control
<table><tr><th>BLK 1 \ BLK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Off</td><td>C</td></tr><tr><td>1</td><td>O</td><td>R</td></tr></table></td><td rowspan="3">C: character
O; outline
R: raster</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">DSP
ON</td><td>0</td><td>Display off</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Display on</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">LECHA</td><td>0</td><td>Character luminance level 1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Character luminance level 2</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">LEBK</td><td>0</td><td>Blank luminance level 1</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Blank luminance level 2</td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">–</td><td>0</td><td>–</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>–</td></tr>
</table>

5) Register 244

<table>
<tr><th rowspan="2">DA0~
DAA</th><th rowspan="2">Register</th><th colspan="2">Content</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>0</td><td>PC0</td><td>0
1</td><td rowspan="3">PC1 \ PC0 | 0 | 1
0 | Hsync/Vsync output | —
1 | Port output | CH1, output</td><td rowspan="3">Pin 8 output mode setting</td></tr>
<tr><td>1</td><td>PC1</td><td>0
1</td></tr>
<tr><td>2</td><td>PC2</td><td>0
1</td></tr>
<tr><td>3</td><td>PC3</td><td>0
1</td><td>PC3 \ PC2 | 0 | 1
0 | Hsync/Vsync output | Test Mode
1 | Port output | CH2, BLI2 output</td><td>Pin 22/23 output mode setting</td></tr>
<tr><td>4</td><td>PD0</td><td>0
1</td><td>L output
H output</td><td>Pin8 output data setting</td></tr>
<tr><td>5</td><td>—</td><td>0
1</td><td>—
—</td><td>—</td></tr>
<tr><td>6</td><td>PD2</td><td>0
1</td><td>L output
H output</td><td>Pin22 output data setting</td></tr>
<tr><td>7</td><td>PD3</td><td>0
1</td><td>L output
H output</td><td>Pin23 output data setting</td></tr>
<tr><td>8</td><td>—</td><td>0
1</td><td>—
—</td><td></td></tr>
<tr><td>9</td><td>NT/
PAL</td><td>0
1</td><td>NTSC mode
PAL mode</td><td></td></tr>
<tr><td>A</td><td>$\overline{\text{SECAM}}$</td><td>0
1</td><td>NTSC or PAL mode
SECAM mode</td><td></td></tr>
</table>

TEST CIRCUIT



APPLICATION CIRCUIT