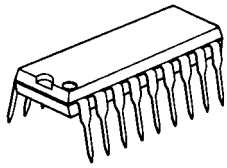
FDD READ AMPLIFIER SYSTEM

■ GENERAL DESCRIPTION

The **NJM3470/3470A** are monolithic read amplifier systems for obtaining digital signal from floppy disk storage.

The **NJM3470/3470A** are designed to get pulse output signal produced by the magnetic head amp of the input signal. They contain amplifiers, peak detector, and pulse shape circuit. They are classified two ranks by peak shift characteristic; **NJM3470** (5%), **NJM3470A** (2%).

■ PACKAGE OUTLINE

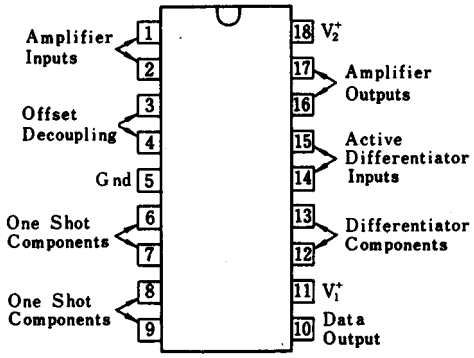


NJM3470D/3470AD

■ FEATURES

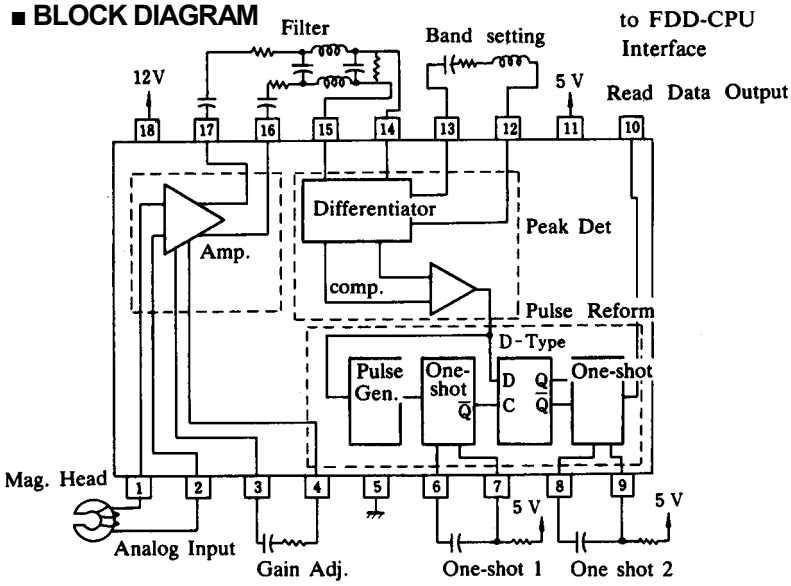
- Gain Adjastable
- Wide Bandwidth (5MHz min. @-3dB)
- Peak Shift (A-rank : 2%max.)
- Package Outline DIP18
- Bipolar Technology

■ PIN CONFIGURATION



NJM3470D/3470AD

■ BLOCK DIAGRAM



NJM3470 BLOCK DIAGRAM
and
STANDARD OUTPUT CIRCUIT

■ ABSOLUTE MAXIMUM RATINGS

(T_a = 25ºC)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage I (Pin 11)	V^+_1	7	V
Supply Voltage II (Pin 18)	V^+_2	16	V
Input Voltage (Pin 1-2)	V_{IN}	-0.2 to 7.0	V
Output Voltage (Pin 10)	V_O	-0.2 to 7.0	V
Operating Temperature Range	T_{opr}	-20 to +75	ºC
Storage Temperature Range	T_{stg}	-40 to +125	ºC

■ **ELECTRICAL CHARACTERISTICS** (Ta = 25ºC, V^+_1 = 5V, V^+_2 = 12V) note: ( ) apply to A-rank.

Amplifier Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differential Voltage Gain	A_{VD}	f = 200kHz, V_{ID} = 5.0mVrms	80 (100)	100 (110)	120 (120)	V/V
Input Bias Current	I_{IB}		-	-10	-25	µA
Input Common Mode Range	V_{ICM}	THD = 5%	-0.1	-	1.0	V
Differential Input Voltage Range	V_{ID}	THD = 5%	-	-	25	mV_{P-P}
Output Voltage Swing Differential	V_{OD}		3.0	4.0	-	V_{P-P}
Output Source Current	I_{SOURCE}		-	8.0	-	mA
Output Sink Current	I_{SINK}		2.8	4.0	-	mA
Small Signal Input Resistance	r_i		100	250	-	kΩ
Small Signal Output Resistance	r_o		-	15	-	Ω
Bandwidth, -3.0dB	BW	V_{ID} = 2.0mVrms	5.0	-	-	MHz
Common Mode Rejection Ratio	CMR	f=100kHz, A_{VD} = 40dB, Vin = $200mV_{p-p}$	50	-	-	dB
Supply Voltage Rejection Ratio (V_1^+)	$SVRR_1$	A_{VD} = 40dB, 4.75 ≤ V_1^+ ≤ 5.25V	50	-	-	dB
Supply Voltage Rejection Ratio (V_2^+)	$SVRR_2$	A_{VD} = 40dB, 10 ≤ V_2^+ ≤ 14V	60	-	-	dB
Differential Output Offset	V_{DO}	V_{ID} = V_{IN} = 0V	-	-	0.4	V
Common Mode Output Offset	V_{CO}	V_{ID} = V_{IN} = 0V	-	3.0	-	V
Equivalent Input Noise Voltage	e_n	BW = 10Hz to 1.0MHz	-	15	-	µVrms

Peak Detector Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Differentiator Output Sink Current	I_{OD}	V_{OD} = 5V	1.0	1.4	-	mA
Peak Shift	PS	f = 250kHz, V_{ID} = $1.0V_{P-P}$, i_{cap} = 500µA			5.0	%
		PS = t_{PS1}-t_{PS2}/2 (t_{PS1} + t_{PS2}) x100			(2.0)	%
Differentiator Input Resistance, Differenial	r_{ID}		-	30	-	kΩ
Differentiator Output Resistance, Differential	r_{OD}		-	40	-	Ω

Logic Block

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Timing Accuracy (mono #1)	E_{t1}	t_1=1.0µS = $0.625R_1C_1$ + 200nS R_1 = 6.4kΩ C_1 = 200pF (accuracy : R_1, C_1) 1.5kΩ ≤ R_1 ≤ 10 kΩ 150pF ≤ C_1 ≤ 680pF	85	-	115	%
Timing Range (mono #2)	t_2		150	-	1000	nS
Timing Accuracy (mono #2)	E_{t2}	t_2 = 200nS = $0.625R_2C_2$ R_2 = 1.6 kΩ C_2 = 200pF (accuracy; R_2, C_2) 1.5 kΩ ≤ R_2 ≤ 10 kΩ 100pF ≤ C_2 ≤ 800pF	85	-	115	%

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