51C65H
HIGH PERFORMANCE STATIC COLUMN 64K X 1 CHMOS DYNAMIC RAM

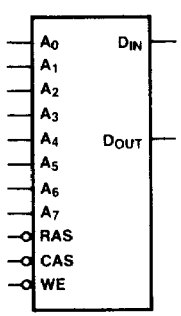
	51C65H-10	51C65H-12
Maximum Access Time (ns)	100	120
Maximum Column Address Access Time (ns)	55	65

- **Static Column Mode Operation**
  - **Continuous data rate over 15 MHz**
  - **Random access from address within row**
- **Low Input/Output Capacitance**
- **Low Operating Current — 37mA (max.)**
- **Fast "Usable Speed"**
  - **t_{CAC} = 20, 25 ns**
- **Fully TTL Compatible**
- **High Reliability Plastic — 16 Pin DIP**

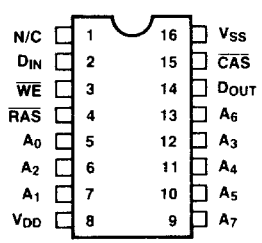
The Intel® 51C65H is a high speed 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C65H offers features not provided by an NMOS dynamic RAM: Static Column Mode for high data bandwidth and fast usable speed. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

Static Column Mode operation allows random or sequential access of all 256 bits within a row simply by changing the column address. Because column address access time is as fast as 55 ns, a continuous data rate of over 15 million bits per second can be achieved. The 51C65H offers high performance while relaxing many critical system timing requirements for fast usable speed. These features make the 51C65H ideally suited for graphics, digital signal processing, and high performance systems.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_7	ADDRESS INPUTS
D_{IN}	DATA IN
D_{OUT}	DATA OUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

June, 1984
Order Number: 280027-001

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias . . . . . −10° to +80°C
Storage Temperature . . Plastic −55°C to +125°C
Voltage on Any Pin except V_{DD} and D_{OUT} Relative to V_{SS} . . . . . −2.0V to 7.5V
Voltage on D_{OUT} Relative to V_{SS} . . . . . −2.0V to V_{DD}+1V
Voltage on V_{DD} Relative to V_{SS} . . . . −1.0V to 7.5V
Data Out Current . . . . . 50 mA
Power Dissipation . . . . . 1.0 W

*COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and fuctional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°C$ to 70°C, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	51C65H Limits			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
$I_{DD\,1}$	V_{DD} Supply Current, Operating		27	37	mA	$t_{RC} = t_{RC}$ (min), for −10 A.C. spec	3,4
			23	35	mA	$t_{RC} = t_{RC}$ (min), for −12 A.C. spec.	
$I_{DD\,2}$	V_{DD} Supply Current, TTL Standby		0.7	4	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH} all other inputs and outputs ≥ V_{SS}	
$I_{DD\,3}$	V_{DD} Supply Current, $\overline{RAS}$-Only Cycle		24	37	mA	$t_{RC} = t_{RC}$ (min), for −10 A.C. spec	3,4
			20	35	mA	$t_{RC} = t_{RC}$ (min), for −12 A.C. spec	
$I_{DD\,4}$	V_{DD} Supply Current, Static Column Mode		18	37	mA	Minimum Cycle for −10 A.C. spec	3,4
			17	35	mA	Minimum Cycle for −12 A.C. spec	
$I_{DD\,5}$	V_{DD} Supply Current Standby, Output Enabled		3	6	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and output ≥ V_{SS}	3
$\|I_{LI}\|$	Input Load Current (any input)			10	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			10	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		7.0	V		5
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.2$ mA	6
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -5$ mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are to $T_A = 25°C$ and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Static Column Mode.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) ≥ V_{SS} and V_{IH} (max) ≤ V_{DD}.
6. Test conditions apply only for D.C. characteristics. A.C. parameters specified with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, Data In	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	Data Out	4	6	pF

†NOTE:
Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS[1,2,3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Read, Refresh and Write Cycles

#	JEDEC Symbol	Symbol	Parameter	51C65H-10		51C65H-12		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}*	$\overline{CAS}$ Hold Time	100		120		ns	
5	t_{WH2RL2}	t_{WRP}	Write to $\overline{RAS}$ Precharge Time	−5		−5		ns	
6	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
7	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		ns	
8	t_{RL1QZ}	t_{RHZ}	$\overline{RAS}$ to Output High Impedance		15		15	ns	4
9	t_{RL1QX}	t_{RLZ}	$\overline{RAS}$ to Output Low Impedance	30		30		ns	4
10	t_{CH2QZ}	t_{HZ}*	$\overline{CAS}$ to Output Low Impedance	0	20	0	20	ns	4,5
11	t_{CL1QX}	t_{LZ}*	$\overline{CAS}$ to Output Low Impedance	0		0		ns	4,5
	t_{RVRV}	t_{REF}	Time Between Refresh		4		4	ms	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6

NOTES:
* This parameter not applicable if operated with $\overline{CAS}$ grounded.
1. All Voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
3. A.C. characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
4. Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
5. At any given temperature and voltage combination, t_{HZ} (max) is less than t_{LZ} (min) from device to device.
6. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	51C65H-10		51C65H-12		Unit	Notes
				Min.	Max.	Min.	Max.		
12	t_{RL1QV}	t_{RAC}	Access Time From $\overline{RAS}$		100		120	ns	7
13	t_{CL1QV}	t_{CAC}*	Access Time From $\overline{CAS}$		20		25	ns	
14	t_{AVQV}	t_{CAA}	Access Time From Column Address		55		65	ns	
15	t_{CL1CH1}	$t_{CAS(R)}$*	$\overline{CAS}$ Pulse Width (Read Cycle)	20		25		ns	
16	t_{CL1RH1}	$t_{RSH(R)}$*	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		ns	
17	t_{WH2CL2}	t_{RCS}*	Read Command Set-up Time	0		0		ns	
18	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	90		110		ns	
19	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	55		65		ns	
20	t_{CH2WX}	t_{RCH}*	Read Command Hold Time referenced to $\overline{CAS}$	0		0		ns	
21	t_{RH2WX}	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10		10		ns	
22	t_{RH2AX}	t_{ARH}	Column Address Hold Time referenced to $\overline{RAS}$	0		0		ns	
23	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	45	20	55	ns	8

Write Cycle

24	$t_{CL1CH1(W)}$	$t_{CAS(W)}$*	$\overline{CAS}$ Pulse Width (Write Cycle)	30		35		ns	
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$*	$\overline{RAS}$ Hold Time (Write Cycle)	35		40		ns	
26	t_{RL1WL2}	t_{WDR}	$\overline{RAS}$ to Write Command Delay Time	30		35		ns	
27	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
28	t_{WL1CH1}	t_{CWL}*	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
29	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	30		35		ns	
30	t_{WH2WL2}	t_{WCP}	Write Command Precharge Time	10		15		ns	
31	t_{WL1CL2}	t_{WCS}*	Write Command Set-up Time	0		0		ns	9
32	t_{CL1WH1}	t_{WCH}*	Write Command Hold Time	30		35		ns	
33	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	80		90		ns	
34	t_{AVWL2}	t_{AWS1}	Column Address to Write Command Set-up Time	5		5		ns	10
35	t_{AVWL2}	t_{AWS2}	Column Address to Write Command Set-up Time	55		65		ns	11
36	t_{WL1AX}	t_{AWH}	Column Address to Write Command Hold Time	15		20		ns	
37	t_{DVWL2}	t_{DS}	Data-In Set-up Time	0		0		ns	
38	t_{WL1DX}	t_{DH}	Data-In Hold Time	20		25		ns	
39	t_{WH2QX}	t_{OW}	Output Active From End of Write	0		0		ns	

NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

7. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If $t_{RAD} > t_{RAD}$ (max), then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max).
8. t_{RAD} specified for reference only.
9. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.
10. t_{AWS1} is applicable for a $\overline{CAS}$ controlled write operation, i.e., the leading edge of $\overline{WE}$ is low prior to or coincident with a $\overline{CAS}$ low transition.
11. Under typical TTL conditions ($V_{IH} \geq 3V$) and low supply inductance $t_{AWS2} = t_{AWS1}$. Otherwise, t_{AWS2} is applicable for a $\overline{WE}$ controlled write operation, i.e., the leading edge of $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write Cycle[12]

#	JEDEC Symbol	Symbol	Parameter	51C65H-10		51C65H-12		Unit	Notes
				Min.	Max.	Min.	Max.		
40	$t_{RL2RL2\ (RMW)}$	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	195		230		ns	
41	$t_{RL1RH1\ (RMW)}$	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	135	75000	160	75000	ns	
42	$t_{CL1CH1\ (RMW)}$	t_{CRW}*	RMW Cycle $\overline{CAS}$ Pulse Width	55		65		ns	
43	t_{RH2WH1}	t_{RWH}	$\overline{RAS}$ to $\overline{WE}$ Hold Time	5		5		ns	
44	t_{RL2WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		ns	13
45	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	55		65		ns	13
46	t_{CL1WL2}	t_{CWD}*	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		ns	13

Static Column Mode[14]

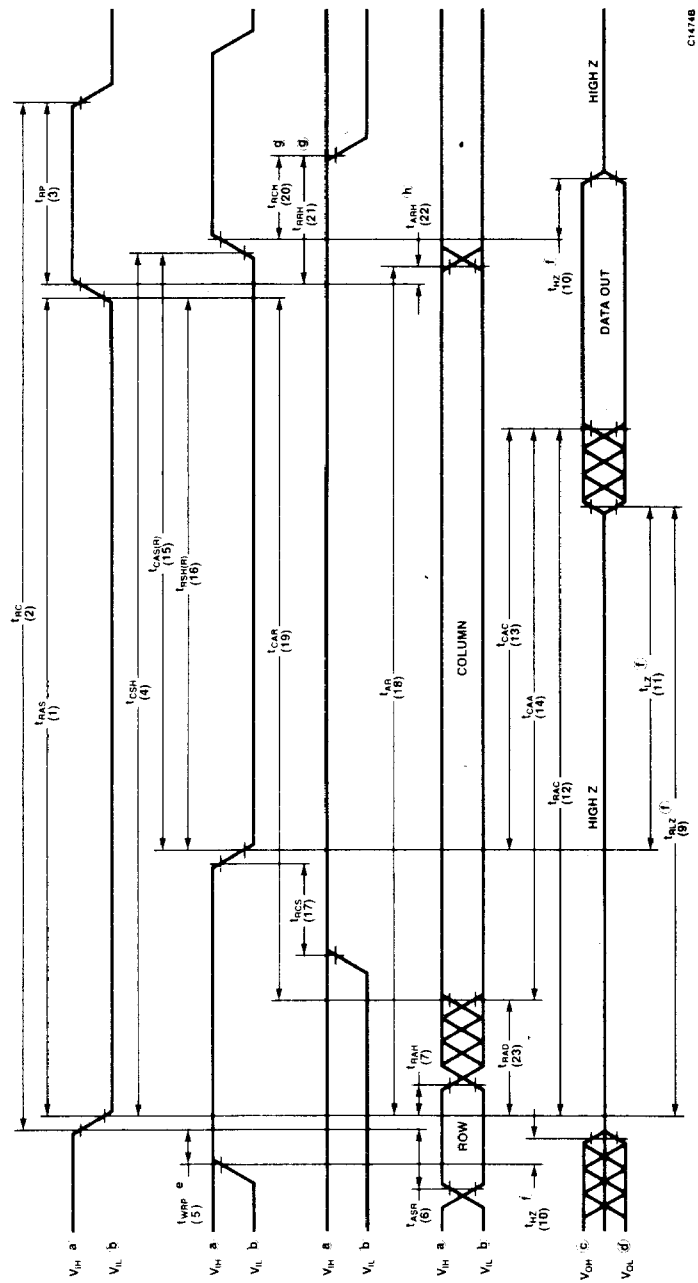
#	JEDEC Symbol	Symbol	Parameter	51C65H-10		51C65H-12		Unit	Notes
				Min.	Max.	Min.	Max.		
47	t_{AXQX}	t_{OHA}	Output Hold Time From Address Change	10		10		ns	
48	t_{WH2QX}	t_{OHW}	Output Hold Time From End of Write	0		0		ns	
49	t_{WH2QV}	t_{WPA}	RMW Write Precharge Access Time		70		80	ns	15
50	t_{WL1QV}	t_{WRA}	RMW Write-Read Access Time		105		120	ns	15
51	t_{WH2WL2}	t_{WPS}	RMW Write Command Prcharge Time	55		65		ns	

NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

12. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
13. t_{WCS}, t_{RWD}, t_{WCD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data pin will remain high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.
14. All previously specified A.C. characteristics are applicable.
15. Access time from a write command to a read command is determined by the longer of t_{CAA} or t_{WPA} or t_{WRA}.

WAVEFORMS
Read Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

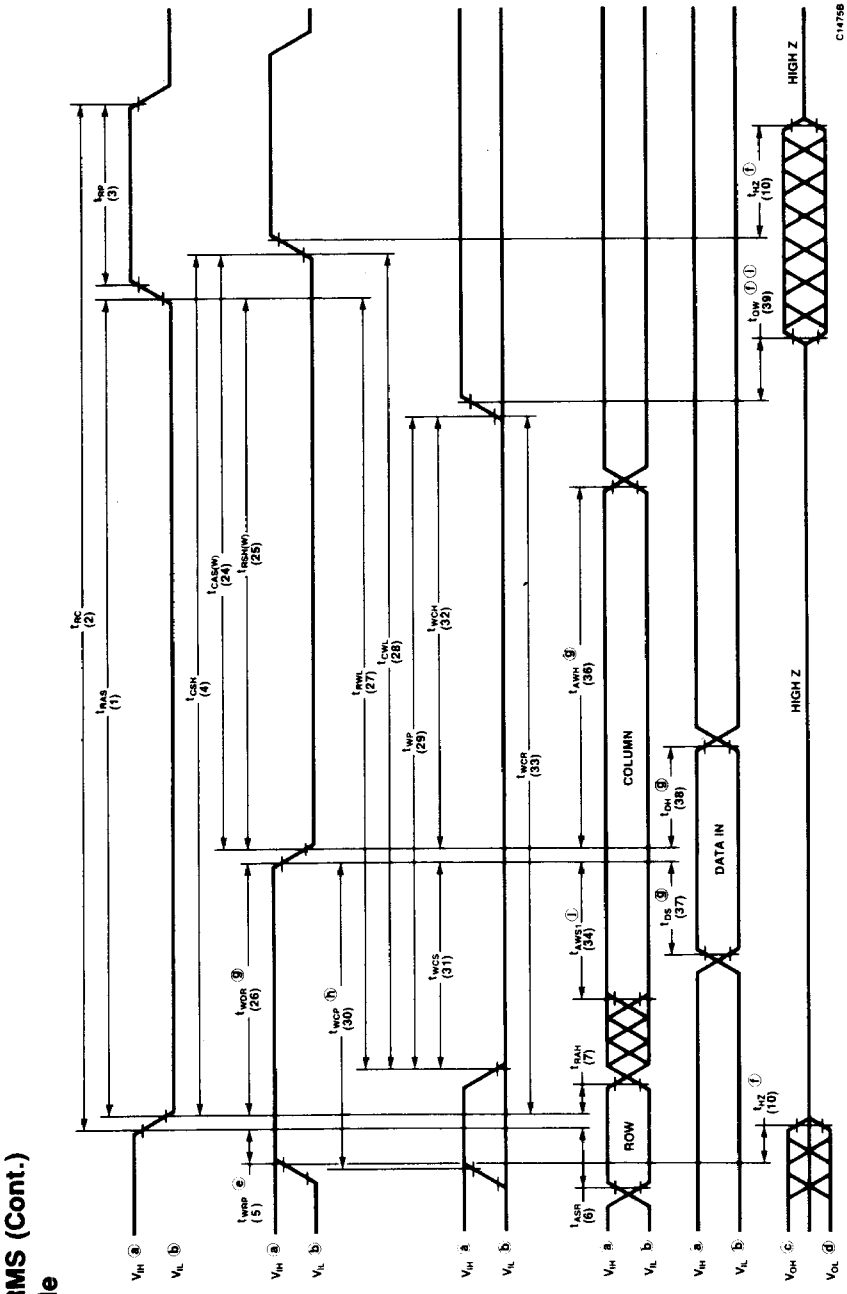
e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. Either t_{RCH} or t_{RRH} must be satisfied.

h. If $t_{ARH} \geq t_{AAH}$ (min), then data from the last address will be latched on D_{OUT}, as long as D_{OUT} is held in low impedance by $\overline{CAS}$.

WAVEFORMS (Cont.)
Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

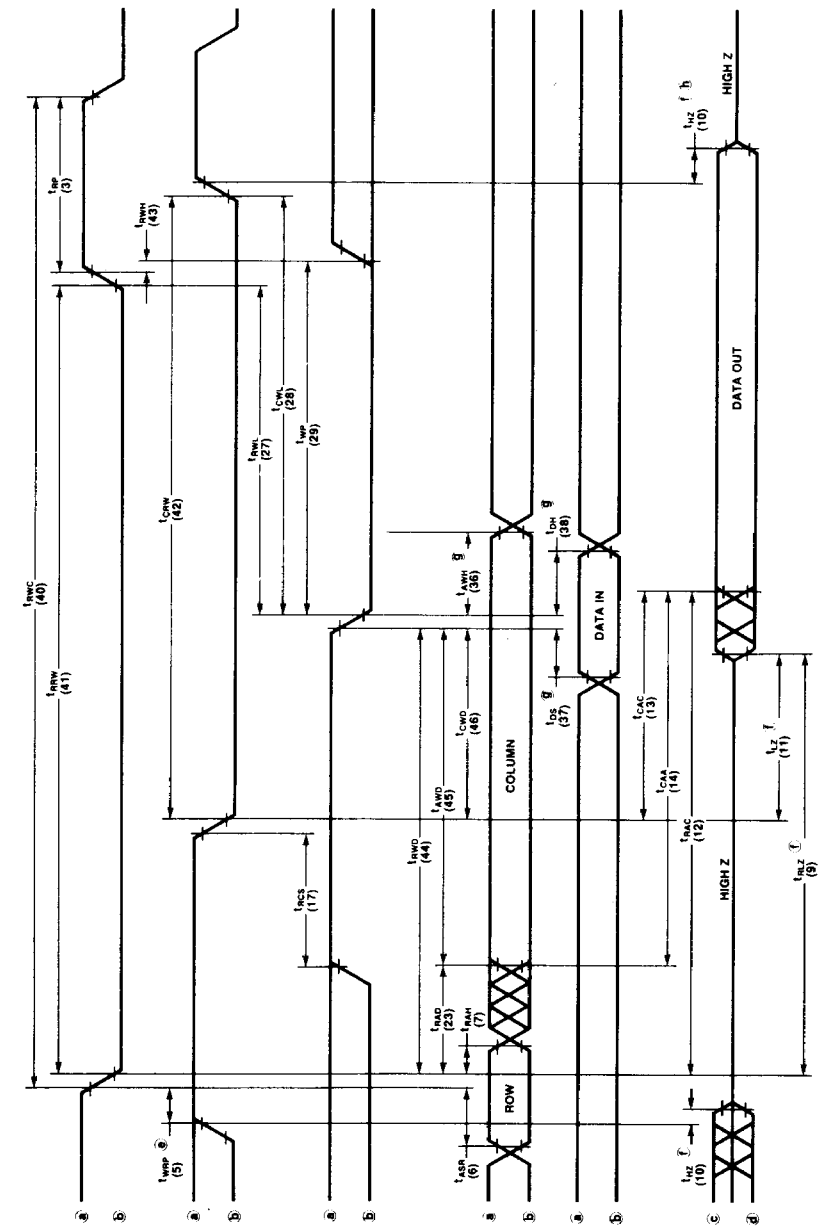
g. t_{AWH}, t_{DS}, t_{DH} and t_{WOR} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.

h. t_{WCP} (min) is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. If $\overline{CAS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance.

j. If a $\overline{WE}$ low transition occurs after a $\overline{CAS}$ low transition, t_{AWS2} is applicable.

WAVEFORMS (Cont.)
Read/Modify/Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

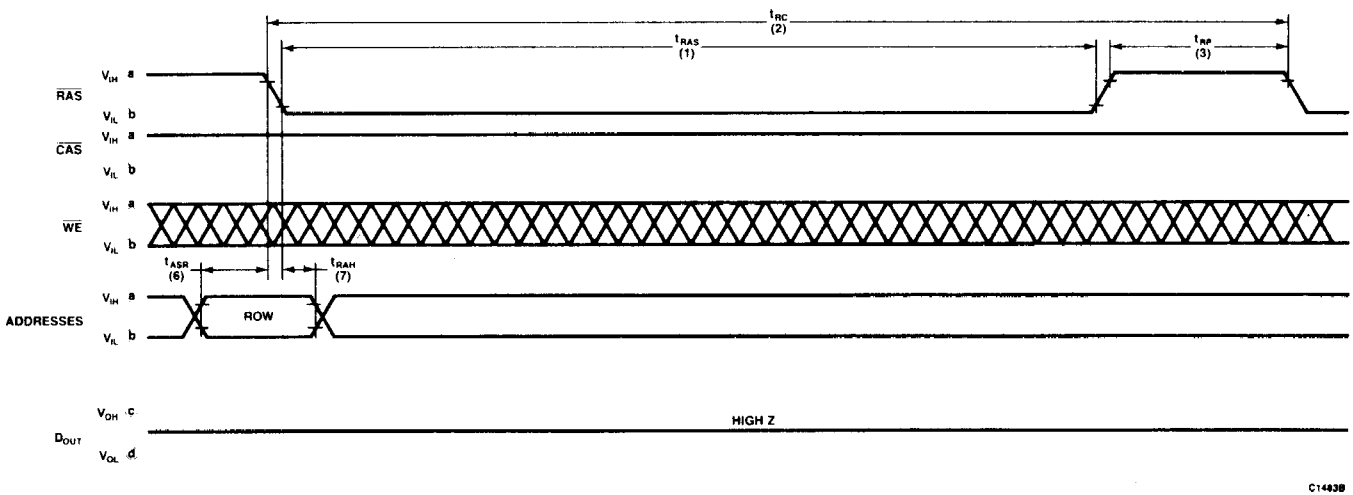
e. t_{WRP} is referenced to $\overline{CAS}$ of $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.

h. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{RWH} \geq t_{RWH}$ (min).

WAVEFORMS (Cont.)
$\overline{RAS}$-Only Refresh Cycle

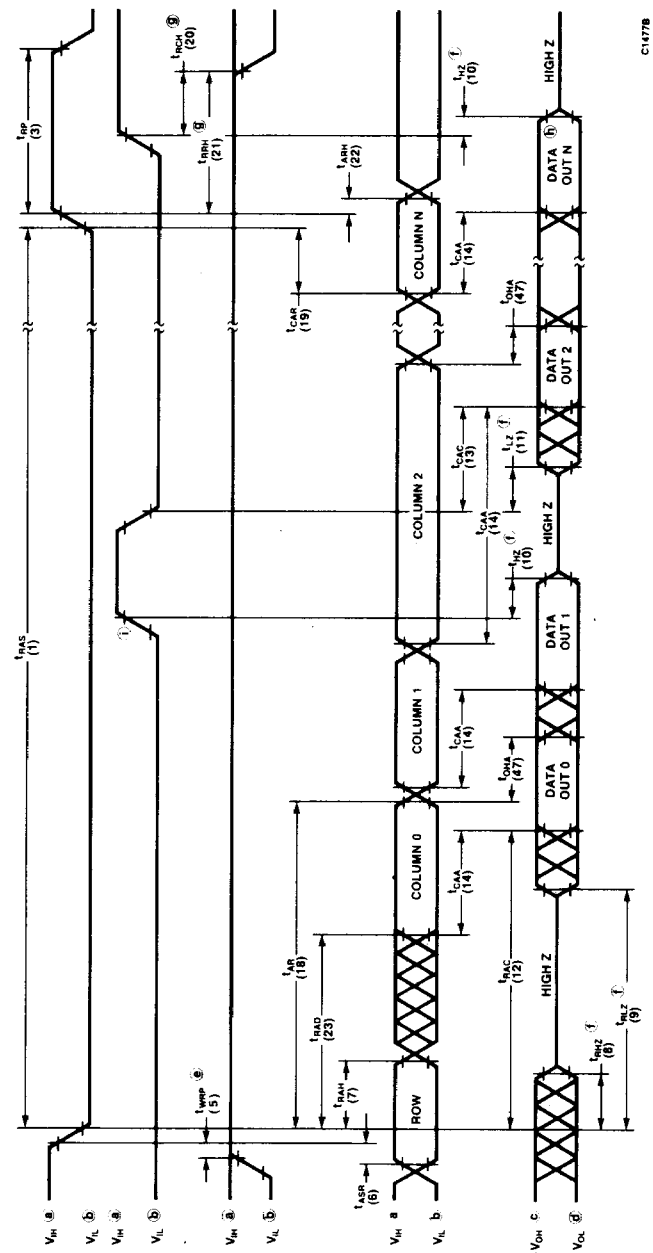


NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

WAVEFORMS (Cont.)
Static Column Mode Read Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

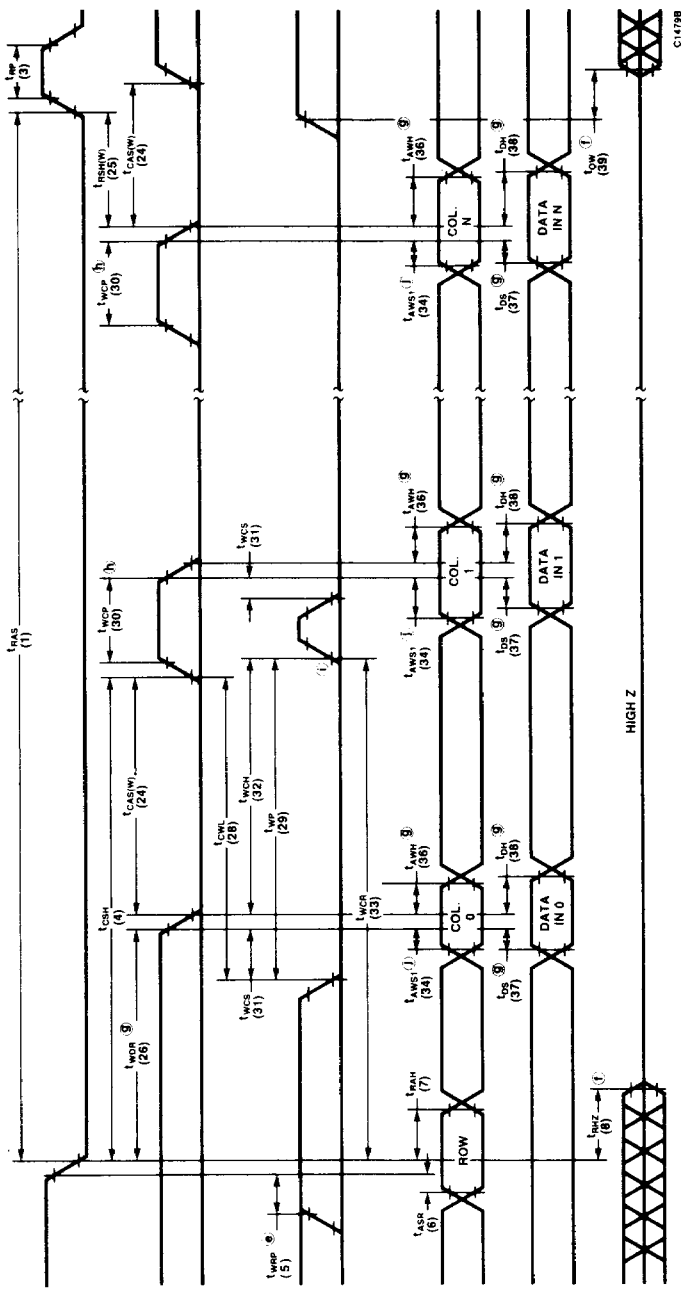
f. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. Either t_{RCH} or t_{RRH} must be satisfied.

h. D_{OUT} is valid as shown if and only if $t_{ARH} \geq t_{ARH}$ (min).

i. $\overline{CAS}$ pulse is shown for reference. In this case, D_{OUT} will go to high impedance.

WAVEFORMS (Cont.)
Static Column Mode Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

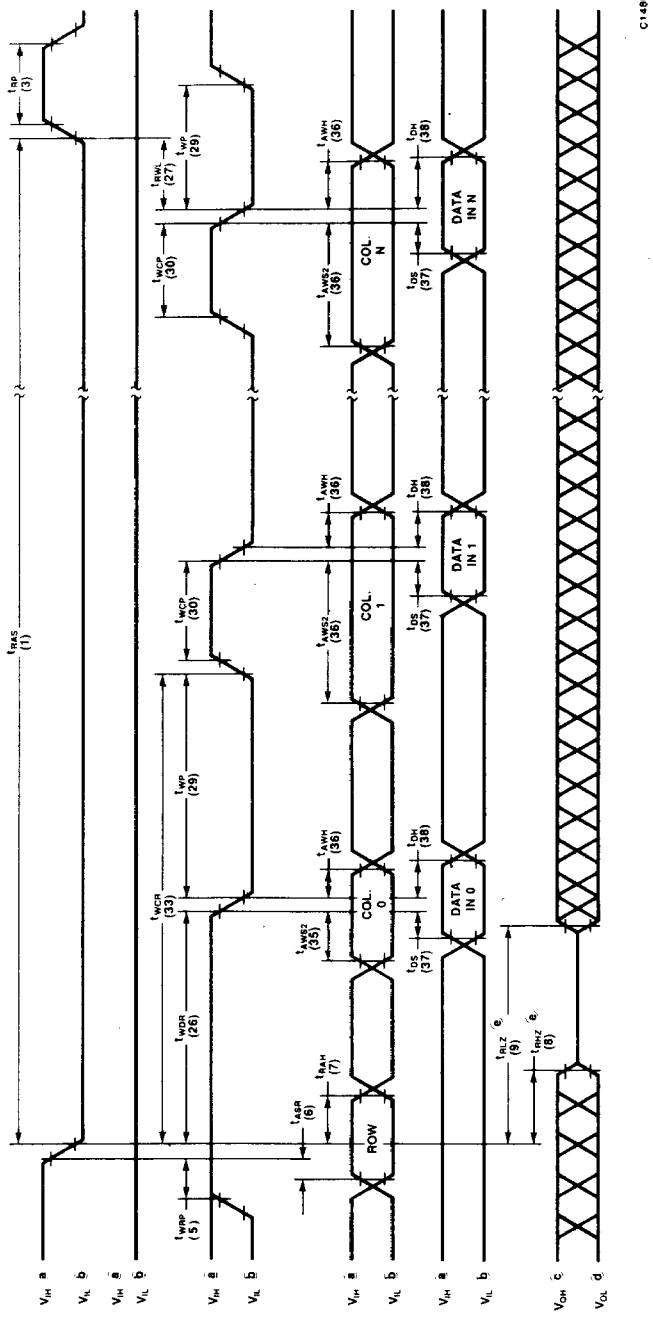
g. t_{AWH}, t_{DS}, t_{DH} and t_{WDR} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.

h. t_{WCP} (min) is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. If $\overline{CAS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance

j. If a $\overline{WE}$ low transition occurs after a $\overline{CAS}$ low transition, t_{AWS2} is applicable.

WAVEFORMS (Cont.)
Static Column Mode Write Cycle ($\overline{CAS}$ Low)



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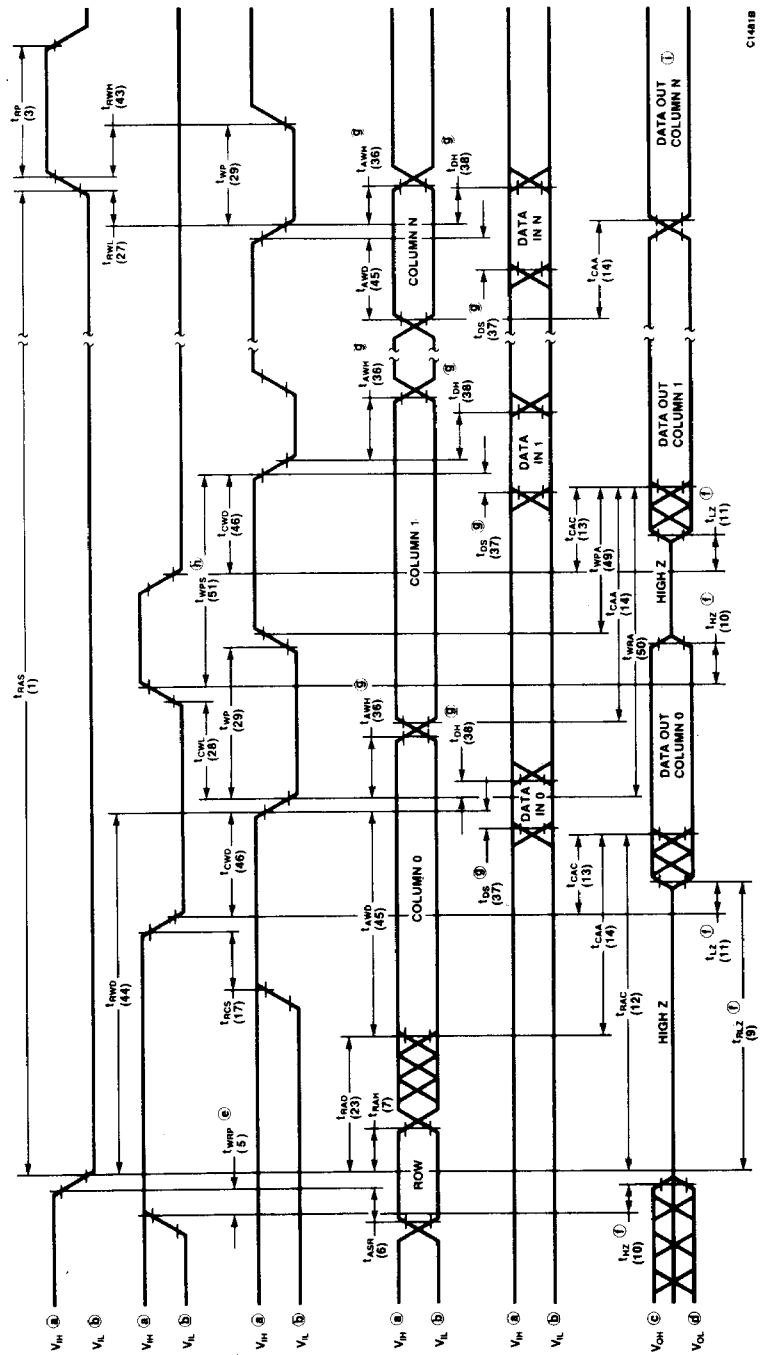
NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

WAVEFORMS (Cont.)
Static Column Mode Read/Modify/Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

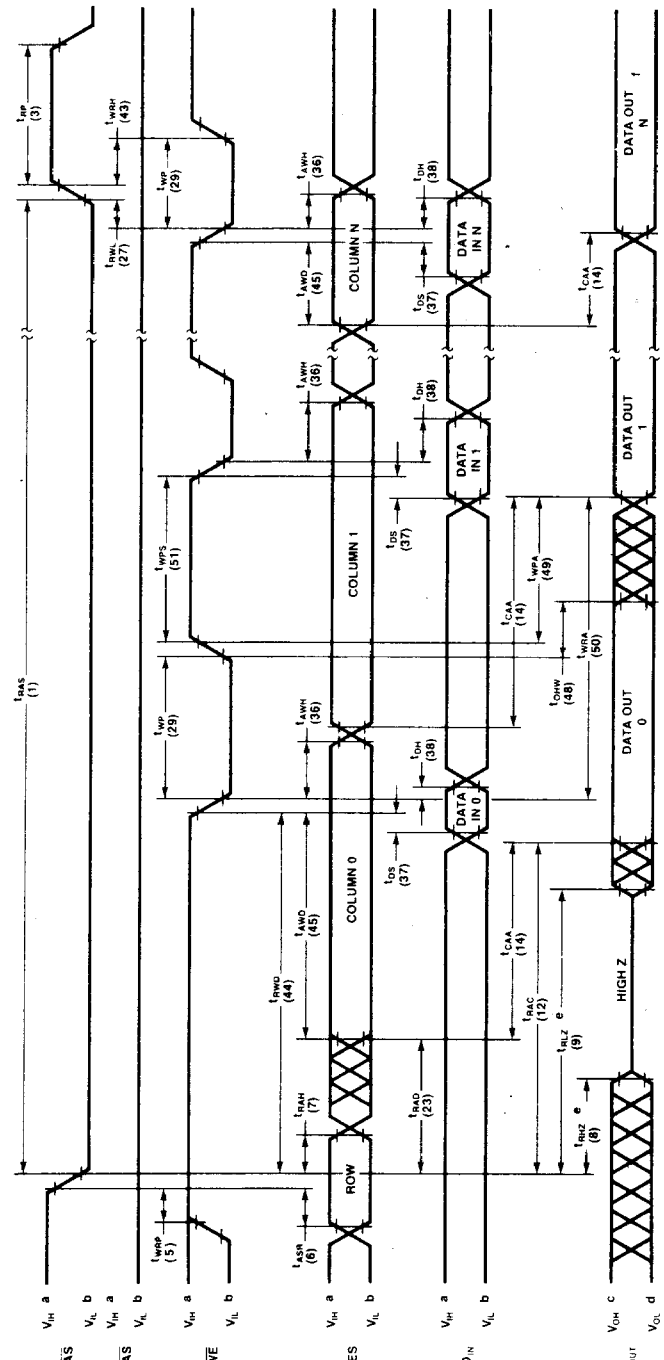
f. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$ low transition, whichever occurs last.

h. t_{WPS} (min) is measured from the earlier of $\overline{CAS}$ of $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{RWH} \geq t_{RWH}$ (min).

WAVEFORMS (Cont.)
Static Column Mode Read-Modify-Write Cycle ($\overline{CAS}$ Low)



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

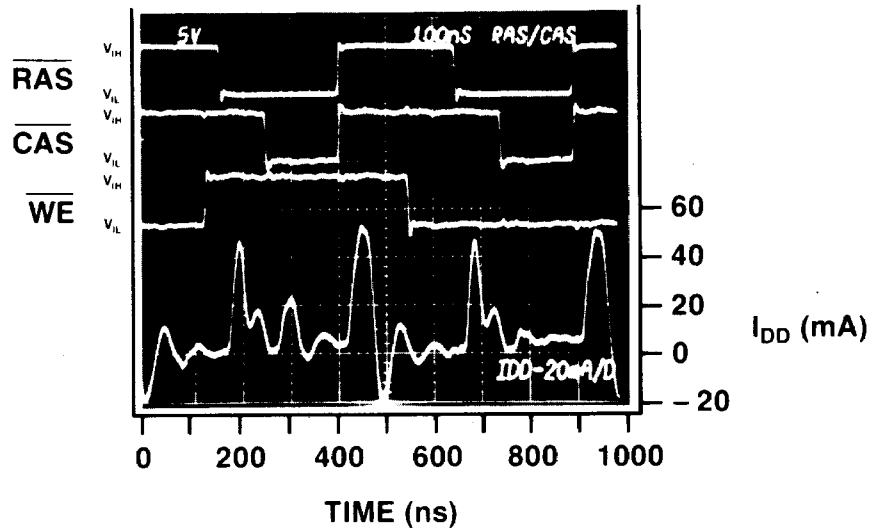
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

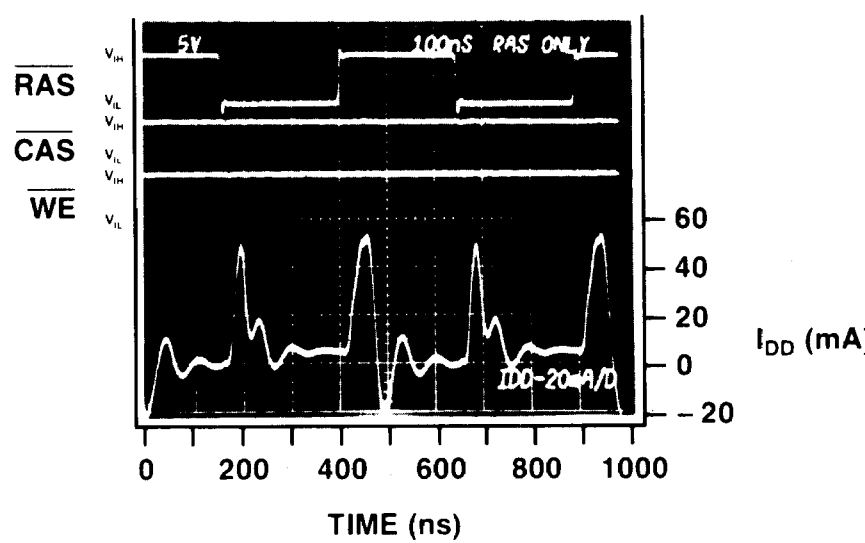
f. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{RWH} \geq t_{RWH}$ (min).

Typical power supply waveforms versus time are shown for the $\overline{RAS}/\overline{CAS}$ timings of the Read/Write and $\overline{RAS}$-only refresh cycles. I_{DD} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges are significantly reduced from typical high speed NMOS DRAMs.

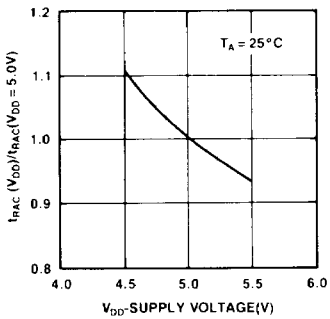
$\overline{RAS}/\overline{CAS}$



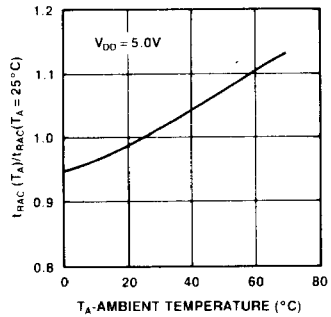
$\overline{RAS}$-ONLY REFRESH



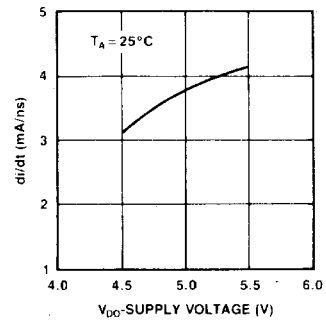
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



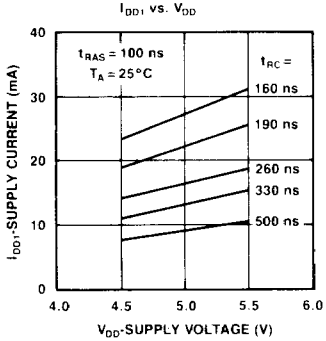
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC}(NORMALIZED) vs. T_A



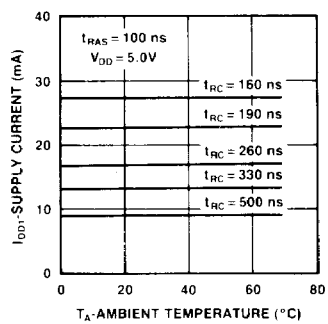
GRAPH 3
TYPICAL CURRENT TRANSIENTS
di/dt vs. V_{DD}



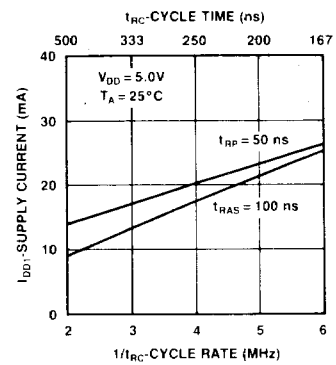
GRAPH 4
TYPICAL OPERATING CURRENT
I_{DD1} vs. V_{DD}



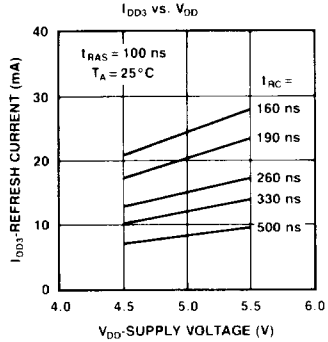
GRAPH 5
TYPICAL OPERATING CURRENT
I_{DD1} vs. T_A



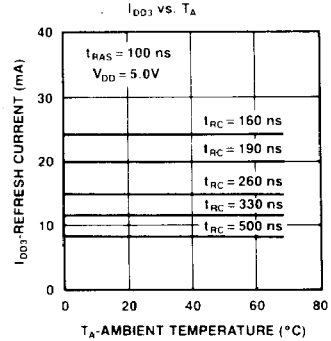
GRAPH 6
TYPICAL OPERATING CURRENT
I_{DD1} vs. $1/t_{RC}$



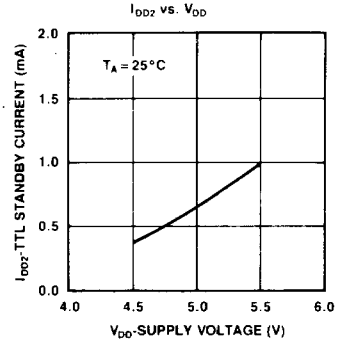
GRAPH 7
TYPICAL REFRESH CURRENT
I_{DD3} vs. V_{DD}



GRAPH 8
TYPICAL REFRESH CURRENT
I_{DD3} vs. T_A



GRAPH 9
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. V_{DD}



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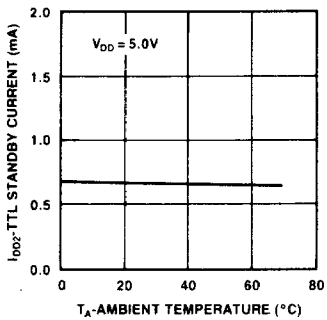
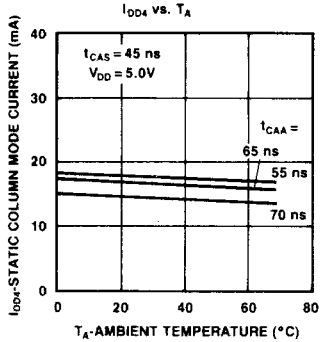
C14938-V

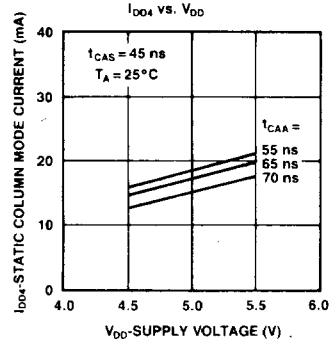
GRAPH 10
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. T_A



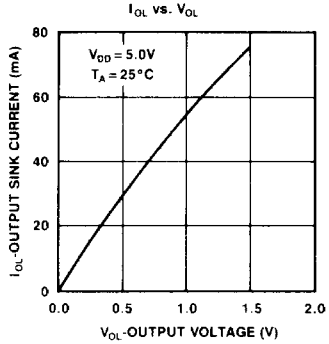
GRAPH 11
TYPICAL STATIC COLUMN MODE CURRENT
I_{DD4} vs. T_A



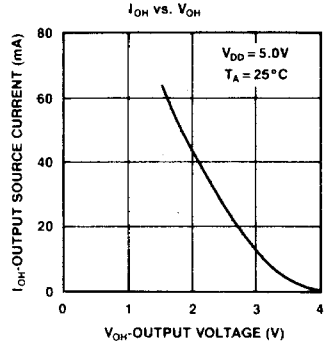
GRAPH 12
TYPICAL STATIC COLUMN MODE CURRENT
I_{DD4} vs. V_{DD}



GRAPH 13
TYPICAL OUTPUT SINK CURRENT
I_{OL} vs. V_{OL}



GRAPH 14
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} vs. V_{OH}



C1493B-V

FUNCTIONAL DESCRIPTION

The 51C65H is a CHMOS dynamic RAM optimized for high data bandwidth applications. The 51C65H functionality is similar to a traditional dynamic RAM operation. The 51C65H reads and writes data by multiplexing 16 address bits into 8 row and 8 column address bits. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address latch and access time is dependent upon a valid column address. The Column Address Strobe ($\overline{CAS}$) acts only as an output enable signal (active low) and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ active low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, has elasped. The output pin will always switch into the high impedance state when a memory cycle is initiated and remain in the high impedance state for a minimum period specified by t_{RLZ}. At that time, the output can change impedance states.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation.

For applications where $\overline{CAS}$ is held low, the ouput pin is always in a low impedance state except when the cycle is initiated. The data out becomes valid when t_{RAC} and t_{CAA} are both satisfied.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The output pin will remain in the high impedance state until both t_{RLZ} and t_{LZ} are satisfied. Data out becomes valid only when t_{CAC}, t_{CAA} and t_{RAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{CAC}, t_{CAA} and t_{RAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation. To simplify the system design, the column address is latched in by the later of $\overline{WE}$ or $\overline{CAS}$. As in the read cycle, $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation.

For applicatcns where $\overline{CAS}$ is held low, the input data must be valid at or before the falling edge of $\overline{WE}$. The output pin is always in a low impedance state except when the cycle is initiated.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge or $\overline{WE}$ of $\overline{CAS}$, whichever occurs last. In an early write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output pin will be in the high impedance state at the beginning of the write action. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh. $\overline{CAS}$ is not required.

Static Column Mode Operation

Static column mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write, and read-modify-write cycles can be performed during static column mode operation. The row address is internally retained by maintaining $\overline{RAS}$ active low. Following the entry cycle into static column mode operation, the data is accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address. Thus, the 51C65H operates like a static RAM for multiple accesses within the same row. $\overline{CAS}$ acts only as an output enable. Intel's Application Note #172 *CHMOS Drams in Graphics Applications,* provides more details on static column mode operation.

Data Out Operation

The 51C65H Data Output (D_{OUT}) is controlled primarily by $\overline{CAS}$ and secondarily by $\overline{RAS}$ and $\overline{WE}$. $\overline{CAS}$ acts only as an output enable. By bringing $\overline{CAS}$ high, the output switches to the high impedance state within the time specified by t_{HZ}. By taking $\overline{CAS}$ low, the output switches to a low impedance state after the time specified by t_{LZ}.

The output is not controlled by $\overline{CAS}$ during a memory cycle initialization. By bringing $\overline{RAS}$ low to initiate a memory cycle, the output automatically switches to the high impedance state within the time specified by t_{RHZ} and will remain in the high impedance state for a least the period specified by t_{RLZ}. In an early write cycle, when $\overline{WE}$ is asserted before $\overline{CAS}$, the output will remain in the high impedance state until the end

of write. The output will also remain in the high impedance state in a $\overline{CAS}$-only cycle.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).

The V_{DD} current (I_{DD}) requirement of the 51C65H during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device will go into an active cycle and I_{DD} would show current transients similar to those shown for the $\overline{RAS}/\overline{CAS}$ timings. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example, a logic "0" may change to a logic "1". The average soft error rate (SER) of less than 10 FITs is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. The SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at $V_{DD} = 4.75V$, and $t_{cycle} = 1\mu s$. A thorium source of 1.6×10^5 $\alpha/cm^2/hr$ is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS,* and A.P. #172, *CHMOS DRAMS in Graphics Applications.*

51C65L
LOW POWER 64K X 1
CHMOS DYNAMIC RAM

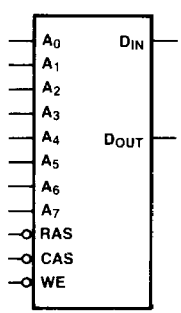
	51C65L-10	51C65L-12
Maximum Access Time (ns)	100	120
Maximum CHMOS Standby Current (mA)	0.05	0.05

- **Low Power Data Retention**
  - Standby current, CHMOS — 50μA (max.)
  - Refresh period, $\overline{RAS}$-Only — 64 ms (max.)
  - Data retention current — 80μA (max.)
- **Low Operating Current — 37 mA (max.)**
- **Low Input/Output Capacitance**
- **Fully TTL Compatible**
- **High Reliability Plastic — 16 Pin DIP**
- **Column Address Not Latched During Read Cycle.**

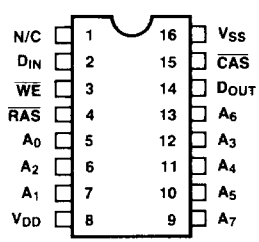
The Intel® 51C65L is a low power 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C65L offers features not provided by an NMOS dynamic RAM: CHMOS standby current and extended $\overline{RAS}$-Only refresh for low data retention power. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

The 51C65L offers a maximum standby current of 50 μA when $\overline{RAS} \geq V_{DD}$-0.5V. During standby (i.e. refresh only cycles), the refresh period can be extended to 64 ms to reduce the total current required for data retention to less than 80 μA (max.). The 51C65L combines low power with high density for portable and battery backup applications.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_7	ADDRESS INPUTS
D_{IN}	DATA IN
D_{OUT}	DATA OUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

June, 1984
Order Number: 280028-001

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . Plastic -55°C to +125°C
Voltage on Any Pin except V_{DD} and D_{OUT} Relative to V_{SS} . . . . . -2.0V to 7.5V
Voltage on D_{OUT} Relative to V_{SS} . . . . . -2.0V to V_{DD} + 1V
Voltage on V_{DD} Relative to V_{SS} . . . . . -1.0V to 7.5V
Data Out Current . . . . . 50 mA
Power Dissipation . . . . . 1.0 W

†COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°C$ to 70°C, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	51C65L Limits			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
$I_{DD\,1}$	V_{DD} Supply Current, Operating		27	37	mA	$t_{RC} = t_{RC}$ (min), for -10 A.C. spec	3,4
			23	35	mA	$t_{RC} = t_{RC}$ (min), for -12 A.C. spec.	
$I_{DD\,2}$	V_{DD} Supply Current, TTL Standby		0.7	2	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and output $\geq V_{SS}$	
$I_{DD\,3}$	V_{DD} Supply Current $\overline{RAS}$-Only Cycle		24	37	mA	$t_{RC} = t_{RC}$ (min), for -10 A.C. spec	3,4
			20	35	mA	$t_{RC} = t_{RC}$ (min), for -12 A.C. spec	
$I_{DD\,5}$	V_{DD} Supply Current Standby, Output Enabled		3	4	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and output $\geq V_{SS}$	3
$I_{DD\,6}$	V_{DD} Supply Current CHMOS Standby		0.008	0.05	mA	$\overline{RAS} \geq V_{DD} - 0.5V$, $\overline{CAS}$ at V_{IH}, all other inputs and output $\geq V_{SS}$	
$\|I_{LI}\|$	Input Load Current (any input)			1	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			1	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	-1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		7.0	V		5
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.2$ mA	6
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -5$ mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are to $T_A = 25°C$ and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL}(min) $\geq V_{SS}$ and V_{IH}(max) $\leq V_{DD}$.
6. Test conditions apply only for D.C. characteristics. A.C. parameters specified with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, Data In	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	Data Out	4	6	pF

†NOTE:
Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS 1, 2, 3

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $v_{SS} = 0V$, unless otherwise noted.

Read, Refresh and Write Cycles

#	JEDEC Symbol	Symbol	Parameter	51C65L-10		51C65L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}*	$\overline{CAS}$ Hold Time	100		120		ns	
5	t_{WH2RL2}	t_{WRP}	Write to $\overline{RAS}$ Precharge Time	−5		−5		ns	
6	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
7	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		ns	
8	t_{RL1QZ}	t_{RHZ}	$\overline{RAS}$ to Output High Impedance		15		15	ns	4
9	t_{RL1QX}	t_{RLZ}	$\overline{RAS}$ to Output Low Impedance	30		30		ns	4
10	t_{CH2QZ}	t_{HZ}*	$\overline{CAS}$ to Output High Impedance	0	20	0	20	ns	4,5
11	t_{CL1QX}	t_{LZ}*	$\overline{CAS}$ to Output Low Impedance	0		0		ns	4,5
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4	ms	6
	t_{RVRV}	t_{REF2}	Time Between Refresh, $\overline{RAS}$-only Refresh		64		64	ms	6
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7

NOTES:
* This parameter not applicable if operated with $\overline{CAS}$ grounded.
1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).
3. A.C. characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
4. Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
5. At any given temperature and voltage combination, t_{HZ} (max) is less than t_{LZ} (min) from device to device.
6. The 51C65L extends the refresh period to 64 ms during $\overline{RAS}$-only refresh operation.
7. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	51C65L-10		51C65L-12		Unit	Notes
				Min.	Max.	Min.	Max.		
12	t_{RL1QV}	t_{RAC}	Access Time From $\overline{RAS}$		100		120	ns	8
13	t_{CL1QV}	t_{CAC}*	Access Time From $\overline{CAS}$		20		25	ns	
14	t_{AVQV}	t_{CAA}	Access Time From Column Address		55		65	ns	
15	t_{CL1CH1}	$t_{CAS(R)}$*	$\overline{CAS}$ Pulse Width (Read Cycle)	20		25		ns	
16	t_{CL1RH1}	$t_{RSH(R)}$*	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		ns	
17	t_{WH2CL2}	t_{RCS}*	Read Command Set-up Time	0		0		ns	
18	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	90		110		ns	
19	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	55		65		ns	
20	t_{CH2WX}	t_{RCH}*	Read Command Hold Time referenced to $\overline{CAS}$	0		0		ns	
21	t_{RH2WX}	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10		10		ns	
22	t_{RH2AX}	t_{ARH}	Column Address Hold Time referenced to $\overline{RAS}$	0		0		ns	
23	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	45	20	55	ns	9

Write Cycle

24	$t_{CL1CH1(W)}$	$t_{CAS(W)}$*	$\overline{CAS}$ Pulse Width (Write Cycle)	30		35		ns	
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$*	$\overline{RAS}$ Hold Time (Write Cycle)	35		40		ns	
26	t_{RL1WL2}	t_{WDR}	$\overline{RAS}$ to Write Command Delay Time	30		35		ns	
27	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
28	t_{WL1CH1}	t_{CWL}*	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
29	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	30		35		ns	
30	t_{WH2WL2}	t_{WCP}	Write Command Precharge Time	10		15		ns	
31	t_{WL1CL2}	t_{WCS}*	Write Command Set-up Time	0		0		ns	10
32	t_{CL1WH1}	t_{WCH}*	Write Command Hold Time	30		35		ns	
33	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	80		90		ns	
34	t_{AVWL2}	t_{AWS1}	Column Address to Write Command Set-up Time	5		5		ns	11
35	t_{AVWL2}	t_{AWS2}	Column Address to Write Command Set-up Time	55		65		ns	12
36	t_{WL1AX}	t_{AWH}	Column Address to Write Command Hold Time	15		20		ns	
37	t_{DVWL2}	t_{DS}	Data-In Set-up Time	0		0		ns	
38	t_{WL1DX}	t_{DH}	Data-In Hold Time	20		25		ns	
39	t_{WH2QX}	t_{OW}	Output Active From End of Write	0		0		ns	

NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

8. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If $t_{RAD} > t_{RAD}$ (max) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max).
9. t_{RAD} specified for reference only.
10. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.
11. t_{AWS1} is applicable for a $\overline{CAS}$ controlled write operation, i.e., the leading edge of $\overline{WE}$ is low prior to or coincident with a $\overline{CAS}$ low transition.
12. Under typical TTL conditions ($V_{IH} \geq 3V$) and low supply inductance, $t_{AWS2} = t_{AWS1}$. Otherwise, t_{AWS2} is applicable for a $\overline{WE}$ controlled write operation, i.e., the leading edge of $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write Cycle[13]

#	JEDEC Symbol	Symbol	Parameter	51C65L-10		51C65L-12		Unit	Notes
				Min.	Max	Min.	Max.		
40	$t_{RL2RL2(RMW)}$	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	195		230		ns	
41	$t_{RL1RH1(RMW)}$	t_{RRW}	RMW Cycle RAS Pulse Width	135	75000	160	75000	ns	
42	$t_{CL1CH1(RMW)}$	t_{CRW}*	RMW Cycle $\overline{CAS}$ Pulse Width	55		65		ns	
43	t_{RH2WH1}	t_{RWH}	$\overline{RAS}$ to $\overline{WE}$ Hold Time	5		5		ns	
44	t_{RL2WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		ns	14
45	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	55		65		ns	14
46	t_{CL1WL2}	t_{CWD}*	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		ns	14

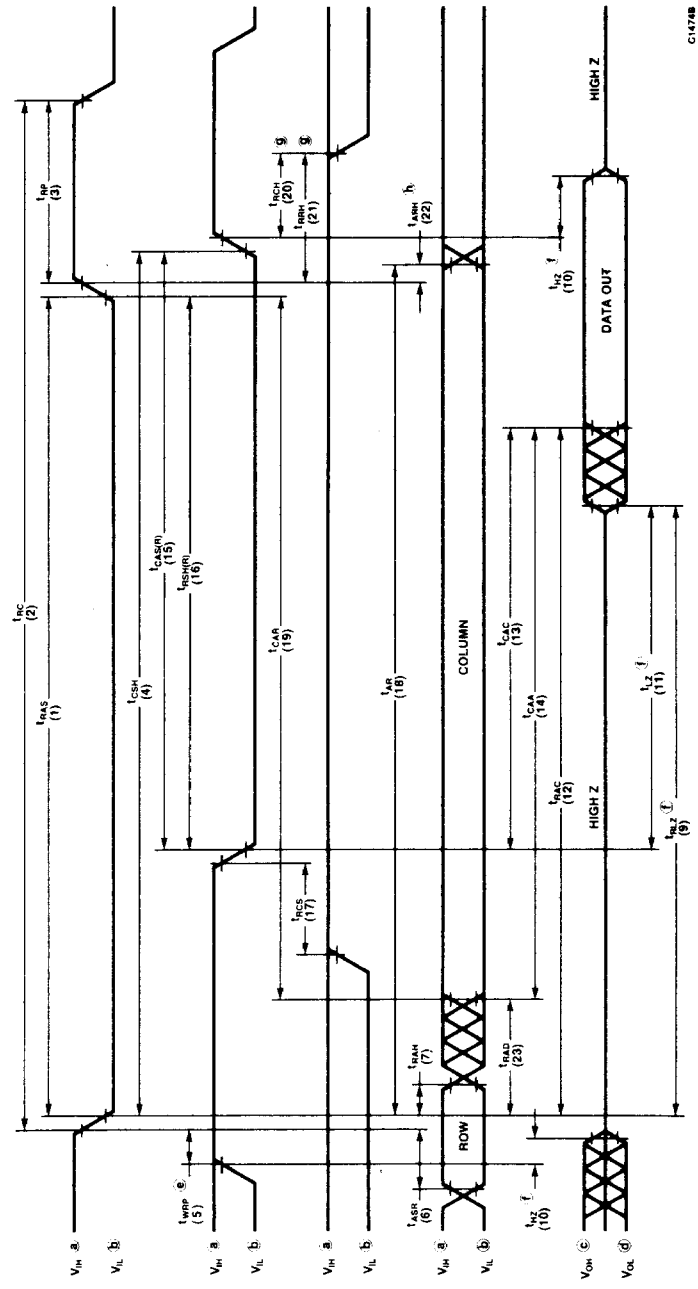
NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

13. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.

14. t_{WCS}, t_{RWD}, t_{WCD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data pin will remain high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.

WAVEFORMS
Read Cycle



NOTES:

a.,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c.,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

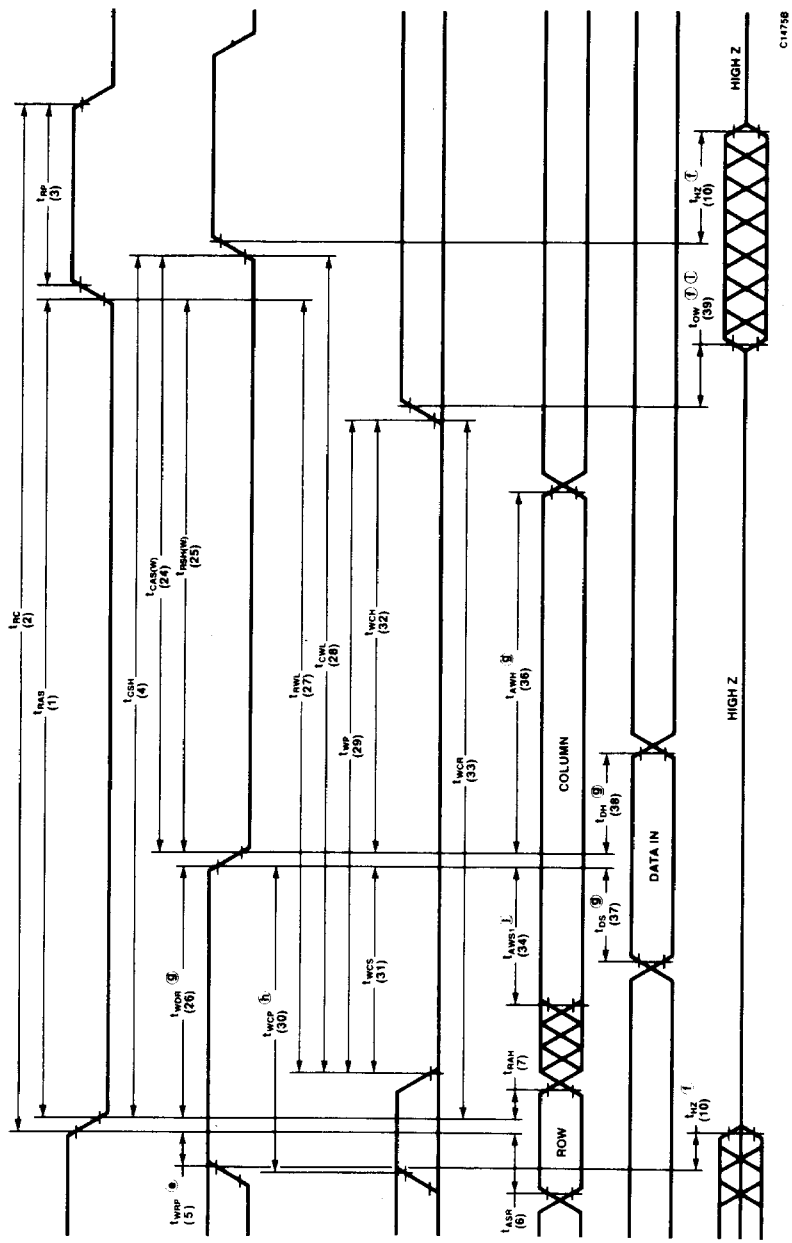
e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. Either t_{RCH} or t_{RRH} must be satisfied.

h. If $t_{ARH} \geq t_{ARH}$ (min), then data from the last address will be latched on D_{OUT}, as long as D_{OUT} is held in low impedance by $\overline{CAS}$.

WAVEFORMS (Cont.)
Write Cycle



NOTES:

a,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

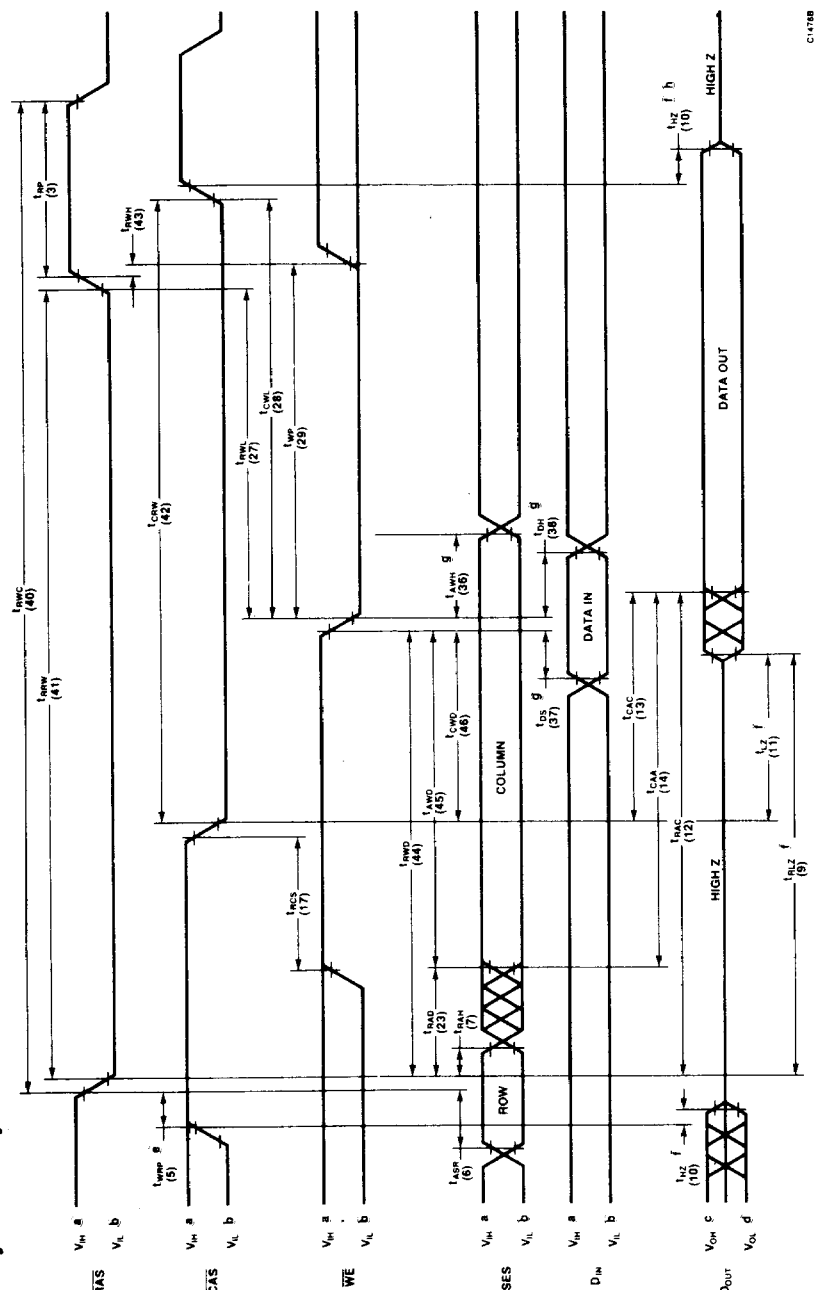
g. t_{AWH}, t_{DS}, t_{DH} and t_{WDR} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.

h. t_{WCP} (min) is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. If $\overline{CAS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance.

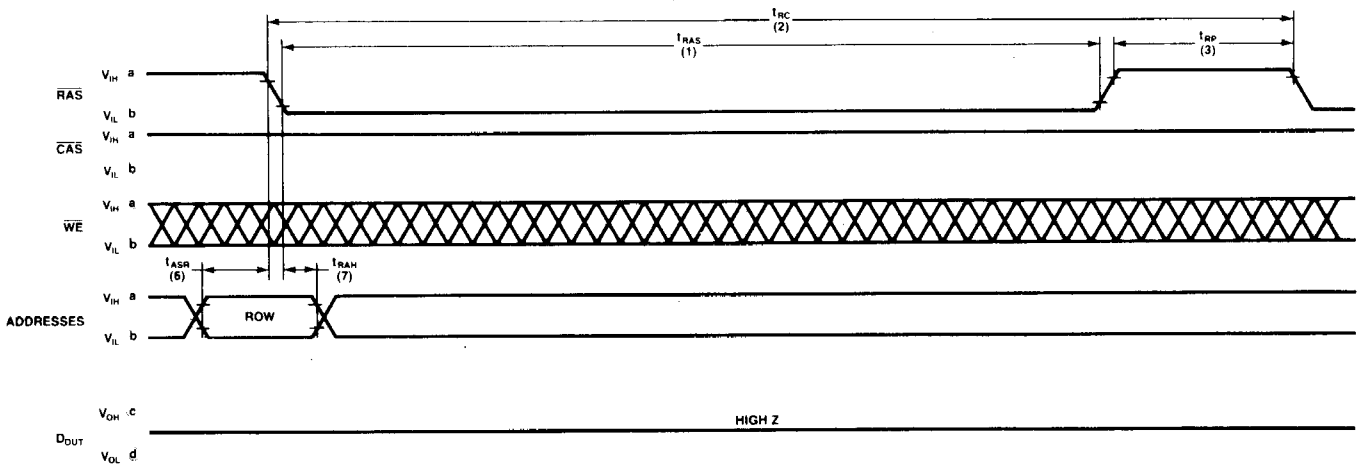
j. If a $\overline{WE}$ low transition occurs after a $\overline{CAS}$ low transition, t_{AWS2} is applicable.

WAVEFORMS (Cont.)
Read/Modify/Write Cycle



NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CAS}$ of $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three state load (5pF and a 380 Ohm Thevenin equivalent).
g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.
h. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{RWH} \geq t_{AWH}$ (min).

WAVEFORMS (Cont.)
$\overline{RAS}$-Only Refresh Cycle

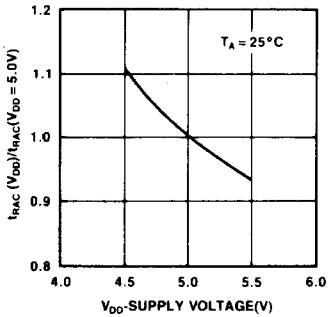


NOTES:

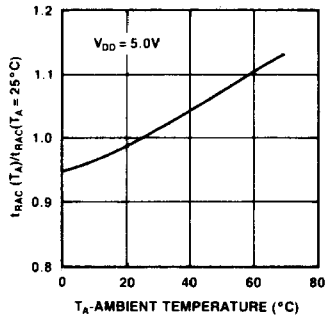
a.,b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c.,d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}

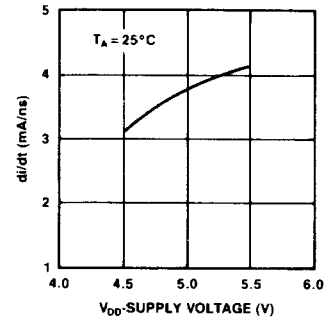
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



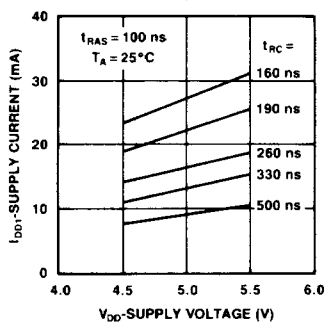
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC}(NORMALIZED) vs. T_A



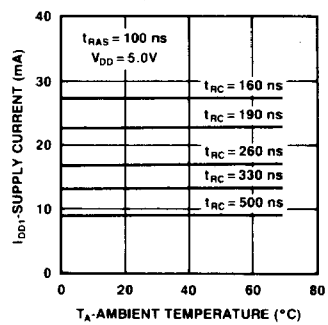
GRAPH 3
TYPICAL CURRENT TRANSIENTS
di/dt vs. V_{DD}



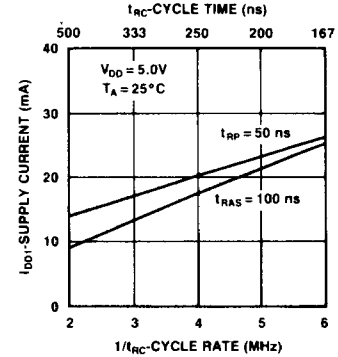
GRAPH 4
TYPICAL OPERATING CURRENT
I_{DD1} vs. V_{DD}



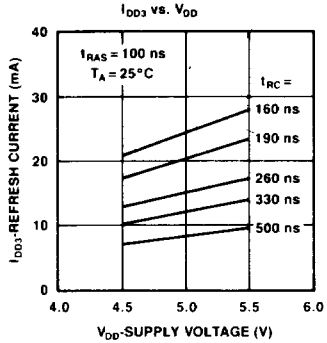
GRAPH 5
TYPICAL OPERATING CURRENT
I_{DD1} vs. T_A



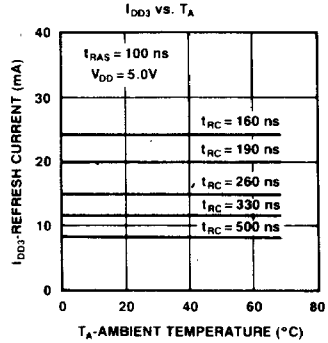
GRAPH 6
TYPICAL OPERATING CURRENT
I_{DD1} vs. $1/t_{RC}$



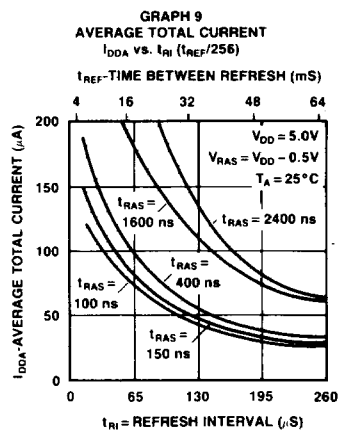
GRAPH 7
TYPICAL REFRESH CURRENT
I_{DD3} vs. V_{DD}



GRAPH 8
TYPICAL REFRESH CURRENT
I_{DD3} vs. T_A



GRAPH 9
AVERAGE TOTAL CURRENT
I_{DDA} vs. t_{RI} (t_{REF}/256)



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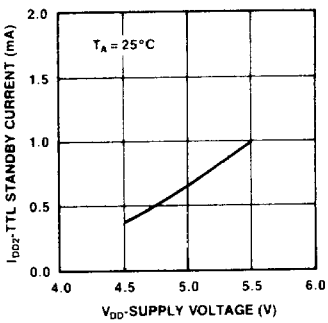
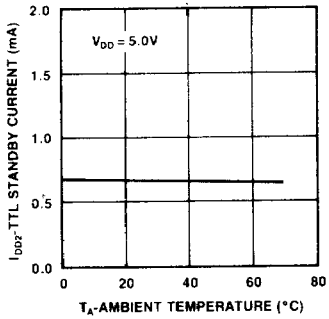
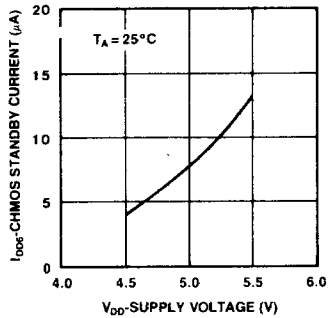
GRAPH 10
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. V_{DD}



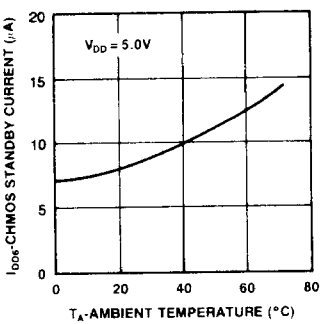
GRAPH 11
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. T_A



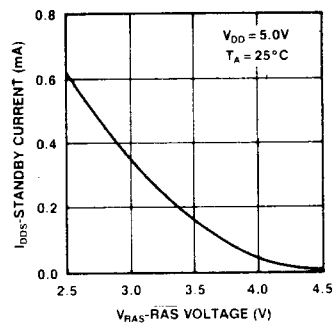
GRAPH 12
TYPICAL CHMOS STANDBY CURRENT
I_{DD6} vs. V_{DD}



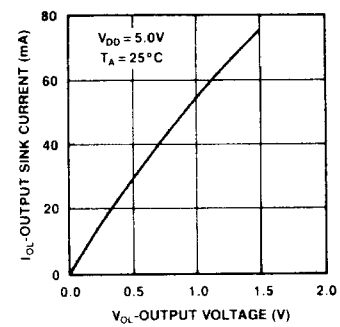
GRAPH 13
TYPICAL CHMOS STANDBY CURRENT
I_{DD6} vs. T_A



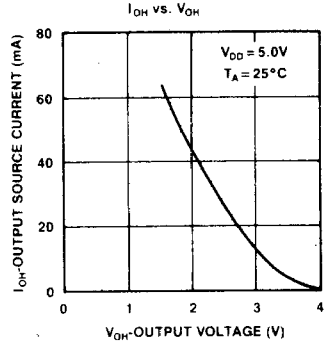
GRAPH 14
AVERAGE STANDBY CURRENT
RELATIVE TO $\overline{RAS}$ VOLTAGE
I_{DDS} vs. V_{RAS}



GRAPH 15
TYPICAL OUTPUT SINK CURRENT
I_{OL} vs. V_{OL}



GRAPH 16
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} vs. V_{OH}



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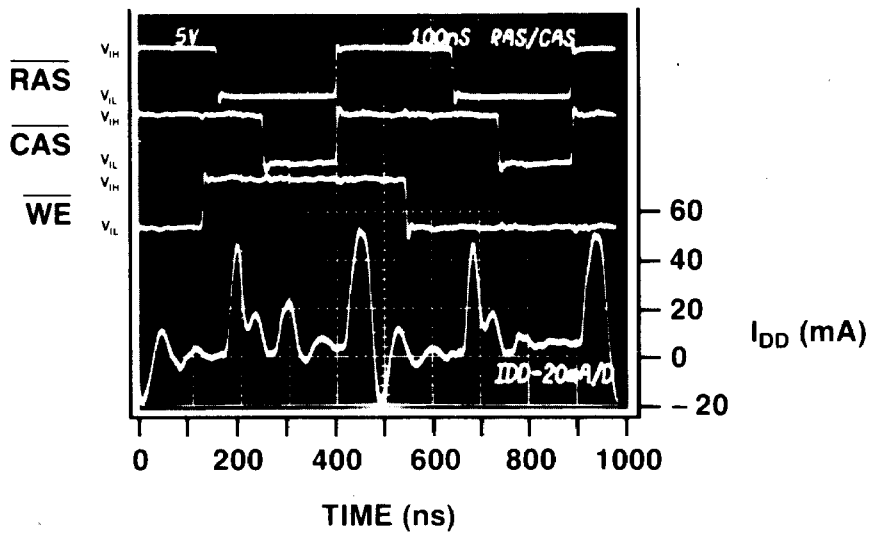
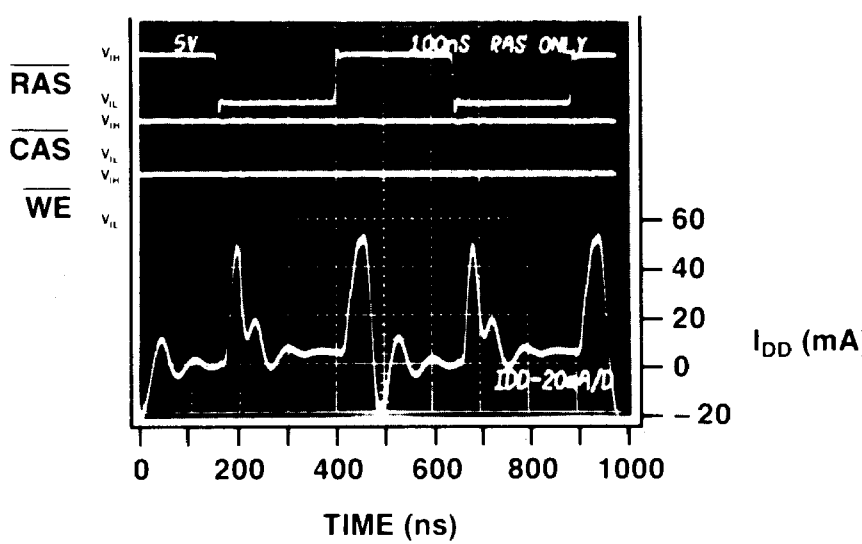
Typical power supply waveforms versus time are shown for the $\overline{RAS}/\overline{CAS}$ timings of the Read/Write and $\overline{RAS}$-only refresh cycles. I_{DD} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges are significantly reduced from typical high speed NMOS DRAMs.

$\overline{RAS}/\overline{CAS}$



$\overline{RAS}$-ONLY REFRESH



FUNCTIONAL DESCRIPTION

The 51C65L is a CHMOS dynamic RAM optimized for low power applications. The 51C65L functionality is similar to a traditional dynamic RAM operation. The 51C65L reads and writes data by multiplexing a 16 address bits into 8 row and an 8 column address bits. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address latch and access time is dependent upon a valid column address. The Column Address Strobe ($\overline{CAS}$) acts only as an output enable signal (active low) and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ active low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, has elapsed. The output pin will always switch into the high impedance state when a memory cycle is initiated and remain in the high impedance state for a minimum period specified by t_{RLZ}. At that time, the output can change impedance states.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation.

For applications where $\overline{CAS}$ is held low, the output pin is always in a low impedance state except when the cycle is initiated. The data out becomes valid when t_{RAC} and t_{CAA} are both satisfied.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The output pin will remain in the high impedance state until both t_{RLZ} and t_{LZ} are satisfied. Data out becomes valid only when t_{CAC} and t_{CAA} and t_{RAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{CAC}, t_{CAA} and t_{RAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation. To simplify the system design, the column address is latched in by the later of $\overline{WE}$ or $\overline{CAS}$. As in the read cycle, $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation.

For applications where $\overline{CAS}$ is held low, the input data must be valid at or before the falling edge of $\overline{WE}$. The output pin is always in a low impedance state except when the cycle is initiated.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In an early write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output pin will be in the high impedance state at the beginning of the write action. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh. $\overline{CAS}$ is not required.

Extended Refresh Cycle

The 51C65HL extends the refresh cycle period to 64 milliseconds for $\overline{RAS}$-only refresh cycles. This feature reduces the total current consumption to a maximum of 80 micro Amperes, and typically 15 micro Amperes, for data retention ($\overline{RAS} \geq V_{DD}$-0.5V, $\overline{RAS}$-only refresh operation for the 51C65L-12). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC}\ I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{t_{RI}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{REF}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Data Out Operation

The 51C65L Data Output (D_{OUT}) is controlled primarily by $\overline{CAS}$ and secondarily by $\overline{RAS}$ and $\overline{WE}$. $\overline{CAS}$ acts only as an output enable. By bringing $\overline{CAS}$ high, the output switches to the high impedance state within the time specified by t_{HZ}. By taking $\overline{CAS}$ low, the output switches to a low impedance state after the time specified by t_{LZ}.

The output is not controlled by $\overline{CAS}$ during a memory cycle initialization. By bringing $\overline{RAS}$ low to initiate a memory cycle, the output automatically switches to the high impedance state within the time specified by t_{RHZ} and will remain in the high impedance state for at least the period specified by t_{RLZ}. In an early write cycle, when $\overline{WE}$ is asserted before $\overline{CAS}$, the output will remain in the high impedance state until the end of write. The output will also remain in the high impedance state in $\overline{CAS}$-only cycle.

Power On

An initial pause of 100 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).

The V_{DD} current (I_{DD}) requirement of the 51C65L during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device will go into an active cycle and I_{DD} would show current transients similar to those shown for the $\overline{RAS}/\overline{CAS}$ timings. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example, a logic "0" may change to a logic "1". The average soft error rate (SER) of the 51C65L is less than 10 FITs. This is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. The SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at $V_{DD} = 4.75V$, and $t_{cycle} = 1\mu s$. A thorium source of 1.6×10^5 $\alpha/cm^2/hr$. is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS,* and A.P. #172, *CHMOS DRAMS in Graphics Applications.*

51C65HL
HIGH PERFORMANCE LOW POWER STATIC COLUMN 64K X 1 CHMOS DYNAMIC RAM

	51C65HL-10	51C65HL-12
Maximum Access Time (ns)	100	120
Maximum Column Address Access Time (ns)	55	65
Maximum CHMOS Standby Current (mA)	0.05	0.05

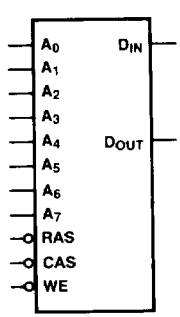
- **Static Column Mode Operation**
  - Continuous data rate over 15 MHz
  - Random access from address within row
  - t_{CAC} = 20, 25 ns
- **Low Input/Output Capacitance**
- **Fully TTL Compatible**
- **Low Power Data Retention**
  - Standby current, CHMOS — 50μA (max.)
  - Refresh period, $\overline{RAS}$-Only — 64 ms (max.)
  - Data Retention Current — 80μA (max.)
- **Low Operating Current — 37 mA (max.)**
- **High Reliability Plastic — 16 Pin DIP**

The Intel® 51C65HL is a high speed 65,536 x 1 dynamic Random Access Memory. Fabricated on Intel's CHMOS III-D technology, the 51C65HL offers features not provided by an NMOS dynamic RAM: Static Column Mode for high data bandwidth, fast usable speed, and CHMOS standby current and extended $\overline{RAS}$-Only refresh for low data retention current. All inputs and outputs are TTL compatible and the input and output capacitances are significantly lowered to allow increased system performance.

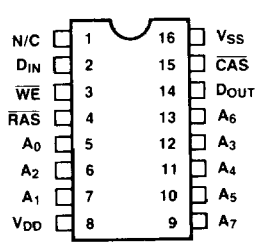
Static Column Mode operation allows random or sequential access of all 256 bits within a row simply by changing the column address. Because column address access time is as fast as 55 ns, a continuous data rate of over 15 million bits per second can be achieved. The 51C65HL offers high performance while relaxing many critical system timing requirements for fast usable speed. These features make the 51C65HL ideally suited for graphics, digital signal processing, and high performance systems.

The 51C65HL offers a maximum standby current of 50 μA when $\overline{RAS} \geq V_{DD}$-0.5V. During standby (i.e. refresh only cycles), the refresh period can be extended to 64 ms to reduce the total current required for data retention to less than 80 μA(max.). The 51C65HL combines this low power with high density for portable and battery backup applications.

LOGIC SYMBOL



PIN CONFIGURATION



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_7	ADDRESS INPUTS
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

June, 1984
Order Number: 280029-001

ABSOLUTE MAXIMUM RATINGS†

Ambient Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . Plastic -55°C to +125°C
Voltage on Any Pin except V_{DD} and D_{OUT} Relative to V_{SS} . . . . . -2.0V to 7.5V
Voltage on D_{OUT} Relative to V_{SS} . . . . . -2.0V to V_{DD} + 1V
Voltage on V_{DD} Relative to V_{SS} . . . . . -1.0V to 7.5V
Data Out Current . . . . . 50 mA
Power Dissipation . . . . . 1.0 W

†COMMENT:
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°C$ to 70°C, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	51C65HL Limits			Unit	Test Conditions	Notes
		Min.	Typ.[2]	Max.			
$I_{DD\,1}$	V_{DD} Supply Current, Operating		27	37	mA	$t_{RC} = t_{RC}$ (min), for −10 A.C. spec	3,4
			23	35	mA	$t_{RC} = t_{RC}$ (min), for −12 A.C. spec.	
$I_{DD\,2}$	V_{DD} Supply Current, TTL Standby		0.7	2	mA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, all other inputs and output $\geq V_{SS}$	
$I_{DD\,3}$	V_{DD} Supply Current, $\overline{RAS}$-Only Cycle		24	37	mA	$t_{RC} = t_{RC}$ (min), for −10 A.C. spec	3,4
			20	35	mA	$t_{RC} = t_{RC}$ (min), for −12 A.C. spec	
$I_{DD\,4}$	V_{DD} Supply Current, Static Column Mode		18	37	mA	Minimum Cycle for −10 A.C. spec	3,4
			17	35	mA	Minimum Cycle for −12 A.C. spec	
$I_{DD\,5}$	V_{DD} Supply Current, Standby, Output Enabled		3	4	mA	$\overline{RAS}$ at V_{IH}, $\overline{CAS}$ at V_{IL}, all other inputs and output $\geq V_{SS}$	3
$I_{DD\,6}$	V_{DD} Supply Current, CHMOS Standby		0.008	0.05	mA	$\overline{RAS} \geq V_{DD} - 0.5V$, $\overline{CAS}$ at V_{IH}, all other inputs and output $\geq V_{SS}$	
$\|I_{LI}\|$	Input Load Current (any input)			1	μA	$V_{IN} = V_{SS}$ to V_{DD}	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State			1	μA	$\overline{RAS}$ and $\overline{CAS}$ at V_{IH}, $D_{OUT} = V_{SS}$ to V_{DD}	
V_{IL}	Input Low Voltage (all inputs)	−1.0		0.8	V		5
V_{IH}	Input High Voltage (all inputs)	2.4		7.0	V		5
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.2$ mA	6
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -5$ mA	6

NOTES:
1. All voltages referenced to V_{SS}.
2. Typical values are to $T_A = 25°C$ and nominal supply voltages.
3. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max) is measured with the output open.
4. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max) is measured with a maximum of two transitions per address input per random cycle, one transition per access cycle in Static Column Mode.
5. Specified V_{IL} (min) is steady state operation. All A.C. parameters are measured with V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
6. Test conditions apply only for D.C. characteristics. A.C. parameters specified with a load equivalent to two TTL loads and 50 pF.

CAPACITANCE†

$T_A = 25°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, Data In	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	Data Out	4	6	pF

†NOTE:
Capacitance is measured at worst case voltage levels with a programmable capacitance meter.

A.C. CHARACTERISTICS [1, 2, 3]

$T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $v_{SS} = 0V$, unless otherwise noted.

Read, Refresh and Write Cycles

No.	JEDEC Symbol	Symbol	Parameter	51C65HL-10		51C65HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	100	75000	120	75000	ns	
2	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}*	$\overline{CAS}$ Hold Time	100		120		ns	
5	t_{WH2RL2}	t_{WRP}	Write to $\overline{RAS}$ Precharge Time	−5		−5		ns	
6	t_{AVRL2}	t_{ASR}	Row Address Set-up Time	0		0		ns	
7	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		ns	
8	t_{RL1QZ}	t_{RHZ}	$\overline{RAS}$ to Output High Impedance		15		15	ns	4
9	t_{RL1QX}	t_{RLZ}	$\overline{RAS}$ to Output Low Impedance	30		30		ns	4
10	t_{CH2QZ}	t_{HZ}*	$\overline{CAS}$ to Output High Impedance	0	20	0	20	ns	4,5
11	t_{CL1QX}	t_{LZ}*	$\overline{CAS}$ to Output Low Impedance	0		0		ns	4,5
	t_{RVRV}	t_{REF1}	Time Between Refresh		4		4	ms	6
	t_{RVRV}	t_{REF2}	Time Between Refresh, $\overline{RAS}$-only Refresh		64		64	ms	6
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7

NOTES:
* This parameter not applicable if operated with $\overline{CAS}$ grounded.
1. All voltages referenced to V_{SS}.
2. An initial pause of 100 microseconds is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).
3. A.C. characteristics assume $t_T = 5$ ns. All A.C. parameters are measured with a load equivalent to two TTL loads and 50 pF, V_{IL} (min) $\geq V_{SS}$ and V_{IH} (max) $\leq V_{DD}$.
4. Assumes three state test load (5 pF and a 380 Ohm Thevenin equivalent).
5. At any given temperature and voltage combination, t_{HZ} (max) is less than t_{LZ} (min) from device to device.
6. The 51C65HL extends the refresh period to 64 ms during $\overline{RAS}$-only refresh operation.
7. t_T is measured between V_{IH} (min) and V_{IL} (max).

A.C. CHARACTERISTICS (Con't.)

Read Cycle

No.	JEDEC Symbol	Symbol	Parameter	51C65HL-10		51C65HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
12	t_{RL1QV}	t_{RAC}	Access Time From $\overline{RAS}$		100		120	ns	8
13	t_{CL1QV}	t_{CAC}*	Access Time From $\overline{CAS}$		20		25	ns	
14	t_{AVQV}	t_{CAA}	Access Time From Column Address		55		65	ns	
15	t_{CL1CH1}	$t_{CAS(R)}$*	$\overline{CAS}$ Pulse Width (Read Cycle)	20		25		ns	
16	t_{CL1RH1}	$t_{RSH(R)}$*	$\overline{RAS}$ Hold Time (Read Cycle)	10		10		ns	
17	t_{WH2CL2}	t_{RCS}*	Read Command Set-up Time	0		0		ns	
18	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	90		110		ns	
19	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	55		65		ns	
20	t_{CH2WX}	t_{RCH}*	Read Command Hold Time referenced to $\overline{CAS}$	0		0		ns	
21	t_{RH2WX}	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10		10		ns	
22	t_{RH2AX}	t_{ARH}	Column Address Hold Time referenced to $\overline{RAS}$	0		0		ns	
23	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	45	20	55	ns	9

Write Cycle

24	$t_{CL1CH1(W)}$	$t_{CAS(W)}$*	$\overline{CAS}$ Pulse Width (Write Cycle)	30		35		ns	
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$*	$\overline{RAS}$ Hold Time (Write Cycle)	35		40		ns	
26	t_{RL1WL2}	t_{WDR}	$\overline{RAS}$ to Write Command Delay Time	30		35		ns	
27	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
28	t_{WL1CH1}	t_{CWL}*	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
29	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	30		35		ns	
30	t_{WH2WL2}	t_{WCP}	Write Command Precharge Time	10		15		ns	
31	t_{WL1CL2}	t_{WCS}*	Write Command Set-up Time	0		0		ns	10
32	t_{CL1WH1}	t_{WCH}*	Write Command Hold Time	30		35		ns	
33	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	80		90		ns	
34	t_{AVWL2}	t_{AWS1}	Column Address to Write Command Set-up Time	5		5		ns	11
35	t_{AVWL2}	t_{AWS2}	Column Address to Write Command Set-up Time	55		65		ns	12
36	t_{WL1AX}	t_{AWH}	Column Address to Write Command Hold Time	15		20		ns	
37	t_{DVWL2}	t_{DS}	Data-In Set-up Time	0		0		ns	
38	t_{WL1DX}	t_{DH}	Data-In Hold Time	20		25		ns	
39	t_{WH2QX}	t_{OW}	Output Active From End of Write	0		0		ns	

NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

8. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If $t_{RAD} > t_{RAD}$ (max) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max).
9. t_{RAD} specified for reference only.
10. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data out pin will remain high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min) the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of the data out is indeterminate.
11. t_{AWS1} is applicable for a $\overline{CAS}$ controlled write operation, i.e., the leading edge of $\overline{WE}$ is low prior to or coincident with a $\overline{CAS}$ low transition.
12. Under typical TTL conditions ($V_{IH} \geq 3V$) and low supply inductance, $t_{AWS2} = t_{AWS1}$. Otherwise, t_{AWS2} is applicable for a $\overline{WE}$ controlled write operation, i.e., the leading edge of $\overline{CAS}$ is low prior to a $\overline{WE}$ low transition.

A.C. CHARACTERISTICS (Con't.)

Read-Modify-Write Cycle[13]

#	JEDEC Symbol	Symbol	Parameter	51C65HL-10		51C65HL-12		Unit	Notes
				Min.	Max.	Min.	Max.		
40	$t_{RL2RL2\ (RMW)}$	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	195		230		ns	
41	$t_{RL1RH1\ (RMW)}$	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	135	75000	160	75000	ns	
42	$t_{CL1CH1\ (RMW)}$	t_{CRW}*	RMW Cycle $\overline{CAS}$ Pulse Width	55		65		ns	
43	t_{RH2WH1}	t_{RWH}	$\overline{RAS}$ to $\overline{WE}$ Hold Time	5		5		ns	
44	t_{RL2WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		ns	14
45	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	55		65		ns	14
46	t_{CL1WL2}	t_{CWD}*	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		ns	14

Static Column Mode[15]

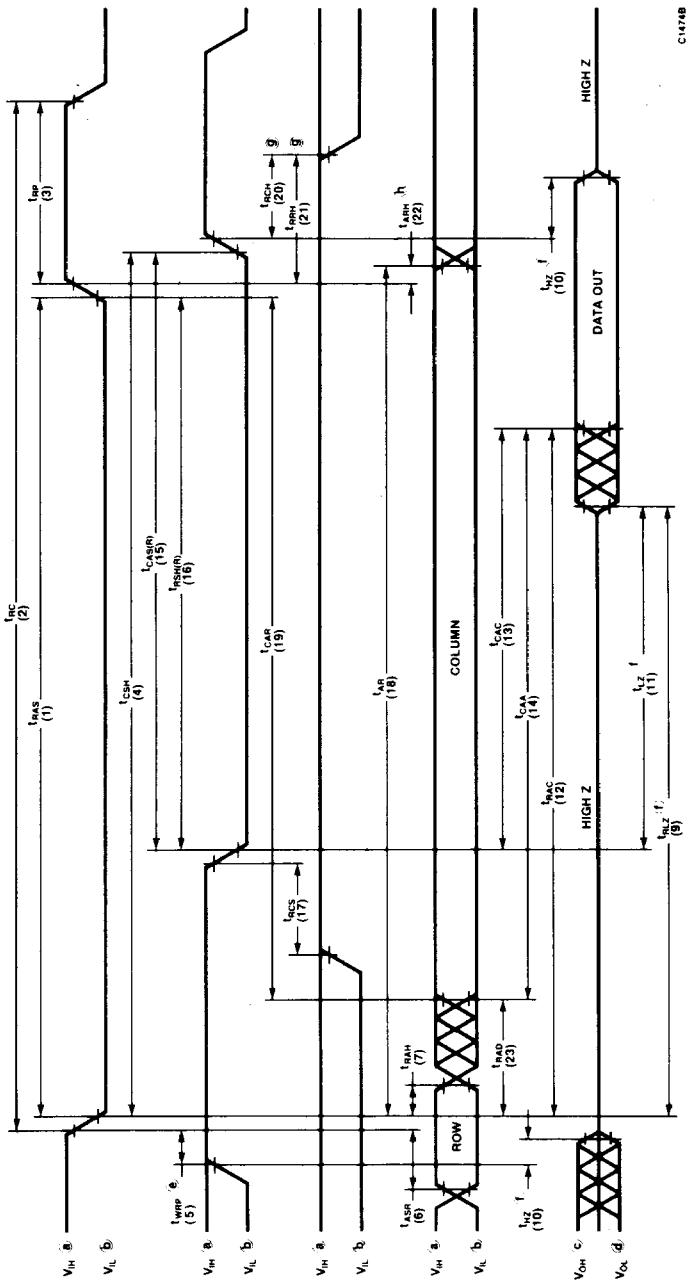
47	t_{AXQX}	t_{OHA}	Output Hold Time From Address Change	10		10		ns	
48	t_{WH2QX}	t_{OHW}	Output Hold Time From End of Write	0		0		ns	
49	t_{WH2QV}	t_{WPA}	RMW Write Precharge Access Time		70		80	ns	16
50	t_{WL1QV}	t_{WRA}	RMW Write-Read Access Time		105		120	ns	16
51	t_{WH2WL2}	t_{WPS}	RMW Write Command Precharge Time	55		65		ns	

NOTES:

* This parameter not applicable if operated with $\overline{CAS}$ grounded.

13. The parameters shown in the Read-Modify-Write timing diagrams which are not listed in the table are previously specified.
14. t_{WCS}, t_{RWD}, t_{WCD} and t_{AWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is a $\overline{CAS}$ controlled write cycle (early write cycle) and the data pin will remain high impedance for the duration of $\overline{WE}$ low. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain the data read from the selected address. If any of the above conditions are not satisfied, the condition of data out is indeterminate.
15. All previously specified A.C. characteristics are applicable.
16. Access time from a write command to a read command is determined by the longer of t_{CAA} or t_{WPA} or t_{WRA}.

WAVEFORMS
Read Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

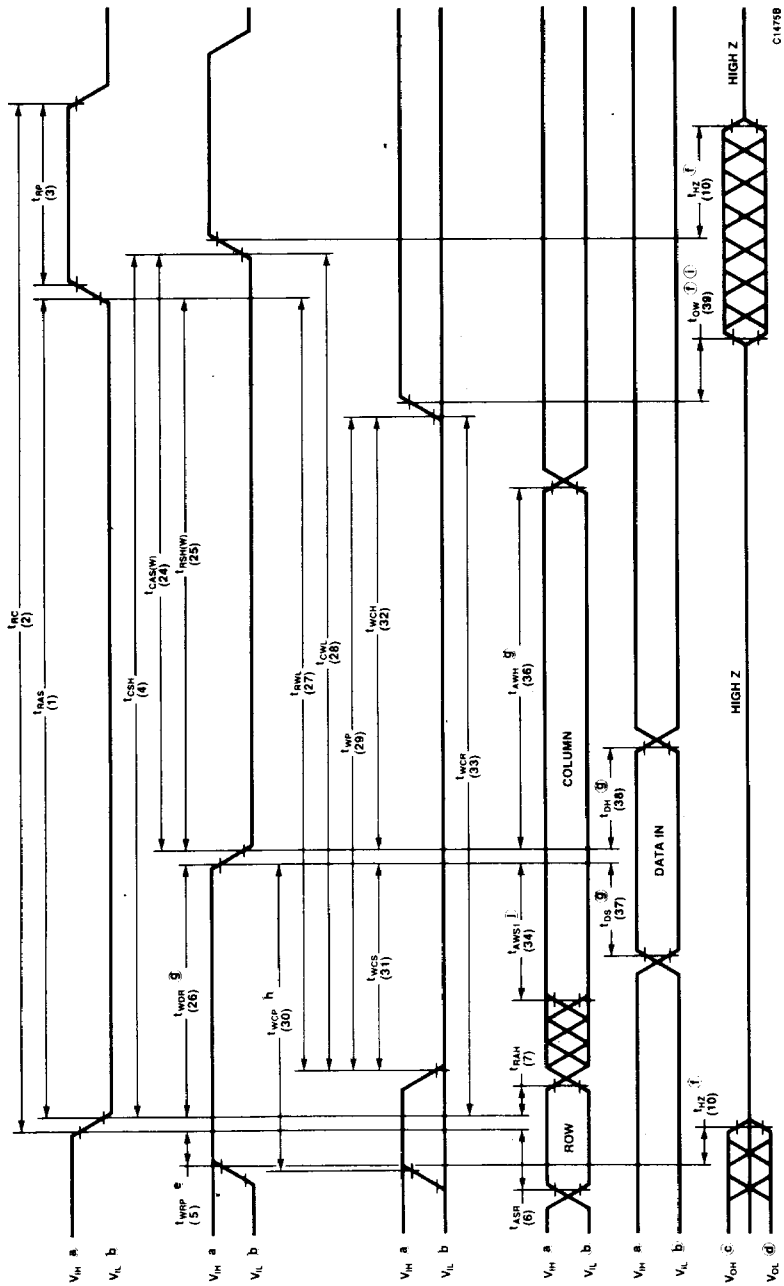
e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. Either t_{RCH} or t_{RRH} must be satisfied.

h. If $t_{ARH} \geq t_{ARH}$ (min), then data from the last address will be latched on D_{OUT}, as long as D_{OUT} is held in low impedance by $\overline{CAS}$.

WAVEFORMS (Cont.)
Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

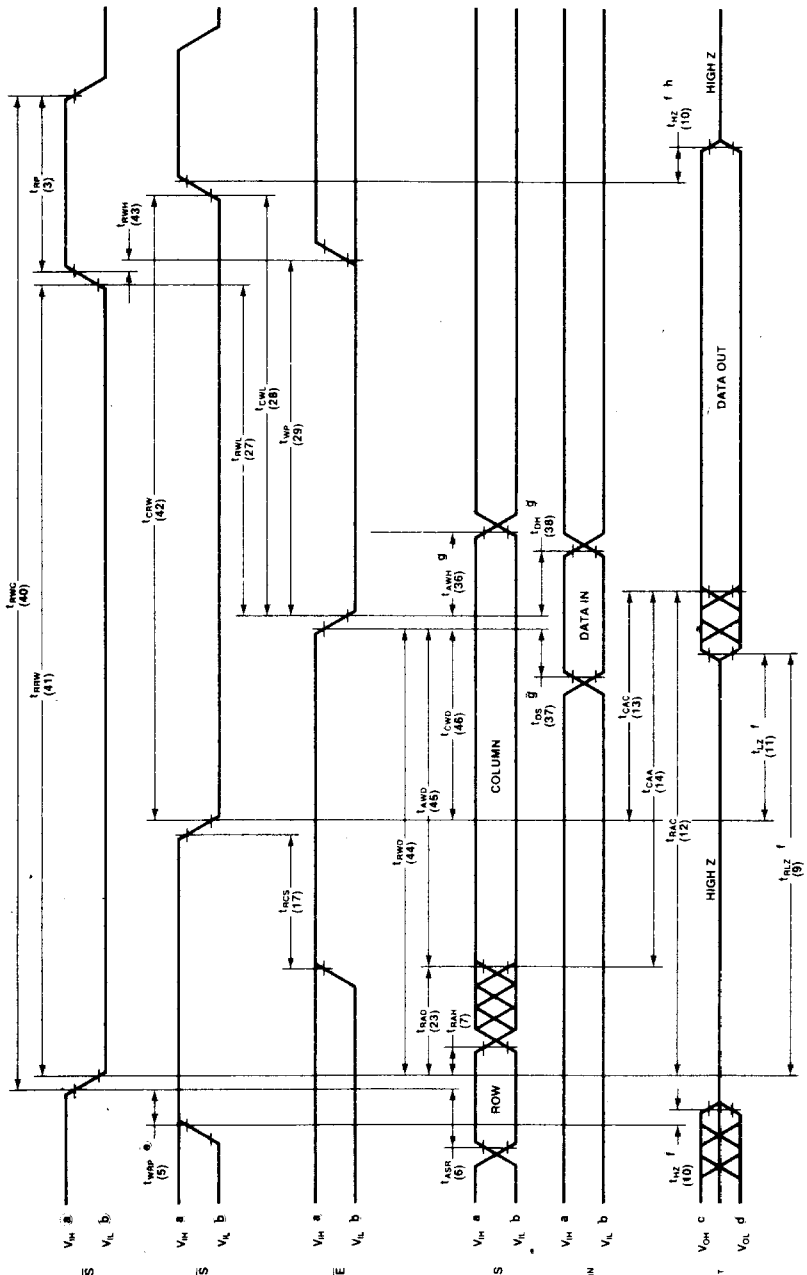
g. t_{AWH}, t_{DS}, t_{DH} and t_{WOR} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.

h. t_{WCP} (min) is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. If $\overline{CAS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance.

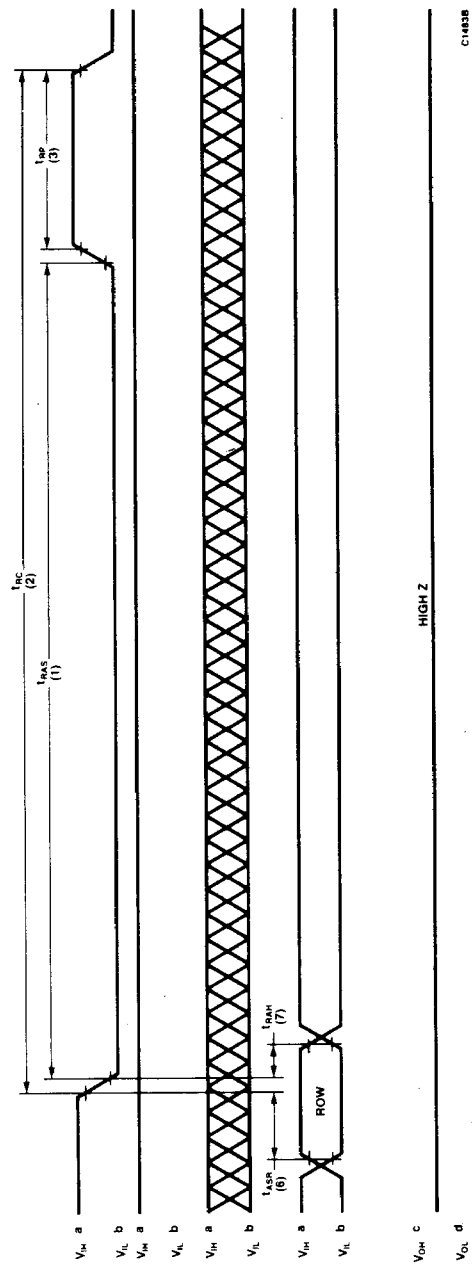
j. If a $\overline{WE}$ low transition occurs after a $\overline{CAS}$ low transition, t_{AWS2} is applicable.

WAVEFORMS (Cont.)
Read/Modify/Write Cycle



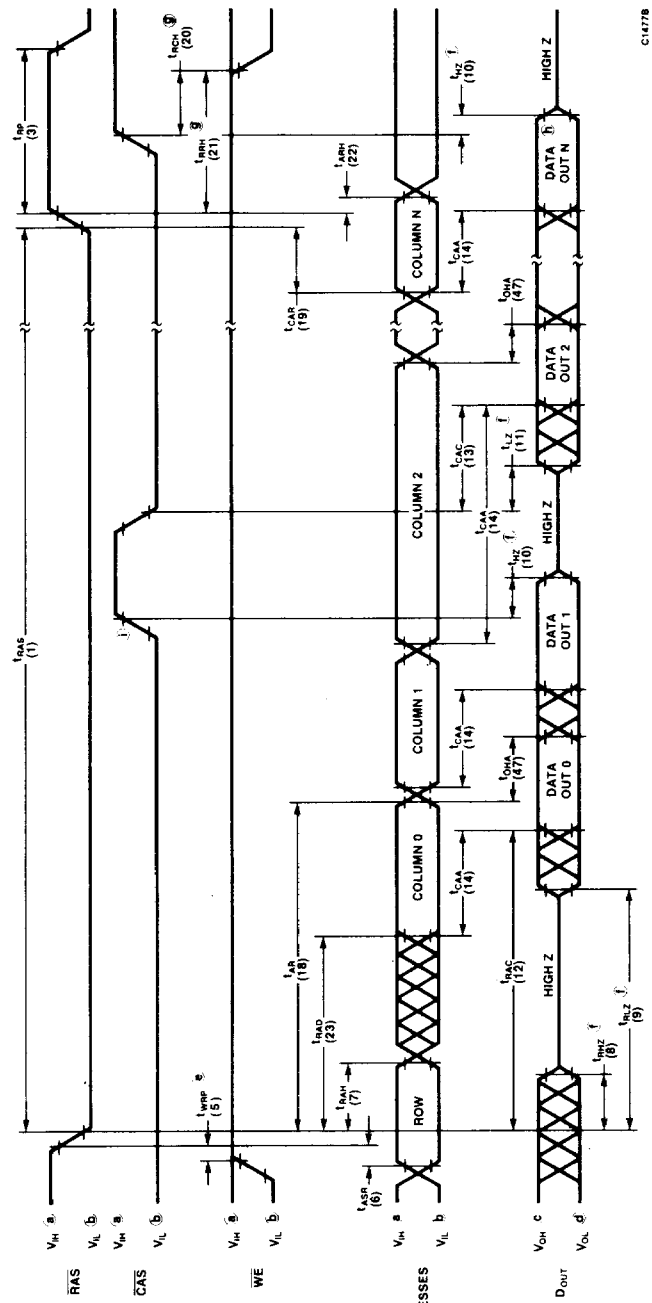
NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{WRP} is referenced to $\overline{CAS}$ of $\overline{WE}$ high transition, whichever occurs first.
f. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.
h. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{RWH} \geq t_{RWH}$ (min).

WAVEFORMS (Cont.)
RAS-Only Refresh Cycle



NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

WAVEFORMS (Cont.)
Static Column Mode Read Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

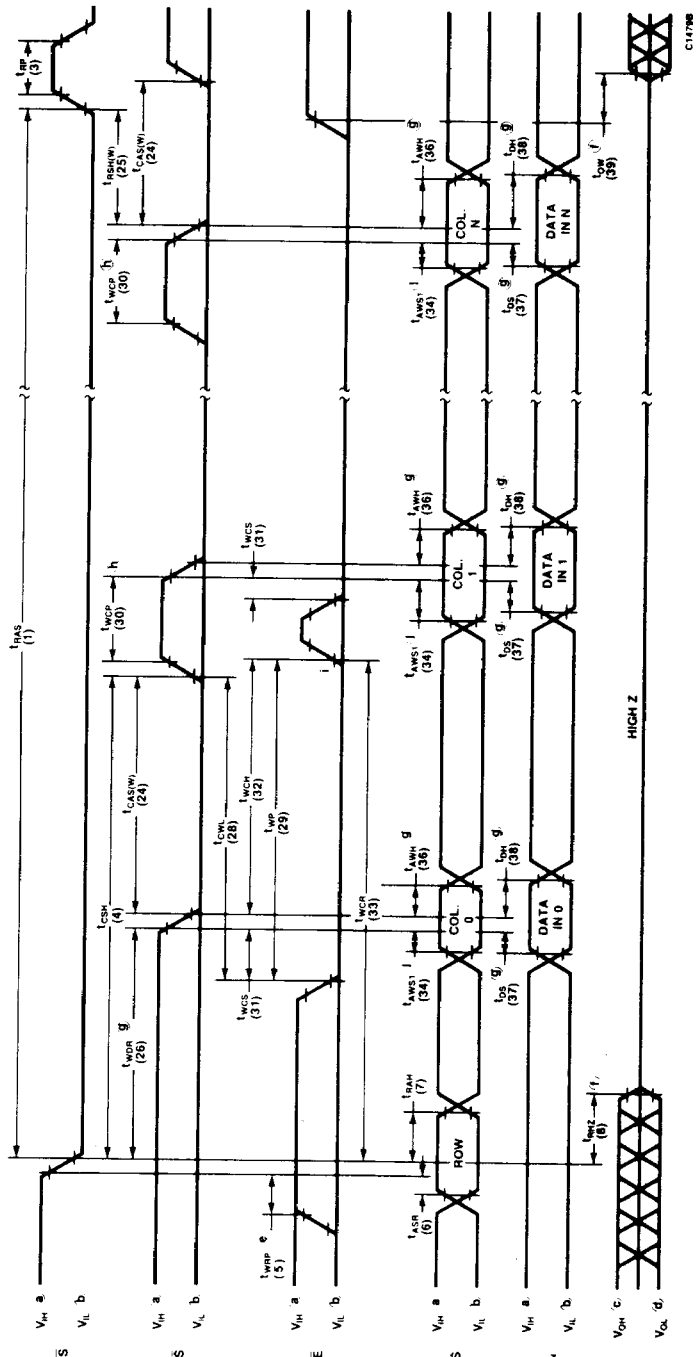
f. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. Either t_{RCH} or t_{RRH} must be satisfied.

h. D_{OUT} is valid as shown if and only if $t_{ARH} \geq t_{ARH}$ (min).

i. $\overline{CAS}$ pulse is shown for reference. In this case, D_{OUT} will go to high impedance.

WAVEFORMS (Cont.)
Static Column Mode Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

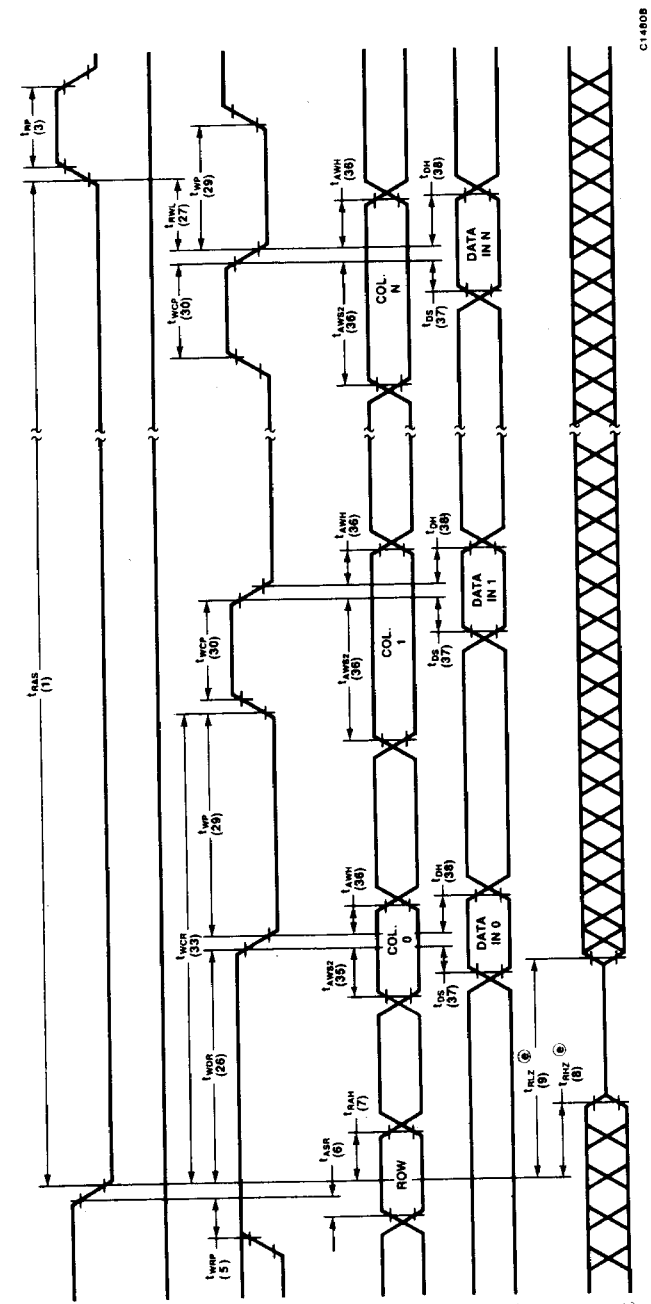
g. t_{AWH}, t_{DS}, t_{DH} and t_{WON} are referenced to $\overline{CAS}$ of $\overline{WE}$ low transition, whichever occurs last.

h. t_{WCP} (min) is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. If $\overline{CAS}$ and $\overline{WE}$ simultaneously make a high transition, the output will remain in high impedance.

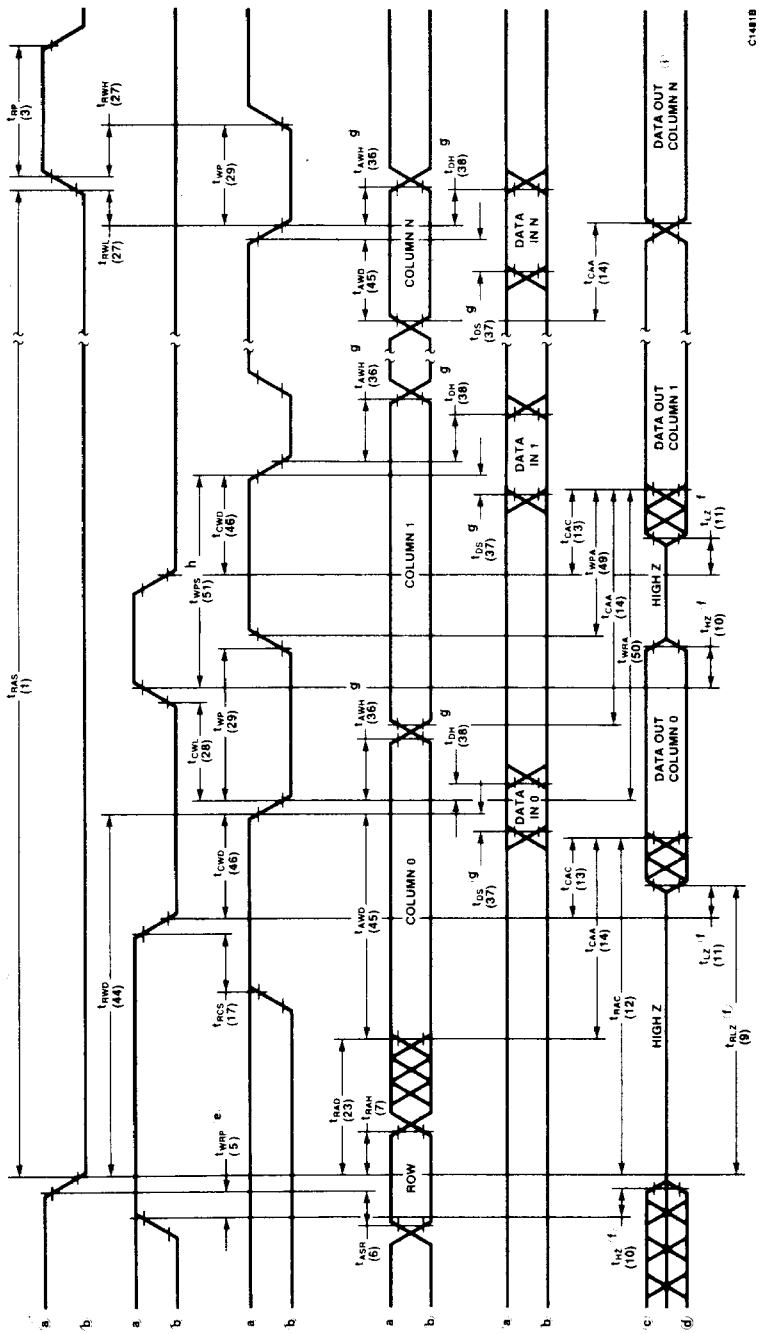
j. If a $\overline{WE}$ low transition occurs after a $\overline{CAS}$ low transition, t_{AWS2} is applicable.

WAVEFORMS (Cont.)
Static Column Mode Write Cycle ($\overline{CAS}$ Low)



NOTES:
a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

WAVEFORMS (Cont.)
Static Column Mode Read/Modify/Write Cycle



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. t_{WRP} is referenced to $\overline{CAS}$ or $\overline{WE}$ high transition, whichever occurs first.

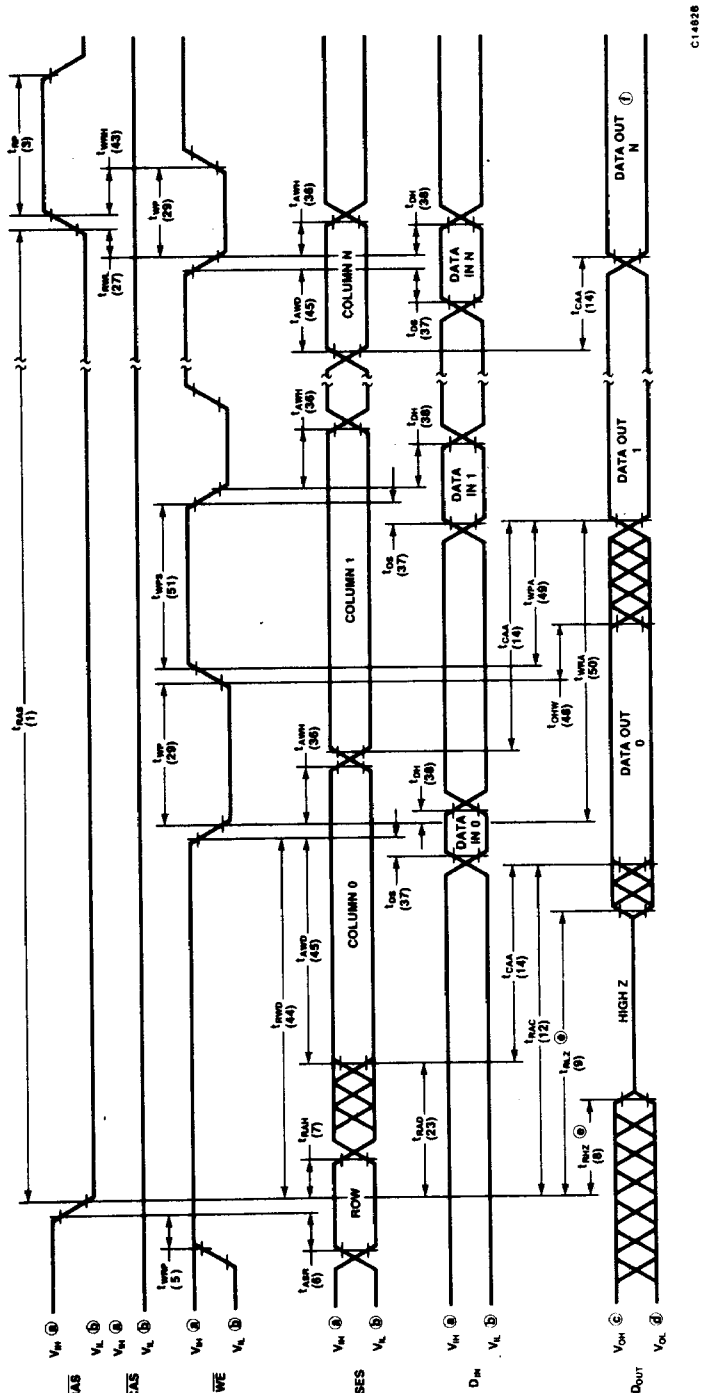
f. Transition is measured ± 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

g. t_{AWH}, t_{DS} and t_{DH} are referenced to $\overline{CAS}$ or $\overline{WE}$ low transition, whichever occurs last.

h. t_{WPS} (min) is measured from the earlier of $\overline{CAS}$ or $\overline{WE}$ high transition to the later of $\overline{CAS}$ or $\overline{WE}$ low transition.

i. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{AWH} \geq t_{RWH}$ (min).

WAVEFORMS (Cont.)
Static Column Mode Read-Modify-Write Cycle ($\overline{CAS}$ Low)



NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

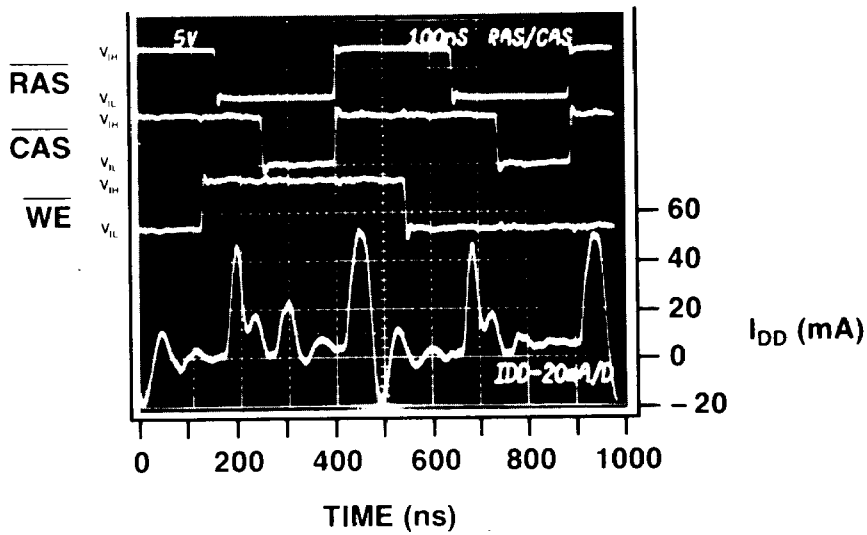
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

e. Transition is measured ±500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

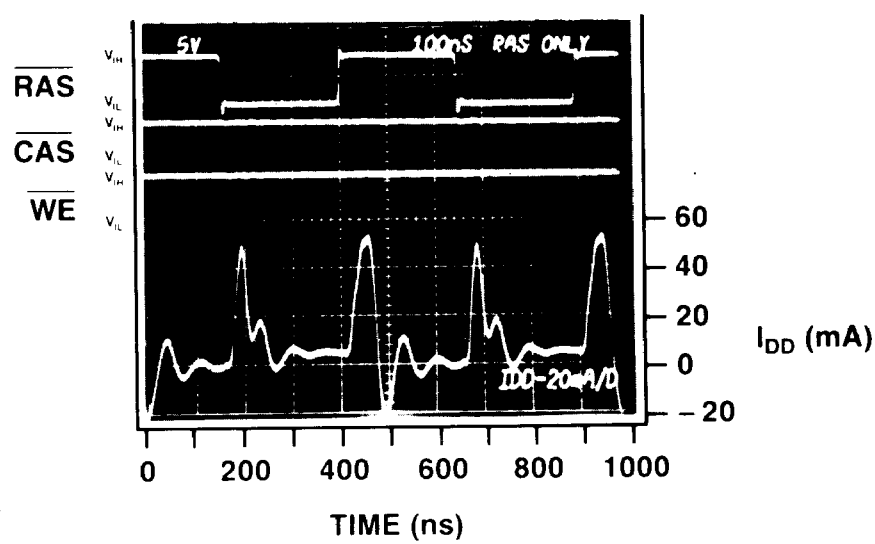
f. D_{OUT} is valid after $\overline{RAS}$ high transition, if and only if $t_{RWH} \geq t_{RWH}$ (min).

Typical power supply waveforms versus time are shown for the $\overline{RAS}/\overline{CAS}$ timings of the Read/Write and $\overline{RAS}$-only refresh cycles. I_{DD} current transients at the $\overline{RAS}$ and $\overline{CAS}$ edges are significantly reduced from typical high speed NMOS DRAMs.

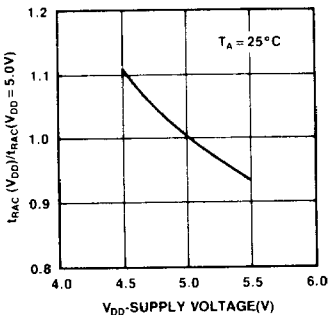
$\overline{RAS}/\overline{CAS}$



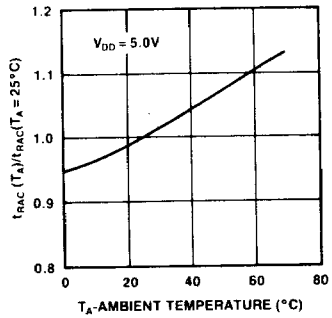
$\overline{RAS}$-ONLY REFRESH



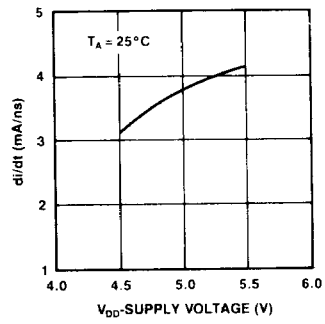
GRAPH 1
TYPICAL ACCESS TIME
t_{RAC} (NORMALIZED) vs. V_{DD}



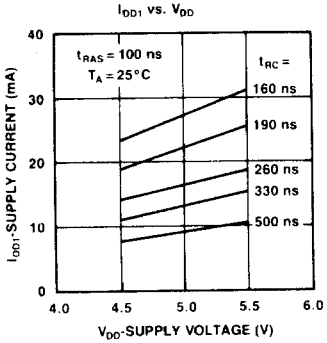
GRAPH 2
TYPICAL ACCESS TIME
t_{RAC}(NORMALIZED) vs. T_A



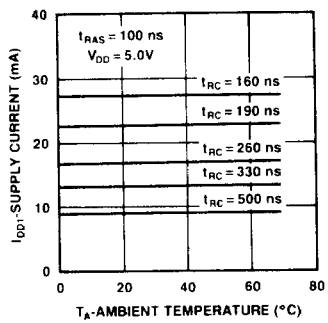
GRAPH 3
TYPICAL CURRENT TRANSIENTS
di/dt vs. V_{DD}



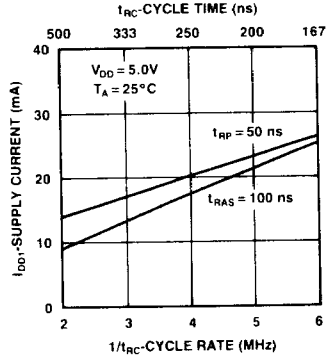
GRAPH 4
TYPICAL OPERATING CURRENT
I_{DD1} vs. V_{DD}



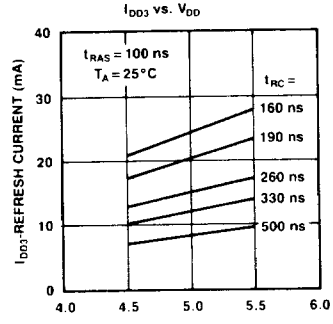
GRAPH 5
TYPICAL OPERATING CURRENT
I_{DD1} vs. T_A



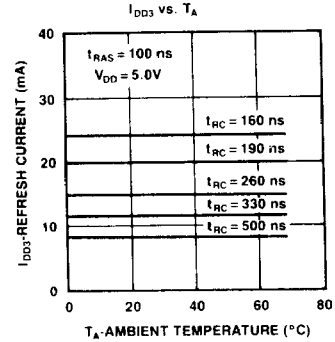
GRAPH 6
TYPICAL OPERATING CURRENT
I_{DD1} vs. 1/t_{RC}



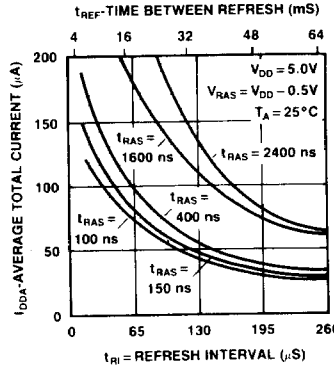
GRAPH 7
TYPICAL REFRESH CURRENT
I_{DD3} vs. V_{DD}



GRAPH 8
TYPICAL REFRESH CURRENT
I_{DD3} vs. T_A



GRAPH 9
AVERAGE TOTAL CURRENT
I_{DDA} vs. t_{RI} (t_{REF}/256)



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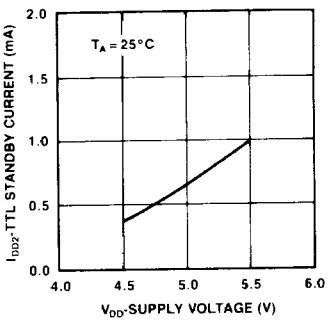
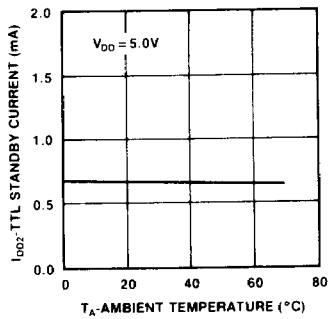
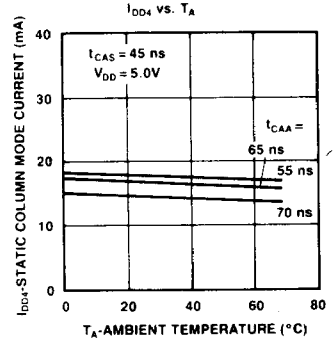
GRAPH 10
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. V_{DD}



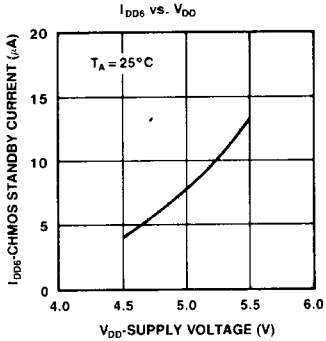
GRAPH 11
TYPICAL TTL STANDBY CURRENT
I_{DD2} vs. T_A



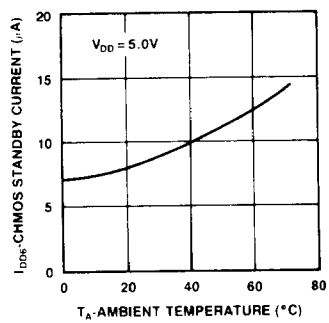
GRAPH 12
TYPICAL STATIC COLUMN MODE CURRENT
I_{DD4} vs. T_A



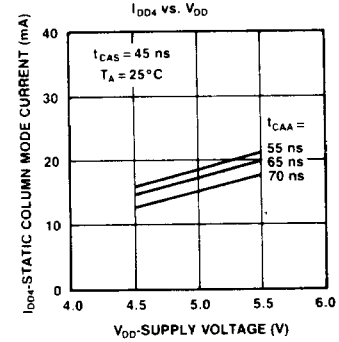
GRAPH 13
TYPICAL CHMOS STANDBY CURRENT
I_{DD6} vs. V_{DD}



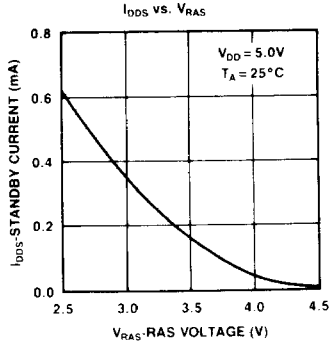
GRAPH 14
TYPICAL CHMOS STANDBY CURRENT
I_{DD6} vs. T_A



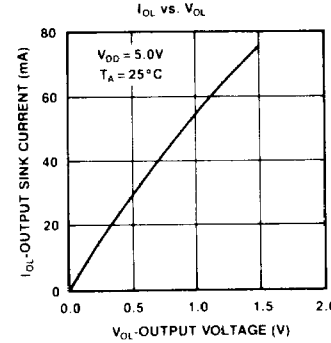
GRAPH 15
TYPICAL STATIC COLUMN MODE CURRENT
I_{DD4} vs. V_{DD}



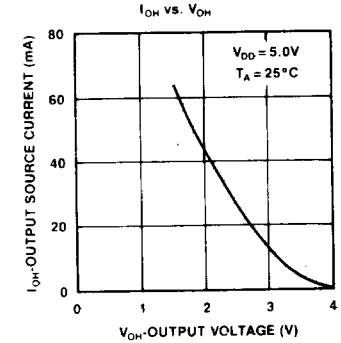
GRAPH 16
AVERAGE STANDBY CURRENT
RELATIVE TO $\overline{RAS}$ VOLTAGE
I_{DDS} vs. V_{RAS}



GRAPH 17
TYPICAL OUTPUT SINK CURRENT
I_{OL} vs. V_{OL}



GRAPH 18
TYPICAL OUTPUT SOURCE CURRENT
I_{OH} vs. V_{OH}



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FUNCTIONAL DESCRIPTION

The 51C65HL is a CHMOS dynamic RAM optimized for high data bandwidth and low power applications. The 51C65HL functionality is similar to a traditional dynamic RAM operation. The 51C65HL reads and writes data by multiplexing 16 address bits into 8 row and a 8 column address bits. The row address is latched in by the Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address latch and access time is dependent upon a valid column address. The Column Address Strobe ($\overline{CAS}$) acts only as an output enable signal (active low) and can remain low during the entire memory operation.

Memory Cycle

The memory cycle is initiated by bringing $\overline{RAS}$ active low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP} has elapsed. The output pin will always switch into the high impedance state when a memory cycle is initiated and remain in the high impedance state for a minimum period specified by t_{RLZ}. At that time, the output can change impedance states.

Read Cycle

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation.

For applications where $\overline{CAS}$ is held low, the output pin is always in a low impedance state except when the cycle is initiated. The data out becomes valid when t_{RAC} and t_{CAA} are both satisfied.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The output pin will remain in the high impedance state until both t_{RLZ} and t_{LZ} are satisfied. Data out becomes valid only when t_{CAC}, t_{CAA} and t_{RAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{CAC}, t_{CAA} and t_{RAC}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation. To simplify the system design, the column address is latched in by the later of $\overline{WE}$ or $\overline{CAS}$. As in the read cycle, $\overline{CAS}$ may either be held low or be pulsed similar to the traditional $\overline{CAS}$ operation.

For applications where $\overline{CAS}$ is held low, the input data must be valid at or before the falling edge of $\overline{WE}$. The output pin is always in a low impedance state except when the cycle is initiated.

For applications where $\overline{CAS}$ is pulsed similar to the traditional $\overline{CAS}$ operation, the additional timing specifications noted by the asterisks in the A.C. Characteristics are applicable. The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In an early write cycle (the leading edge of $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the output pin will be in the high impedance state at the beginning of the write action. Terminating the write action with $\overline{CAS}$ will maintain the output in the high impedance state; terminating with $\overline{WE}$ allows the output to go active.

Refresh Cycle

To retain data, a refresh operation is performed by clocking each of the 256 row addresses (A_0 through A_7) with RAS at least every 4 milliseconds. Any Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only cycle will perform refresh. $\overline{CAS}$ is not required.

Extended Refresh Cycle

The 51C65HL extends the refresh cycle period to 64 milliseconds for $\overline{RAS}$-only refresh cycles. This feature reduces the total current consumption to a maximum of 80 micro Amperes, and typically 15 micro Amperes, for data retention ($\overline{RAS} \geq V_{DD}$-0.5V, $\overline{RAS}$-only refresh operation for the 51C65HL-12). The low standby current can significantly extend battery life in battery back-up applications. Current consumption is calculated from the following equation:

$$I = \frac{(t_{RC}\ I_{ACTIVE}) + (t_{RI} - t_{RC})\ (I_{STANDBY})}{t_{RI}}$$

where t_{RC} = refresh cycle time,
and t_{RI} = refresh interval time or $t_{REF}/256$

Before entering or leaving an extended refresh period, the entire array must be refreshed at the normal interval of four milliseconds. This can be accomplished by either a burst or distributed refresh.

Static Column Mode Operation

Static column mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Read, write, and read-modify-write cycles can be performed during static column mode operation. The row address is internally retained by maintaining $\overline{RAS}$ active low. Following the entry cycle into static column mode operation, the data is accessed simply by changing the column address. Because the column address buffer acts as a transparent or flow-through latch, access begins from a valid column address. Thus, the 51C65HL operates like a static RAM for multiple accesses within the

same row. $\overline{CAS}$ acts only as an output enable. Intel's Application Note #172 *CHMOS DRAMS in Graphics Applications,* provides more details on static column mode operation.

Data Out Operation

The 51C65HL Data Output (D_{OUT}) is controlled primarily by $\overline{CAS}$ and secondarily by $\overline{RAS}$ and $\overline{WE}$. $\overline{CAS}$ acts only as an output enable. By bringing $\overline{CAS}$ high, the output switches to the high impedance state within the time specified by t_{HZ}. By taking $\overline{CAS}$ low, the output switches to a low impedance state after the time specified by t_{LZ}.

The output is not controlled by $\overline{CAS}$ during a memory cycle initialization. By bringing $\overline{RAS}$ low to initiate a memory cycle, the output automatically switches to the high impedance state within the time specified by t_{RHZ} and will remain in the high impedance state for at least the period specified by t_{RLZ}. In an early write cycle, when $\overline{WE}$ is asserted before $\overline{CAS}$, the output will remain in the high impedance state until the end of write. The output will also remain in the high impedance state in a $\overline{CAS}$-only cycle.

Power On

An initial pause of 100 μ is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 64 ms).

The V_{DD} current (I_{DD}) requirement of the 51C65HL during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ = V_{SS} during power on, the device will go into an active cycle and I_{DD} would show current transients similar to those shown for the $\overline{RAS}/\overline{CAS}$ timings. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

Soft Error Rate

Soft errors are random, non-recurring changes in memory logic states caused by the impact of an ionizing particle, such as an alpha particle. For example, a logic "0" may change to a logic "1". The average soft error rate (SER) of less than 10 FITs is determined by accelerated testing using an alpha particle source and is subsequently confirmed by system testing. The SER is a function of the operating voltage, cycle time, package, and the alpha particle source. Intel measures the SER at V_{DD} = 4.75V, and t_{cycle} = 1μs. A thorium source of 1.6×10^5 $\alpha/cm^2/hr$. is used because it best matches the package energy spectra.

References

For further details see Application Note (A.P.) #171, *Low Power with CHMOS DRAMS,* and A.P. #172, *CHMOS DRAMS in Graphics Applications.*