MIC59P50

8-Bit Parallel-Input Protected Latched Driver

General Description

The MIC59P50 parallel-input latched driver is a high-voltage (80V), high-current (500mA) integrated circuit comprised of eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Similar to the MIC5801, additional protection circuitry supplied on this device includes thermal shutdown, under voltage lockout (UVLO), and over-current shutdown.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The MIC59P50 has open-collector outputs capable of sinking 500mA and integral diodes for inductive load transient suppression with a minimum output breakdown voltage rating of 80V above V_{EE} (50V sustaining). The drivers can be operated with a split supply, where the negative supply is down to –20V and may be paralleled for higher load current capability.

With a 5V logic supply, the MIC59P50 will typically operate at better than 5MHz. With a 12V logic supply, significantly higher speeds are obtained. The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL circuits may require pull-up resistors.

Each of these eight outputs has an independent over-current shutdown at 500 mA. Upon current shutdown, the affected channel will turn OFF and the flag will go low until V_{DD} is cycled or the $\overline{\text{ENABLE}}$/RESET pin is pulsed high. Current pulses less than 2µs will not activate over-current shutdown. Temperatures above 165°C will shut down the device and activate the open collector FLAG output at pin 1. The UVLO circuit disables the outputs at low V_{DD}; hysteresis of 0.5V is provided.

Features

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Per-Output Over-Current Shutdown (500mA Typical)
- Undervoltage Lockout
- Thermal Shutdown
- Output Fault Flag
- Output Transient Protection Diodes
- CMOS, PMOS, NMOS, and TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches
- Single or Split Supply Operation

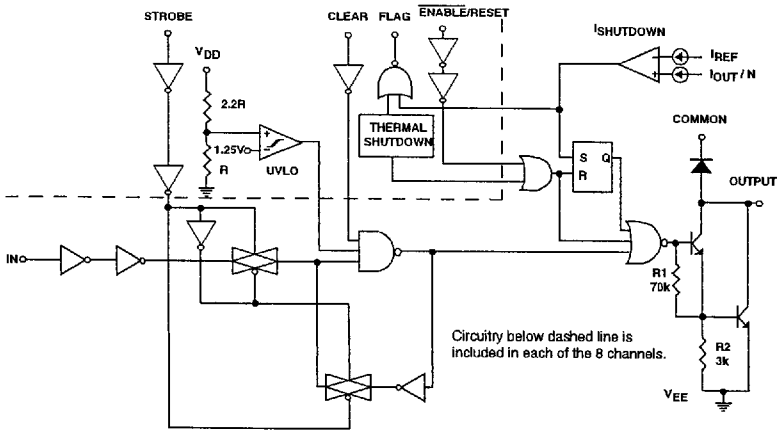
Ordering Information

Part Number	Temperature Range	Package
MIC59P50AJ	–55°C to +125°C	24-Pin Ceramic DIP*
MIC59P50AJB†	–55°C to +125°C	24-Pin Ceramic DIP*
MIC59P50BN	–40°C to +85°C	24-Pin Plastic DIP*
MIC59P50BV	–40°C to +85°C	28-Pin PLCC
MIC59P50BWM	–40°C to +85°C	24-Pin Wide SOIC

* 300-mil "skinny DIP"

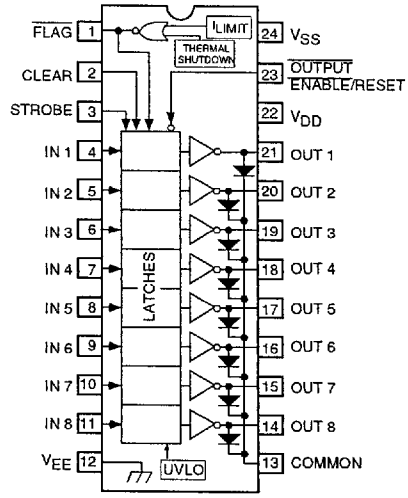
† AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

Functional Diagram



Pin Configuration

(Ceramic and Plastic DIP and SOIC)



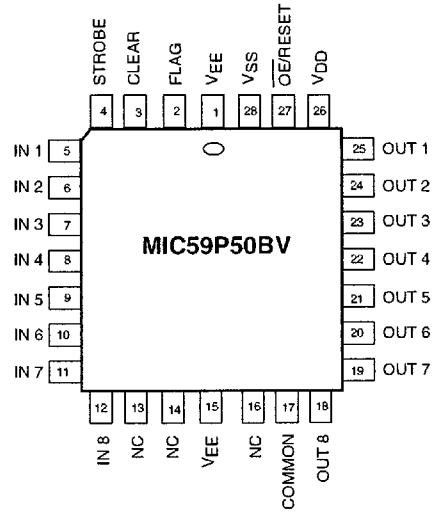
Absolute Maximum Ratings T_A = +25°C

Output Voltage (V_{CE}) 80V
Supply Voltage (V_{DD}) 15V
($V_{DD} - V_{EE}$) 25V
Input Voltage (V_{IN}) ..... –0.3V to V_{DD}+0.3V
Continuous Collector Current (I_C) 500mA
Protected Current ..... 1.5A, **Note 1**
Power Dissipation (P_D)
Plastic DIP (N) 2.4W
Derate above T_A = +25°C ..... 24mW/°C
Ceramic DIP (J) 2.2W
Derate above T_A = +25°C ..... 22mW/°C
PLCC (V) 1.6W
Derate above T_A = +25°C ..... 16mW/°C
Wide SOIC (WM) 1.4W
Derate above T_A = +25°C ..... 14mW/°C
Operating Temperature (T_A)
Plastic DIP (N), PLCC (V), SOIC (WM) .. –40°C to +85°C
Ceramic DIP (J) ..... –55°C to +125°C
Storage Temperature (T_S) ..... –65°C to +150°C
Junction Temperature (T_J) ..... +150°C
ESD ..... **Note 2**

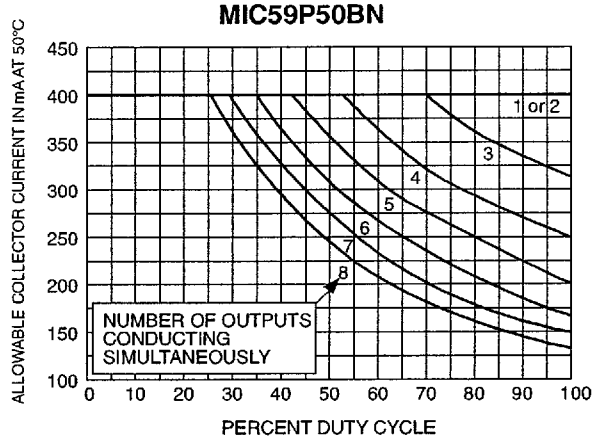
Note 1: Each channel. V_{EE} connection must be designed to minimize inductance and resistance.

Note 2: Devices are input-static protected but can be damage by extremely high static charges.

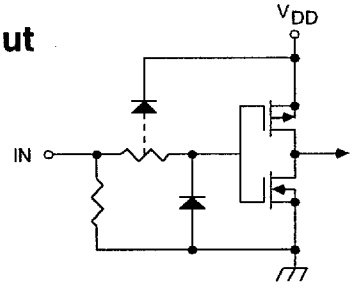
PLCC Pin Configuration



Allowable Output Current



Typical Input



Pin Description

Pin	Name	Description
1	FLAG	Error Flag. Open Collector Output is Low upon Overcurrent Fault or Overtemperature Fault. OUTPUT ENABLE/RESET must be pulled high to reset the flag and fault condition.
2	CLEAR	Sets All Latches OFF (open).
3	STROBE	Input Strobe Pin. Loads output latches when High.
4–11	INPUT	Parallel Inputs, 1 through 8
12	V_{EE}	Output Ground (Substrate). Most negative voltage in the system connects here.
13	COMMON	Transient suppression diodes cathode common pin.
14–21	OUTPUT	Parallel Outputs, 8 through 1.
22	V_{DD}	Logic Positive Supply voltage.
23	$\overline{\text{OUTPUT ENABLE RESET}}$	Output Enable Reset. When Low, Outputs are active. When High, outputs are inactive and the Flag and outputs are reset from a fault condition. An undervoltage condition emulates a high $\overline{OE}$ input.
24	V_{SS}	Logic reference (Ground) pin.

Electrical Characteristics

V_{DD} = 5V; T_A = +25°C; unless noted.

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{CE} = 80V, T_A = +25°C V_{CE} = 80V, T_A = +70°C			50 100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA		0.9	1.1	V
		I_C = 200 mA I_C = 350 mA		1.1 1.3	1.3 1.6	
Input Voltage	$V_{IN(0)}$				1.0	V
	$V_{IN(1)}$	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V **Note 3**	10.5 8.5 3.5			
Input Resistance	R_{IN}	V_{DD} = 12V V_{DD} = 10V V_{DD} = 5.0V	50 50 50	200 300 600		kΩ
$\overline{\text{Flag}}$ Output Current	I_{OL}	V_{OL} = 0.4V		15		mA
$\overline{\text{Flag}}$ Output Leakage	I_{OH}	V_{OH} = 12.0V		50		nA
Supply Current	$I_{DD(ON)}$ (One output active)	V_{DD} = 12V, Outputs Open V_{DD} = 10V, Outputs Open V_{DD} = 5.0V, Outputs Open		3.3 3.1 2.4	4.5 4.5 3.6	mA
	$I_{DD(ON)}$ (All outputs active)	V_{DD} = 12V, Outputs Open V_{DD} = 10V, Outputs Open V_{DD} = 5.0V, Outputs Open		6.4 6.0 4.7	10.0 9.0 7.5	mA
	$I_{DD(OFF)}$ (Total)	V_{DD} = 12V, Outputs Open, Inputs = 0V V_{DD} = 5.0V, Outputs Open, Inputs = 0V		3.0 2.2	4.5 3.6	mA
Clamp Diode Leakage Current	I_R	V_R = 80V, T_A = +25°C V_R = 80V, T_A = +70°C			50 100	µA
Over-Current Threshold	I_{LIM}	Each Output		500		mA
Start-Up Voltage	V_{SU}	**Note 4**	3.5	4.0	4.5	V
Minimum Operating V_{DD}	$V_{DD\ MIN}$		3.0	3.5	4.0	V
Clamp Diode Forward Voltage	V_F	I_F = 350 mA		1.7	2.0	V
Thermal Shutdown				165		°C
Thermal Shutdown Hysteresis				10		

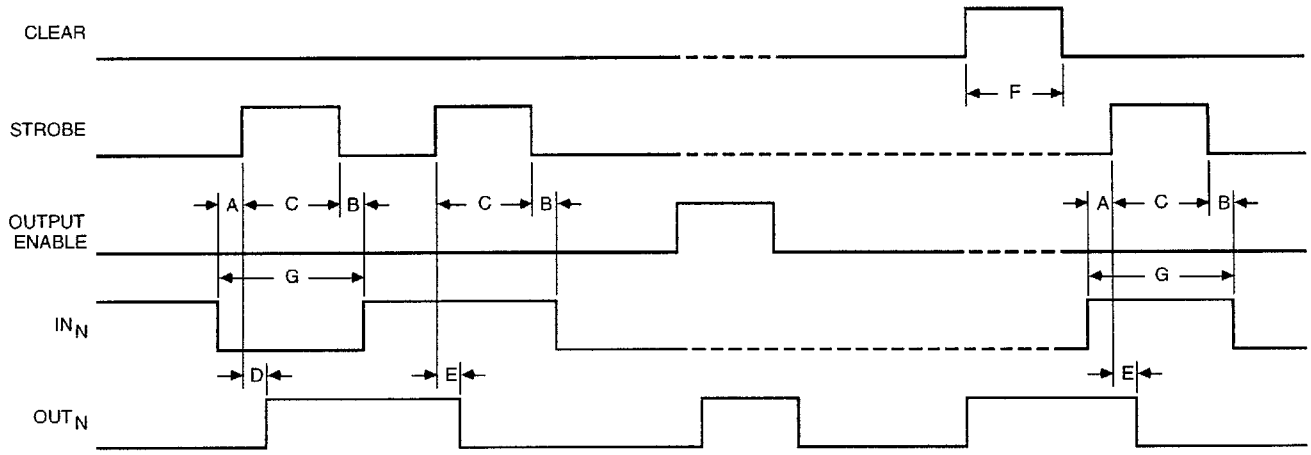
NOTE 3: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".
NOTE 4: Undervoltage lockout is guaranteed to release device at no more than 4.5V and disable the device at no less than 3.0V input logic voltage.

Truth Table

IN_N	Strobe	Clear	Output Enable	OUT_N t–1	OUT_N t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = Irrelevant
t–1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the off condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches. If current shutdown is activated, the OUTPUT ENABLE must be pulsed high to restore operation and reset the Flag. Over temperature faults are not latched and require no reset pulse.



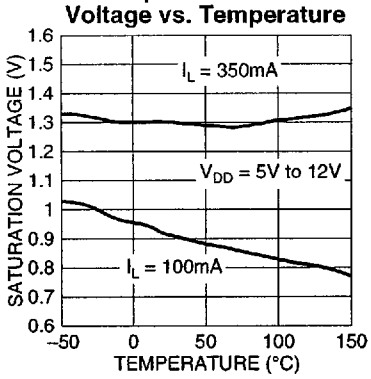
Timing Conditions

(T_A = +25°C, Logic Levels are V_{DD} and V_{SS}, V_{DD} = 5V).

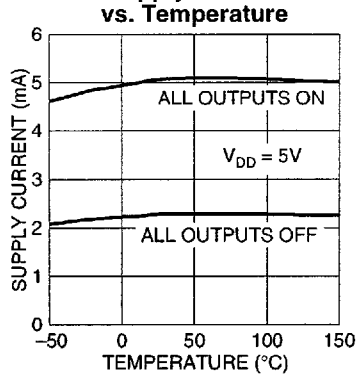
A. Minimum data active time before strobe enabled (data set-up time) ..... 50 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 50 ns
C. Minimum strobe pulse width ..... 125 ns
D. Typical time between strobe activation and output on to off transition ..... 500 ns
E. Typical time between strobe activation and output off to on transition ..... 500 ns
F. Minimum clear pulse width ..... 300 ns
G. Minimum data pulse width ..... 225 ns

Typical Characteristic Curves

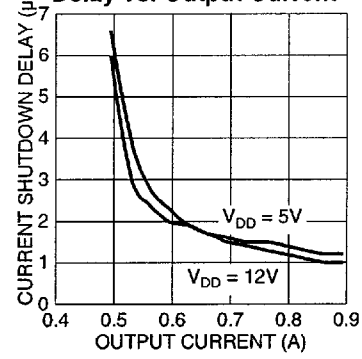
Output Saturation Voltage vs. Temperature



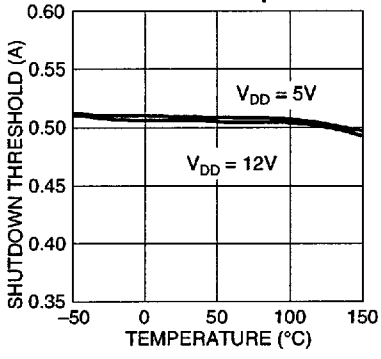
Supply Current vs. Temperature



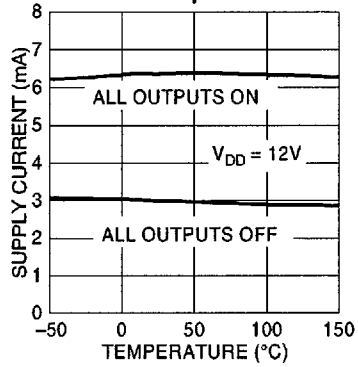
Current Shutdown Delay vs. Output Current



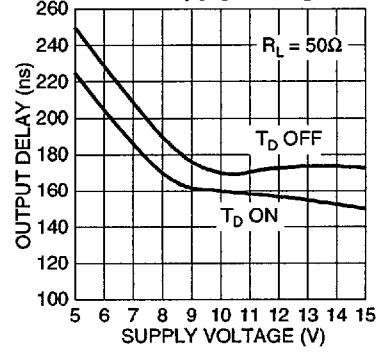
Current Shutdown Threshold vs. Temperature



Supply Current vs. Temperature

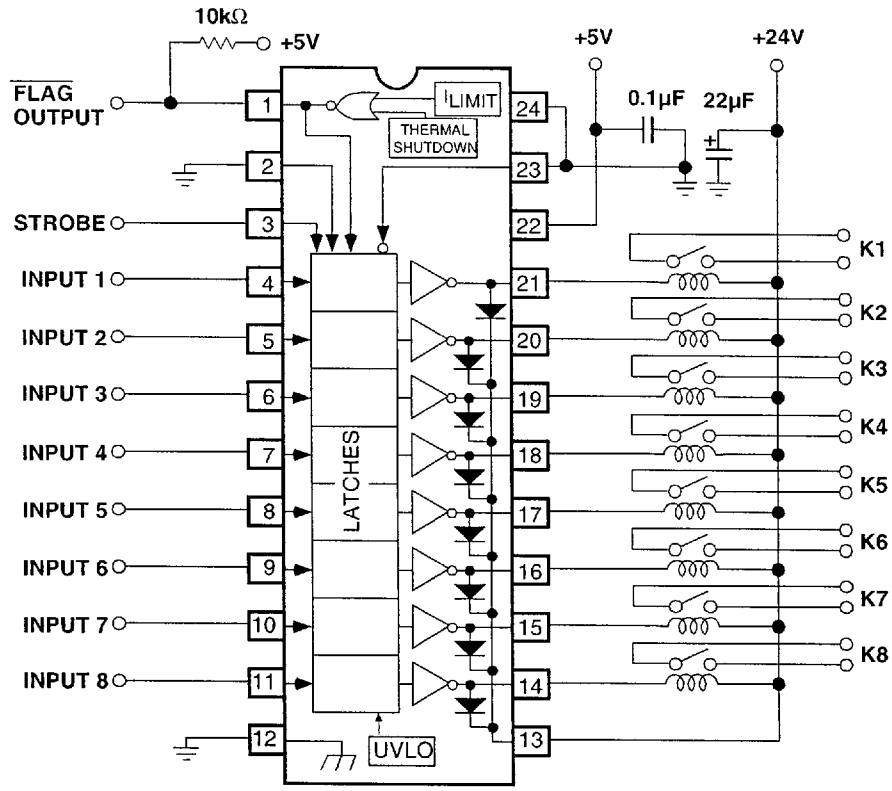


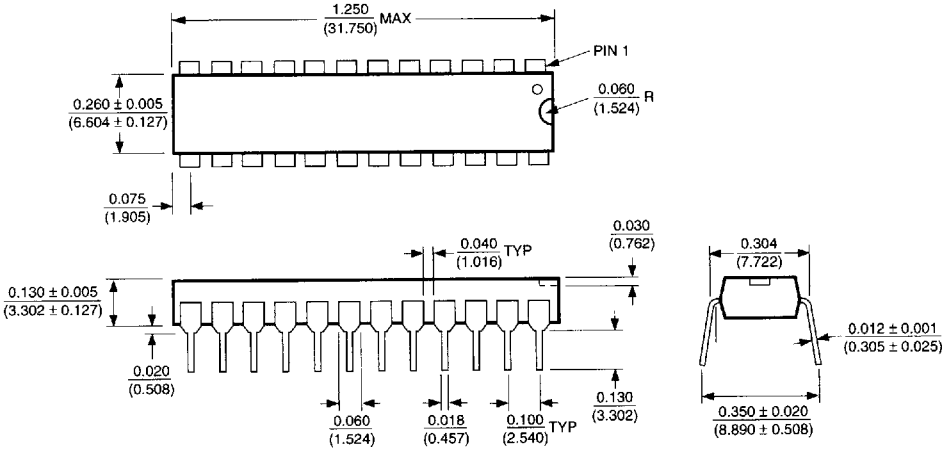
Output Enable Delay vs. Supply Voltage



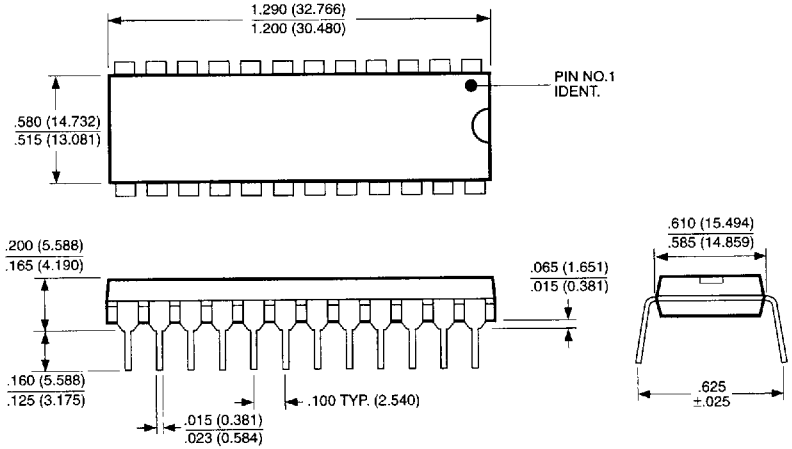
Typical Applications

MIC59P50 Protected Relay Driver





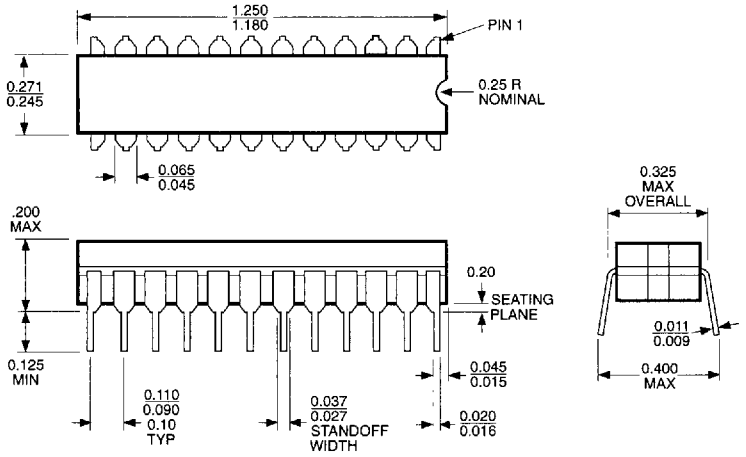
24-Pin Plastic Skinny DIP (N)



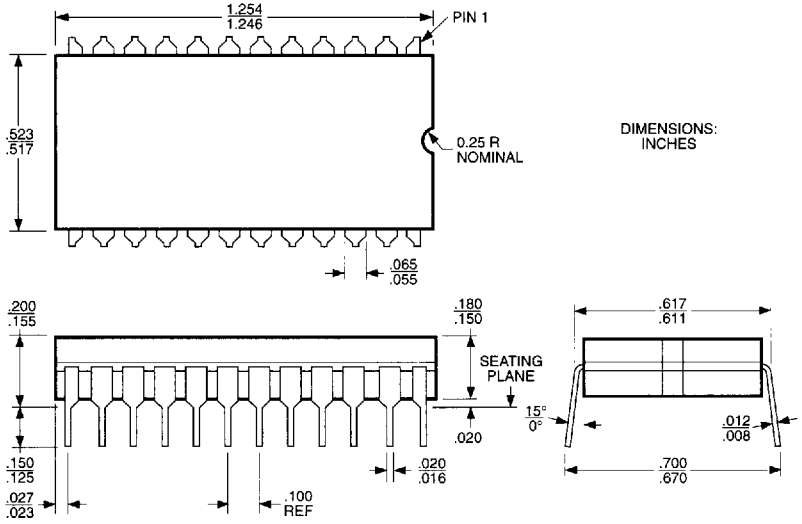
24-Pin Plastic DIP (N)

Note: Pin 1 is denoted by one or more of the following: a notch, a printed triangle, or a mold mark.

6088819 0001943 983

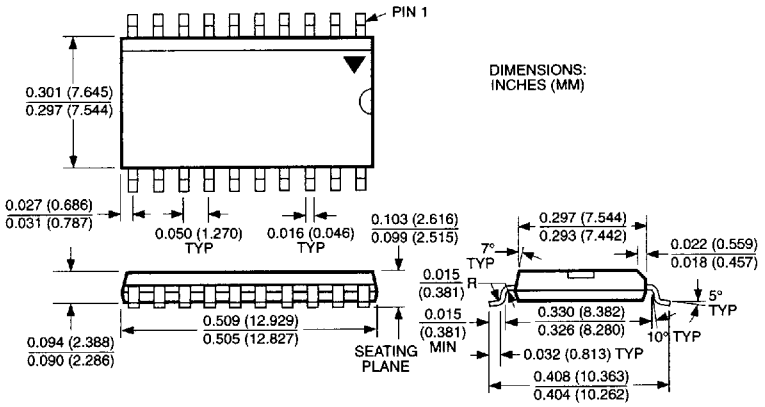


24-Pin Ceramic Skinny DIP (J)

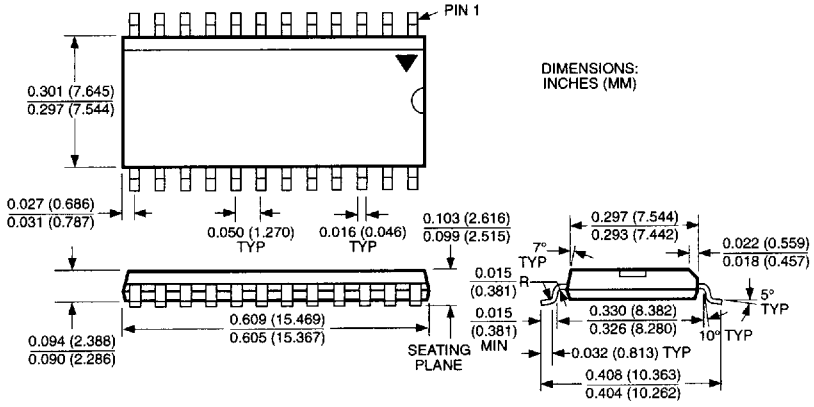


24-Pin Ceramic DIP (J)

6088819 0001949 3T1

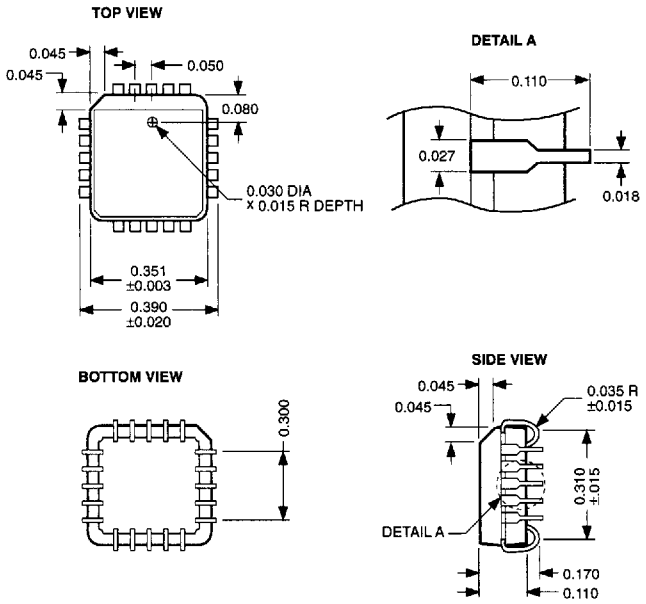


20-Pin Wide SOIC (WM)

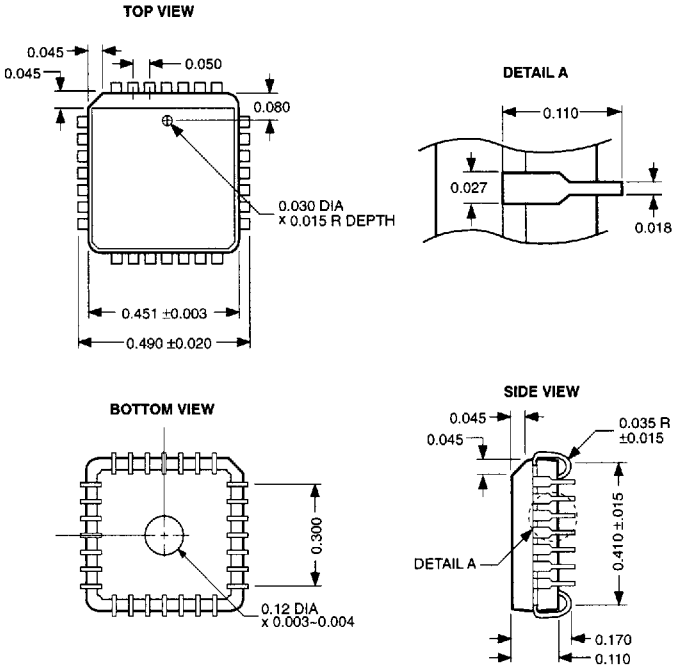


24-Pin Wide SOIC (WM)

6088819 0001954 769



20-Pin PLCC (V)



28-Pin PLCC (V)

6088819 0001955 6T5