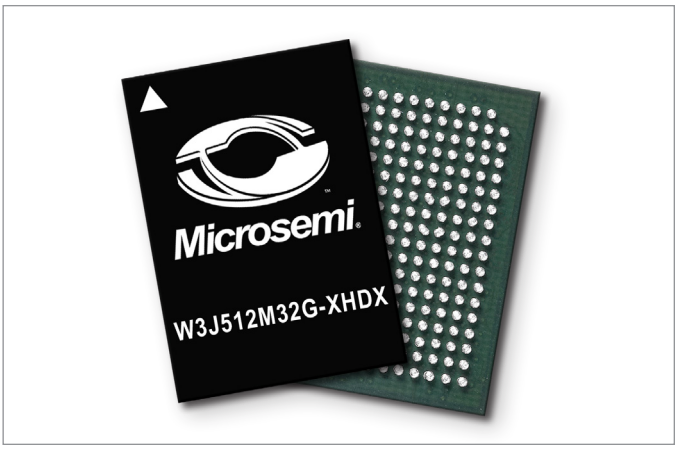
2GB (x32) High Density DDR3 SDRAM

Models: W3J512M32G-XHDX
W3J512M32K-XHDX

The W3J512M32G-XHDX and W3J512M32K-XHDX are Microsemi's latest family of high density/high performance DDR3 SDRAM's. These are designed to support high performance processors and FPGAs.



Product Features

- DDR3 Data Rate = 800, 1066, 1333 Mb/s
- V_{CC} = V_{CCQ} = 1.5V or 1.35V
- Differential bidirectional data strobe byte
- 8-bit prefetch architecture
- Eight internal banks for concurrent operation
- Auto Refresh and Self Refresh Modes
- On Die Termination (ODT), nominal and dynamic for data, strobe and mask signals
- Output driver calibration
- Programmable CAS latency: 5, 6, 7, 8, 9 or 10
- Posted CAS additive latency: 0, CL-1, CL-2
- CAS# Write latency = 5, 6, 7 or 8 based on t_{CK}
- Fixed burst length of 8 (BL8) and burst chop of 4 (BC4) via the mode register
- t_{CK} range: 400 - 667MHz
- Write leveling
- Configured as 1-Rank x32-bit data

Package

- 10 x 14mm, 168 Plastic Ball Grid Array (PBGA), 140mm^2
- 2.5 mm package body thickness max
- 0.8 mm pitch
- Tin lead ball attach

Benefits

- 68% space saving
- 46% I/O reduction
- Reduced part count from 4 to 1
- Reduced layer count
- Suitable for hi-reliability applications
- Commercial, industrial and military temperature ranges
- Typically lower power at same data rate when compared to DDR2

** This product may or may not be under development, not qualified or characterized and is subject to change or cancellation without notice.*

Contact your Microsemi Sales Representative for availability.

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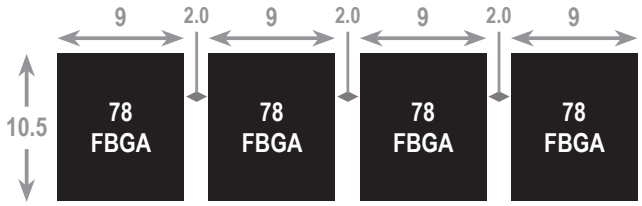
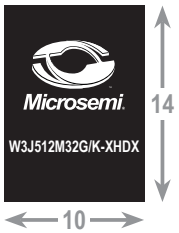
Density Comparison for the x32 device

	CSP Approach (mm)	W3J512M32G/K-XHDX	SAVINGS
			
Area	441 mm^2	140 mm^2	68%
I/O Count	4 x 78 balls = 312 balls	168 Balls	46%

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