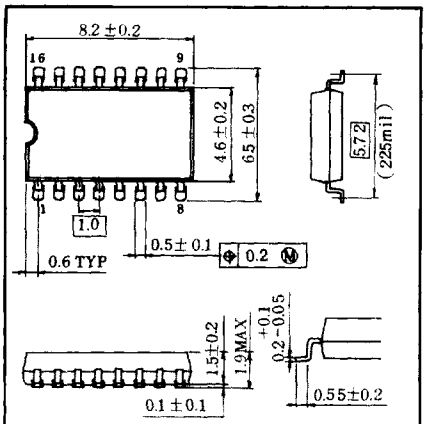
FM IF DETECTION

Unit in mm



Package width and length do not include mold protrusion.
Allowable mold protrusion is 0.15mm.

JEDEC	—
TOSHIBA	SSOP16-P-225

TA8104F is an IF detecting IC designed for the application to paging system.

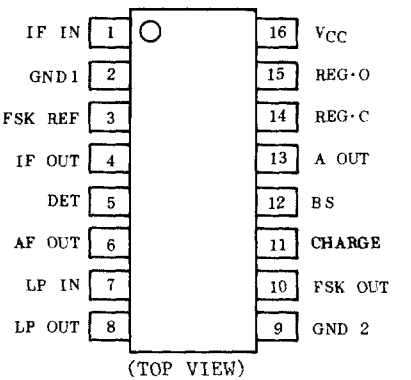
- High sensitive IF limiter amplifier
- Non-adjusting type quadrature detection
- Low-pass filter amplifier (LPA)
- FSK waveform shaping
- Battery saving (BS)
- Alarm function (ALM)
- External constant voltage output

- Built-in low-pass filter and waveform shaping circuit enable the extraction of FSK signals from voice signal.
- Built-in battery-saving function can reduce the load upon the battery which is functioning as power supply.
- Alarm function makes possible the observation of battery consumption which is constituting power supply. Alarm sensitivity is 1.1V(Typ.).
- Constant voltage power supply can be fabricated through externally adding a transistor : V_{reg}=1.0V(Typ.)
- Extremely low consumption current : I_{CCQ}=700μA(Typ.)
- Wide range of operating power supply voltage
  : V_{opr}=1.1~5.0V (Ta=25°C)

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	5	V
Power Dissipation	P_D	370	mW
Operating Temperature	T_{opr}	-30~85	°C
Storage Temperature	T_{stg}	-55~150	°C

PIN CONNECTION



(TOP VIEW)

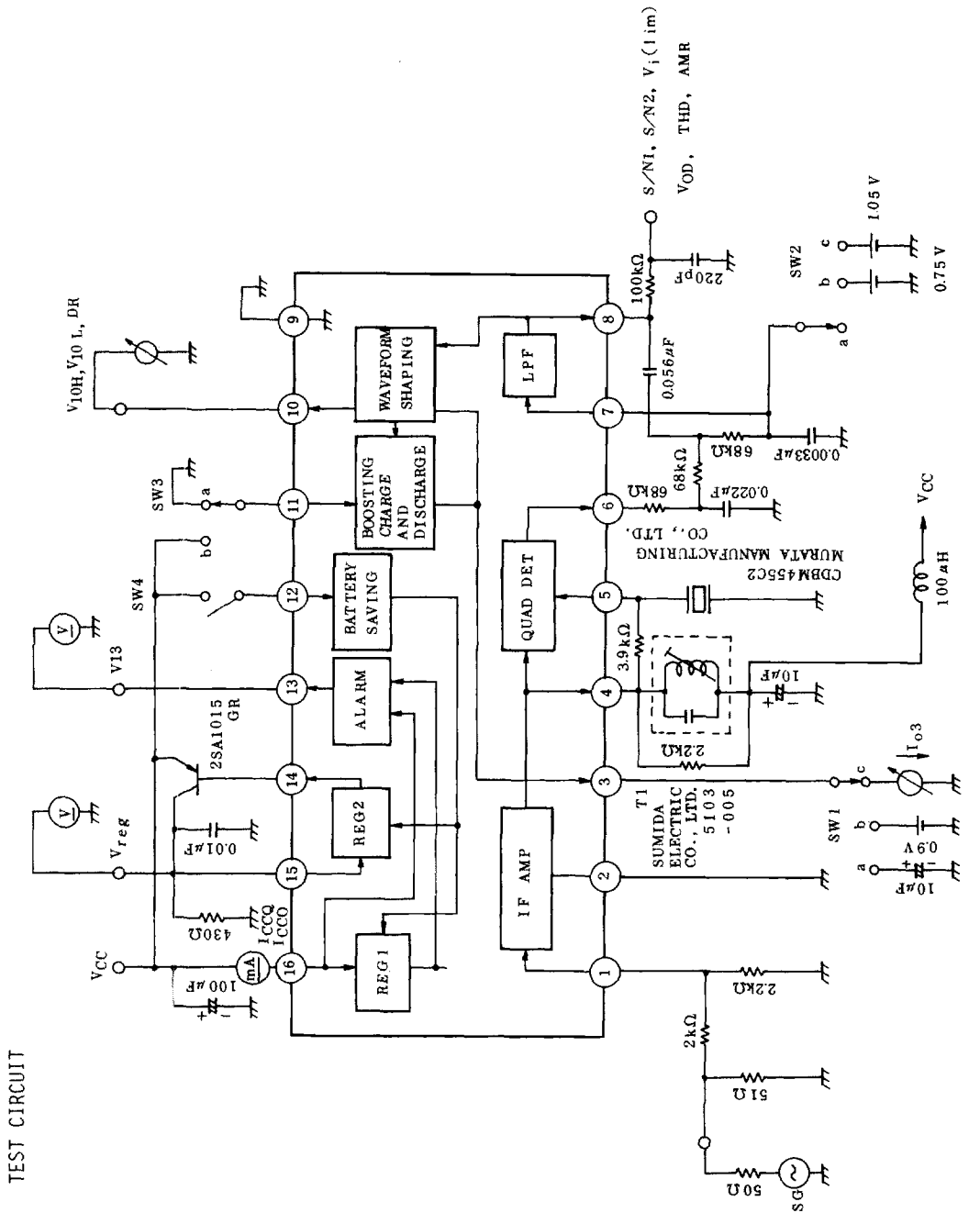
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC}=1.4V, f_i=455kHz, Dev=±2.5kHz, f_m=100Hz, V_i=60dBμ, SW1=SW2=SW3=a, SW4=ON, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Quiescent Current		I_{CCQ}	-	V_i=0		0.4	0.7	1.0	mA
Supply Current at Battery Saving		I_{CCO}	-	V_i=0, SW4=OFF		-	-	10	μA
Signal to Noise Ratio		S/N1	-	V_i=21dBμ		8	-	-	dB
		S/N2	-			33	40	-	
Limiting Sensitivity Voltage		$V_{i(lim)}$	-			-	20	-	dBμ
Detected Output Voltage		V_{OD}	-			20	30	40	mV_{rms}
Total Harmonic Distortion Ratio		THD	-			-	-30	-	dB
AM Rejection Ratio		AMR	-	AM=30%		-	30	-	dB
Waveform-shaped Output Voltage		V_{10H}	-	SW2=b	SW1=b	1.07	-	-	V
		V_{10L}	-	SW2=c	V_{CC}=1.1V	-	-	0.15	
Waveform-shaped Duty Ratio		DR	-			-	50	-	%
Alarm Output Voltage		V_{13L}	-	V_{16}=1.17V		-	-	150	mV
		V_{13H}	-	V_{16}=1.03V		0.99	-	-	V
Constant Voltage Output		V_{reg}	-			0.93	1.0	1.07	V
IF AMP. Input Impedance	Parallel resistance	R_{ip}	-			-	20	-	kΩ
	Parallel capacity	C_{ip}	-			-	8.6	-	pF
Pin-charge Current		I_{O3}	-	SW1=C, SW3=b		-	45	-	μA

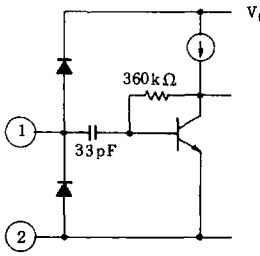
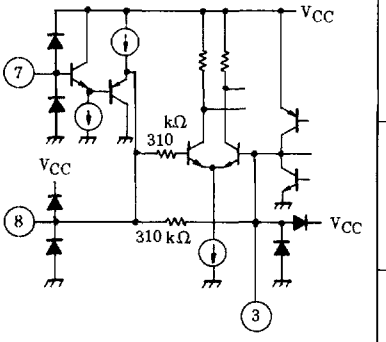
Note: V_i is SG open-end output minus 13dB.

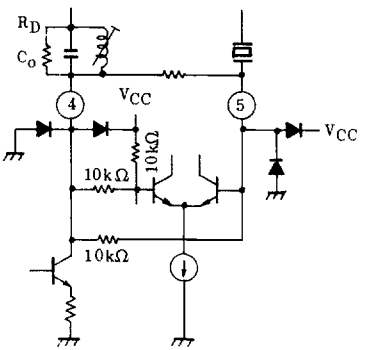
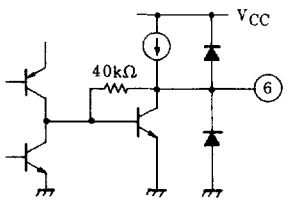
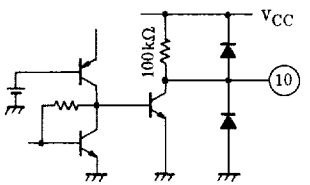
TEST CIRCUIT

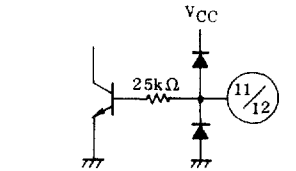
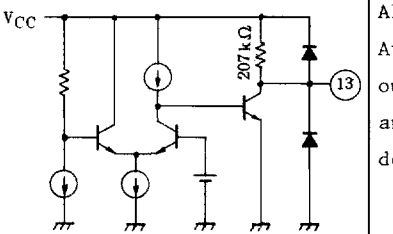
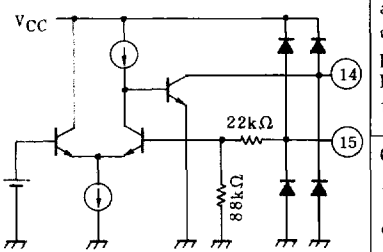


TERMINAL DESCRIPTION

(Terminal voltage is the typical value at V_{CC}=1.4V, Ta=25°C and quiescent time in test circuit.)

TERMINAL No.	TERMINAL NAME	TERMINAL VOLTAGE	INTERNAL EQUIVALENT CIRCUIT (Resistance and capacity are typical values)	FUNCTION
1	IF IN	0		Input terminal of IF AMP. This AMP. is made into BPF AMP. construction of f_0=455kHz for stably amplifying IF signal.
2	GND 1	0		GND of IF AMP.
3	FSK REF	0.9		Reference input terminal of differential AMP. which is constituting waveform-shaping section. Externally connect condenser. By the boosting charge and discharge circuit of pushpull output, potentials of ③ pin and ⑧ pin can be made equal.
7	LP IN	0.9		Input terminal for LPF. Bias is supplied from ⑥ pin through external resistance.
8	LP OUT	0.9		Output terminal for LPF. Construction is of emitter-follower type, however, potential is maintained equal to that of input terminal for LPF.

TERMINAL No.	TERMINAL NAME	TERMINAL VOLTAGE	INTERNAL EQUIVALENT CIRCUIT (Resistance and capacity are typical values)	FUNCTION
4	IF OUT	1.4		Output terminal of IF AMP. Externally connect tuning coil. At this time, RD of 2.2kΩ is recommendable for stabilizing the IF AMP. If f_O temperature characteristic of whole set can be compensated, C_O of 470pF or over (for example, 10000pF) is advisable for increasing practical sensitivity.
5	DET	1.4		Phase-shift input terminal of FM demodulator. Externally connect resonator CDBM455C2 made by MURATA MANUFACTURING CO.,LTD.
6	AF OUT	0.9		FM demodulated output.
9	GND 2	0		GND terminal other than IF AMP.
10	FSK OUT	0.7		Waveform-shaped output terminal. FSK signal, which is input from LPF out ⑧ pin and of which waveform is shaped, is output as inverted signal.

TERMINAL No.	TERMINAL NAME	TERMINAL VOLTAGE	INTERNAL EQUIVALENT CIRCUIT (Resistance and capacity are typical values)	FUNCTION
11	CHARGE	0		Terminal for controlling the operation of boosting charge-and-discharge circuit. Operates at "H".
12	BS	1.4		Terminal for controlling the operation of battery saving. Operates at "H".
13	A OUT	0.1		Alarm output terminal. At $V_{CC} \simeq 1.1V$, this terminal output becomes "H" ($\simeq V_{CC}$) and can indicate deterioration of battery.
14	REG·C	0.7		Becomes terminal for controlling the transistor for external current amplifier at the fabrication of regulator for external power supply. Externally connect PNP transistor.
15	REG·O	1.0		Output voltage monitoring terminal of regulator for external power supply.
16	V_{CC}	1.4		Power supply terminal.

. Function of Battery-Saving

Since the battery-saving function is built in, this IC can minimize the consumption of battery by means of reducing the consumption current through the battery-saving function when the battery is applied as the power supply of the set.
Since the BS terminal (⑫ pin) functions as the base input of the NPN transistor, the IC can be driven by the C-MOS output of the microcomputer because of its high input impedance and the drivability with low power.

STATE OF BS TERMINAL (⑫ PIN)	BATTERY-SAVING FUNCTION	EACH CIRCUIT OPERATION STATE IN OTHER ICS	CONSUMPTION CURRENT OF IC (AT QUIESCENT TIME)
L	Battery-saving state	Operation-stop state	10μA(TYP.)
H	Battery-saving OFF state	Normal-operation state	700μA(TYP.)

. FSK Waveform Shaping Function

For extracting the FSK signal from the FSK modulation signal, the waveform is shaped by the waveform shaping circuit (comparator) in IC and is turned into a more correct logic output resulting in reducing the read error of the microcomputer when the FSK signal level is low or the noise is superimposed upon the FSK signal in the weak electric field.

. Quick Charge-and-Discharge Circuit

At the time when the battery-saving OFF state (Normal operation state) is restored from the battery-saving state, if the FSK signal is input, the time for the FSK REF terminal (③pin) to arrive at the reference voltage is delayed by the time constant determined by the capacitor connected to the FSK REF terminal (③pin) and the internal resistance.
In this case, sometimes the erroneous waveform-shaping signal is output due to the error of the input voltage of the waveform-shaping circuit (comparator).
In such a case, by means of quickly discharging the capacitor connected to the FSK REF terminal (③pin) through the quick charge-and-discharge circuit, the time for the FSK REF terminal (③pin) to become the same potential as that of the LP OUT terminal is shortened and the output of the erroneous waveform-shaping signal is prevented.

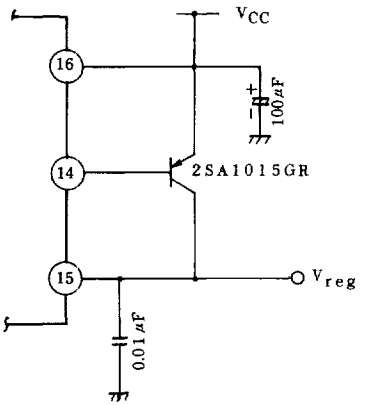
* The quick charge-and-discharge circuit becomes active when the charge terminal (⑪ pin) is at "H".

. Alarm Function

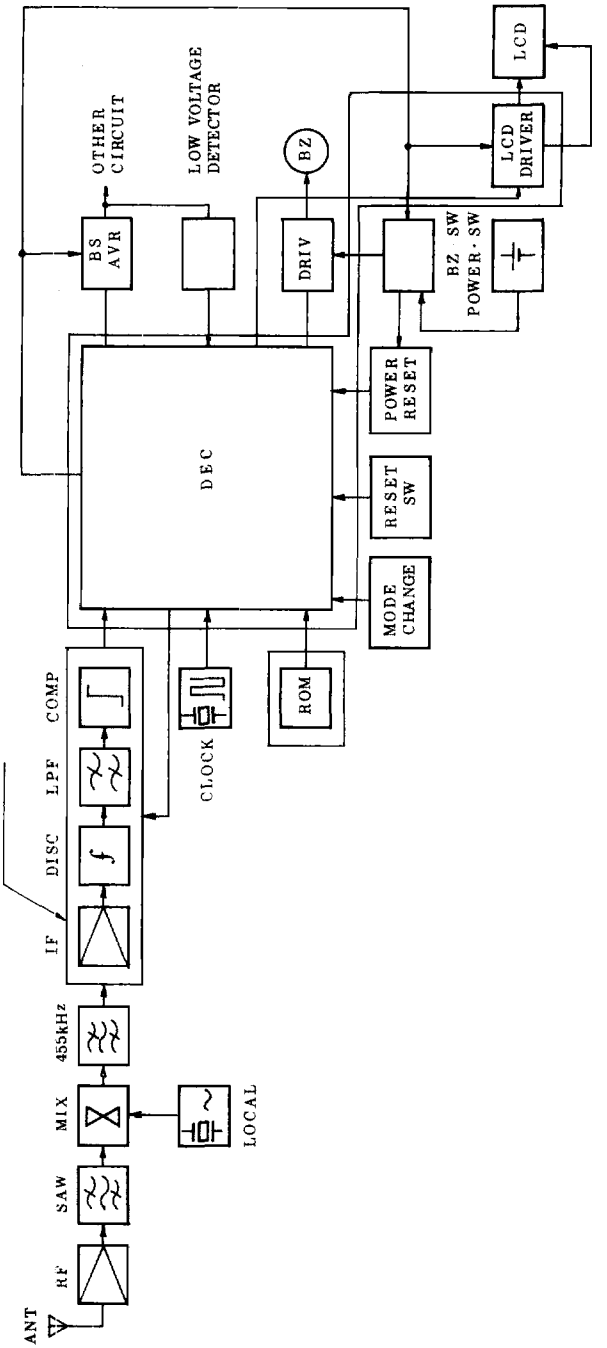
In case the battery is used as the power supply of the set, when the power supply voltage is reduced and the voltage of the V_{CC} terminal ((16) pin) becomes approx. 1.1V, the output of the A OUT terminal ((13) pin) rises approx. up to 1.1V and the consumption of the battery power can be detected.

. External Constant Voltage Output Function

Through externally mounting the transistor on the REG·C terminal ((14) pin) as shown in the figure below, the REG·O terminal ((15) pin) can be used for the constant voltage output V_{reg}=1.0V(TYP.) of high-output type.
At the time of the battery-saving function operation, the constant voltage output also becomes OFF.



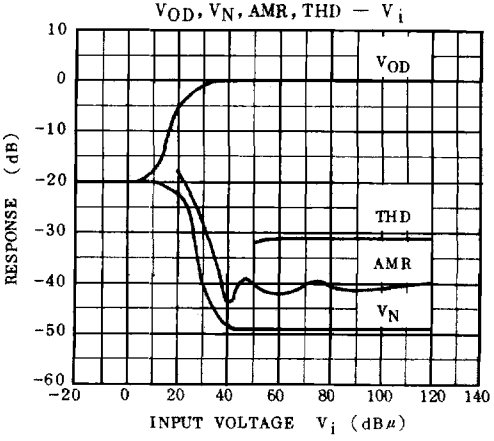
APPLICATION EXAMPLE



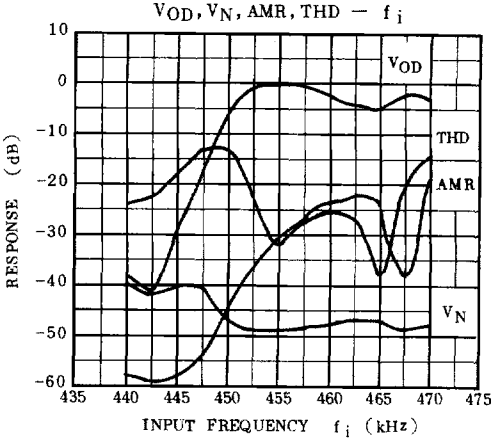
COIL DATA (Typical value)

COIL No.	STAGE	TEST FREQUENCY (kHz)	L (μH)	C_o (pF)	Q_o	No. OF TURNS				KIND OF WIRE (mm)	REMARKS
						1-2	2-3	1-3	4-6		
T1	DET	455		470	60			135		0.05 UEW	

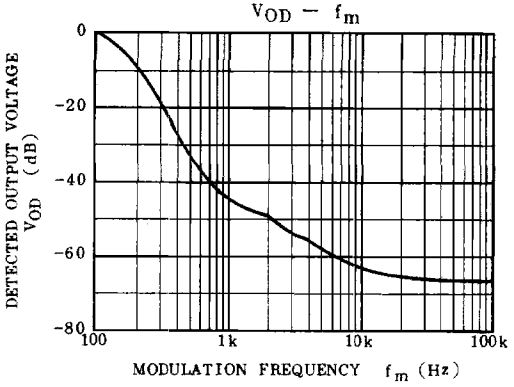
$V_{OD}, V_N, AMR, THD - V_i$



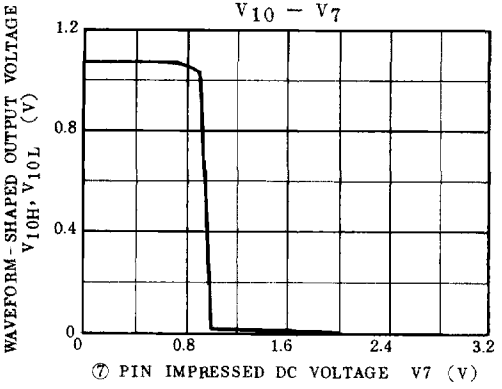
$V_{OD}, V_N, AMR, THD - f_i$



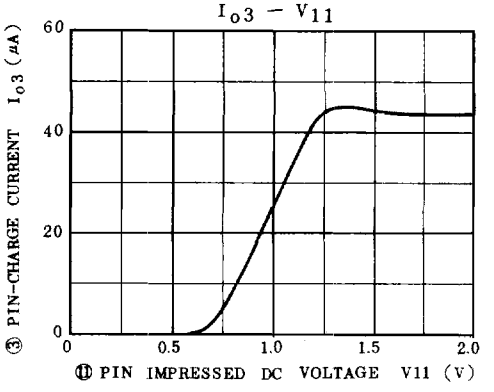
$V_{OD} - f_m$



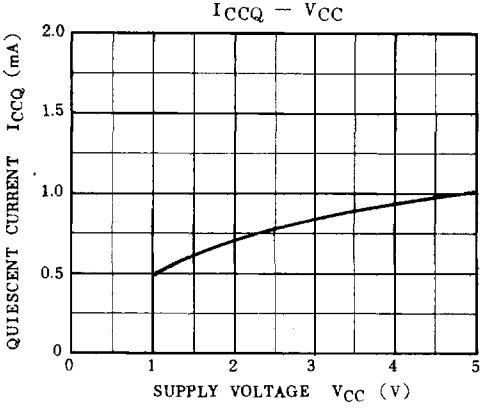
$V_{10} - V_7$



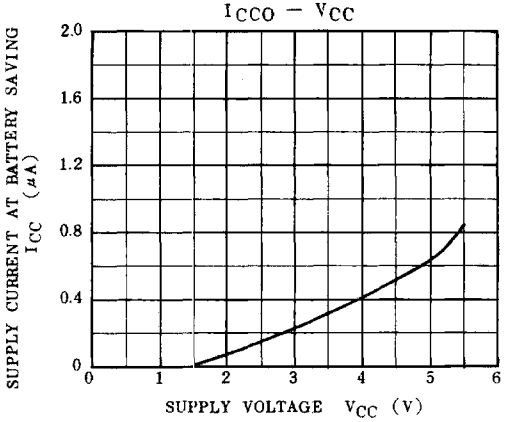
$I_{o3} - V_{11}$



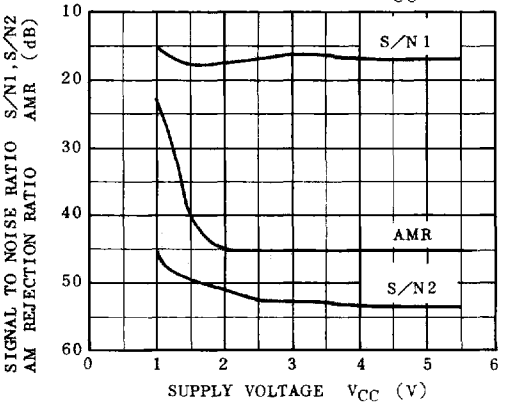
$I_{CCQ} - V_{CC}$



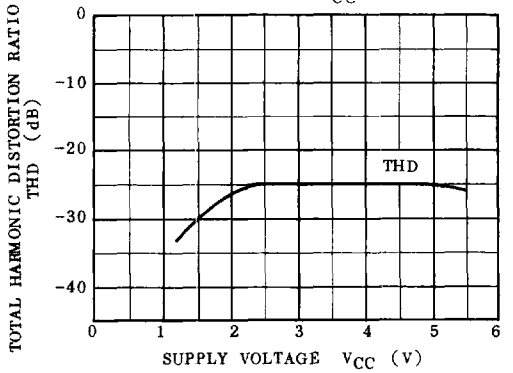
$I_{CCO} - V_{CC}$



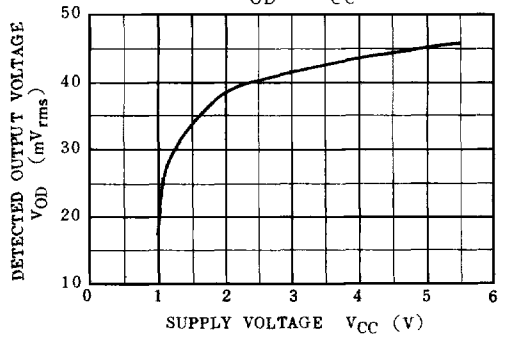
S/N1, S/N2, AMR − V_{CC}



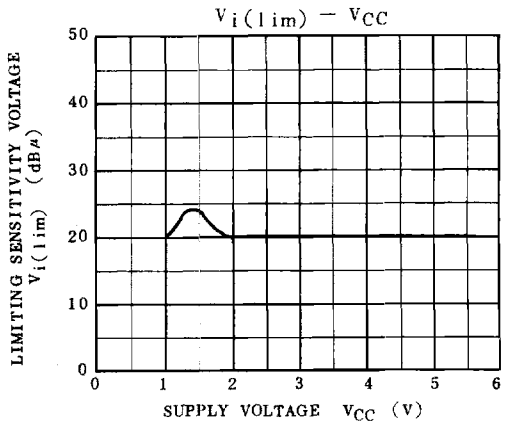
THD − V_{CC}



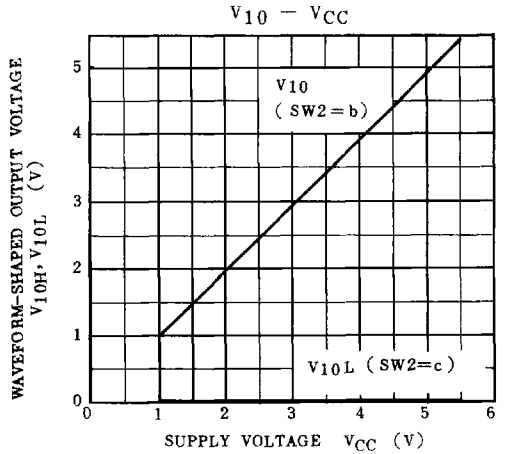
$V_{OD} - V_{CC}$



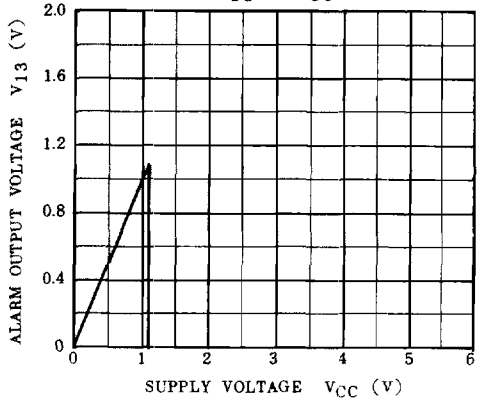
$V_{i(lim)} - V_{CC}$



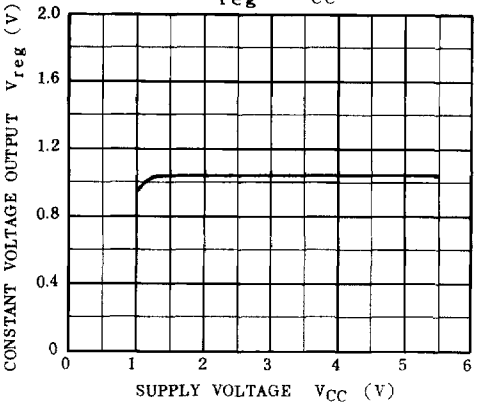
$V_{10} - V_{CC}$



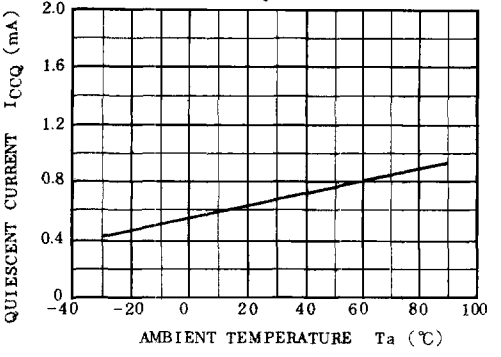
$V_{13} - V_{CC}$



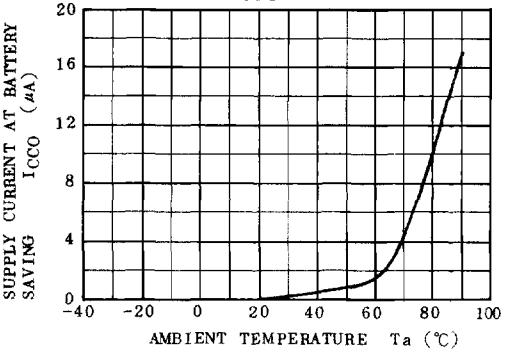
$V_{reg} - V_{CC}$



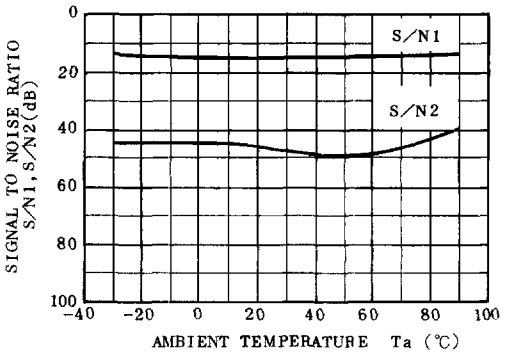
$I_{CCQ} - Ta$



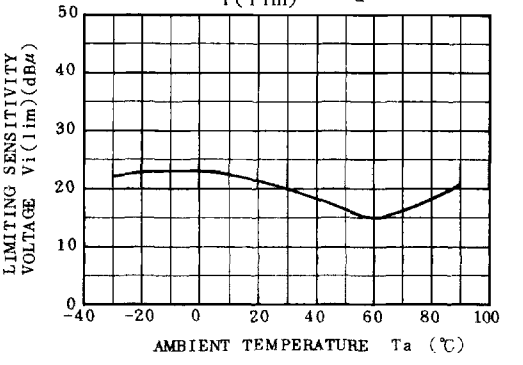
$I_{CCO} - Ta$



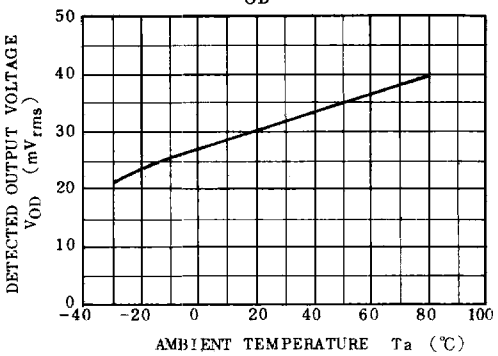
S/N1, S/N2 — Ta



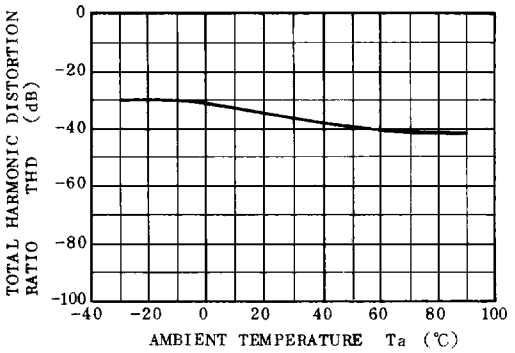
$V_{i(lim)} - Ta$



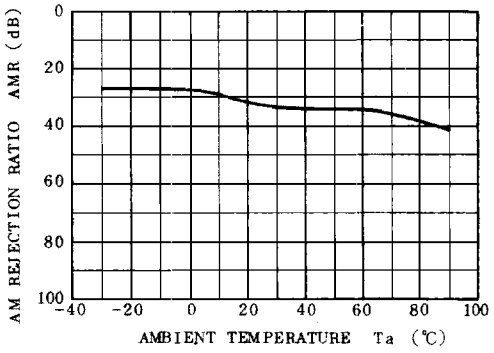
V_{OD} – Ta



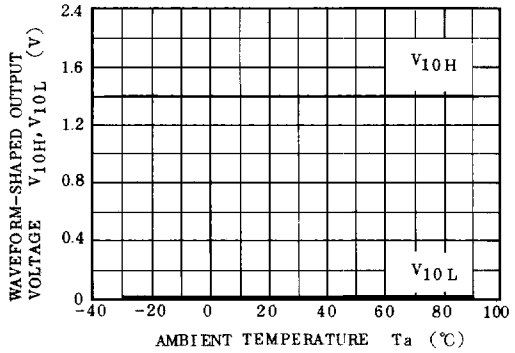
THD – Ta



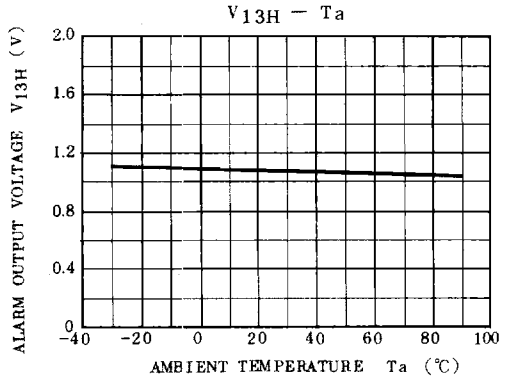
AMR – Ta



V_{10H}, V_{10L} – Ta



V_{13H} – Ta



V_{reg} – Ta