

# INT202

## Low-side Driver IC

### Low-side Drive and High-side Control for Simultaneous Conduction



#### Product Highlights

##### 5 V CMOS Compatible Control Inputs

- Combines logic inputs for low and high-side drives
- Schmidt-triggered inputs for noise immunity

##### Built-in High-voltage Level Shifters

- Integrated level shifters simplify high-side interface
- Can withstand up to 800 V for direct interface to the INT201 high-side driver
- Pulsed high-voltage level shifters reduce power consumption

##### Gate Drive Output for an External MOSFET

- Provides 300 mA sink/150 mA source current
- Can drive MOSFET gate at up to 15 V
- External MOSFET allows flexibility in design for various motor sizes

##### Built-in Protection Features

- UV lockout

## Description

The INT202 Low-side driver IC provides gate drive for an external low-side MOSFET switch and high-side level shifting. When used in conjunction with the INT201 high-side driver, the INT202 provides a simple, cost-effective interface between low-voltage control logic and high-voltage loads. The INT202 is designed to be used with rectified 110 V or 220 V supplies. Both high side and low side switches can be controlled independently from ground-referenced 5 V logic inputs on the low side driver.

Pulsed level shifting saves power and provides enhanced noise immunity. The circuit is powered from a nominal 15 V supply to provide adequate gate drive for external N-channel MOSFETs.

Applications include switched reluctance motor drives. The INT202 can also be used to implement multi-phase configurations.

The INT202 is available in 8-pin plastic DIP and SOIC packages.

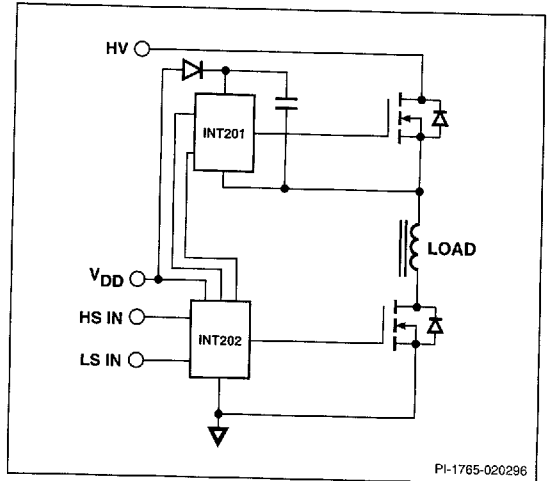


Figure 1. Typical Application

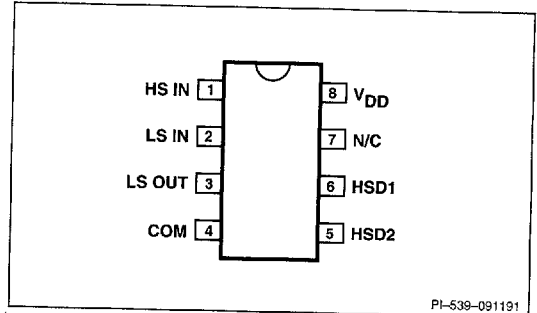


Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	PACKAGE OUTLINE	ISOLATION VOLTAGE
INT202PFI1	PO8A	600 V
INT202TFI1	TO8A	600 V
INT202PFI2	PO8A	800 V
INT202TFI2	TO8A	800 V



## Pin Functional Description

**Pin 1:** Active-high logic-level input  $\overline{HS\ IN}$  controls the pulse circuit which signals the INT201 high-side driver.

**Pin 2:** Active-high logic level input  $LS\ IN$  controls the low side driver output.

**Pin 3:**  $LS\ OUT$  is the driver output which controls the low-side MOSFET.

**Pin 4:**  $COM$  connection; analog reference point for the circuit.

**Pin 5:** Level shift output  $HSD\ 2$  signals the high-side driver to turn off. One short, precise pulse is sent on each positive transition of  $\overline{HS\ IN}$ .

**Pin 6:** Level shift output  $HSD\ 1$  signals the high-side driver to turn on. Two short, precise pulses are sent on each negative transition of  $\overline{HS\ IN}$ .

**Pin 7:** N/C for creepage distance.

**Pin 8:**  $V_{DD}$  supplies power to the logic, high-side interface, and low-side driver.

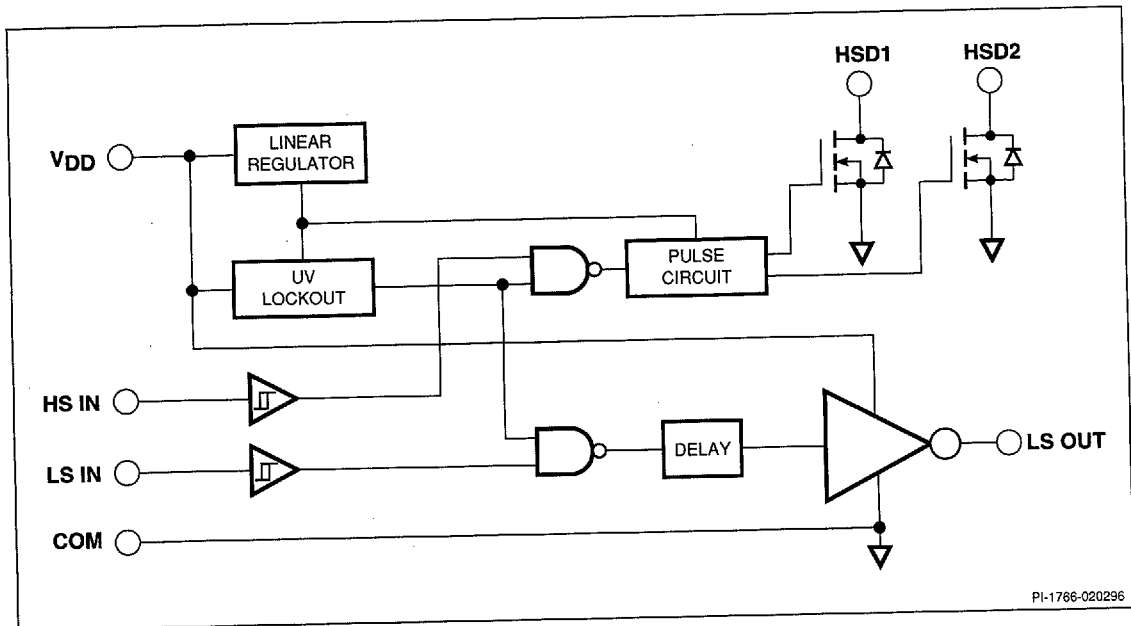


Figure 3. Functional Block Diagram of the INT202

## INT202 Functional Description

### 5 V Regulator

The 5 V linear regulator circuit provides the supply voltage for the control logic and high-voltage level shift circuit. This allows the logic section to be directly compatible with 5 V CMOS logic without the need of an external 5 V supply.

### Undervoltage Lockout

The undervoltage lockout circuit disables the LS OUT pin and both HSD pins whenever the  $V_{DD}$  power supply falls below typically 9.0 V, and maintains this condition until the  $V_{DD}$  power supply rises above typically 9.35 V. This guarantees that both MOSFETs will remain off during power-up or fault conditions.

### HSD1/HSD2

The HSD1 and HSD2 outputs are connected to integrated high-voltage N-channel MOSFET transistors which perform the level-shifting function for communication to the high-side driver. Controlled current capability allows the drain voltage to float with the high-side driver. Two individual channels produce a true differential communication channel for accurately controlling the high-side driver in the presence of fast moving high-voltage waveforms.

### Pulse Circuit

The pulse circuit provides the two high-voltage level shifters with precise timing signals. Two pulses are sent over HSD1 to signal the high-side driver to turn on. One pulse is sent over HSD2 to signal the high-side driver to turn off. The combination of differential communication with the precise timing provides maximum immunity to noise.

### Driver

The CMOS drive circuit provides drive power to the gate of the MOSFET used on the low side of the half bridge circuit. The driver consists of a CMOS buffer capable of driving an external transistor gate at up to 15 V.

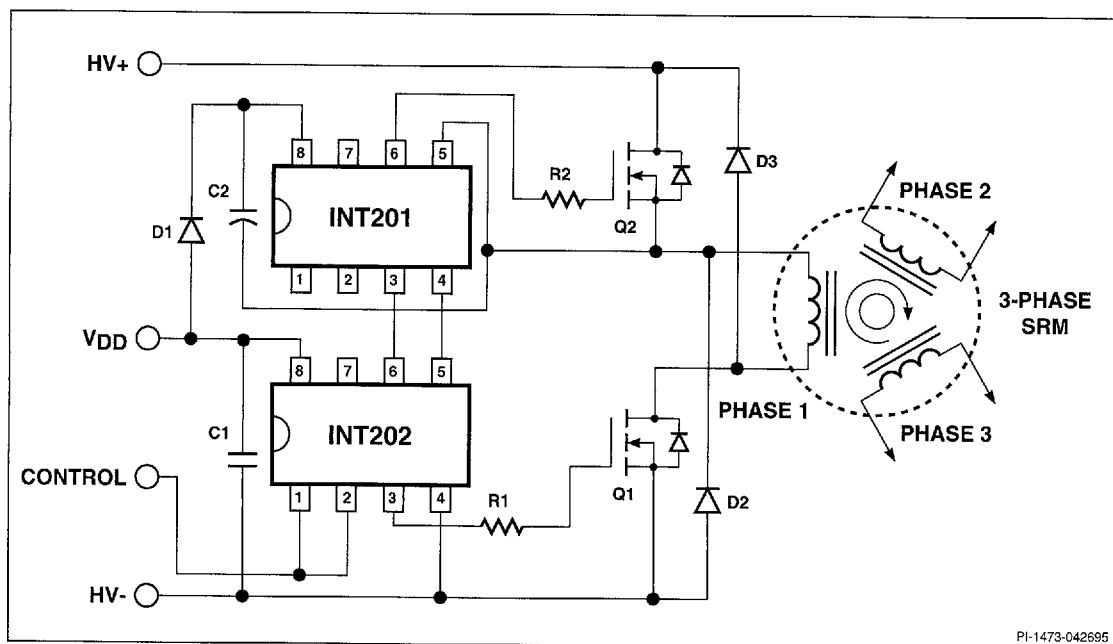


Figure 4. Using the INT202 and INT201 to Drive a Switched Reluctance Motor.

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## General Circuit Operation

The three-phase switched reluctance motor drive circuit shown in Figure 4 illustrates a typical application for the INT202/201. The LS IN signal directly controls MOSFET Q1. The HS IN signal causes the INT202 to command the INT201 to turn MOSFET Q2 on or off as required.

Local bypassing for the low-side driver is provided by C1. Bootstrap bias for the high-side driver is provided by D1 and C2. Slew rate and effects of parasitic oscillations in the load waveforms are controlled by resistors R1 and R2.

The inputs are designed to be compatible with 5 V CMOS logic levels and should not be connected to  $V_{DD}$ . Normal CMOS power supply sequencing should be observed. The order of signal application should be  $V_{DD}$ , logic signals, and then HV+.  $V_{DD}$  should be supplied from a low impedance voltage source.

The length of time that the high-side can remain on is limited by the size of the bootstrap capacitor. Applications with extremely long high-side on times require special techniques discussed in AN-10.

Maximum frequency of operation is limited by power dissipation due to high-

voltage switching, gate charge, and bias power. Figure 5 indicates the maximum switching frequency as a function of input voltage and gate charge. For higher ambient temperatures, the switching frequency should be derated linearly.

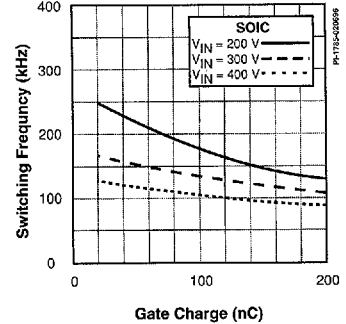
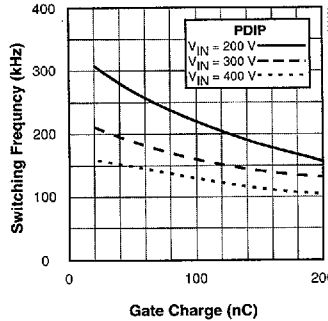


Figure 5. Switching Frequency versus Gate Charge for a) PDIP and b) SOIC.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

HSD1/HSD2 Voltage (1 Suffix) .....	600 V	Power Dissipation	PF Suffix ( $T_A = 25^\circ\text{C}$ ) .....	1.25 W
(2 Suffix) .....	800 V		PF Suffix ( $T_A = 70^\circ\text{C}$ ) .....	800 mW
HSD1/HSD2 Slew Rate .....	10 V/ns	TF Suffix ( $T_A = 25^\circ\text{C}$ ) .....	1.04 W	
$V_{DD}$ Voltage .....	16.5 V	TF Suffix ( $T_A = 70^\circ\text{C}$ ) .....	667 mW	
Logic Input Voltage .....	-0.3 V to 5.5 V	Thermal Impedance ( $\theta_{JA}$ )		
LS OUT Voltage .....	-0.3 V to $V_{DD} + 0.3$ V	PF Suffix .....	100°C/W	
Storage Temperature .....	-65 to 125°C	TF Suffix .....	120°C/W	
Ambient Temperature .....	-40 to 85°C	1. Unless noted, all voltages referenced to COM, $T_A = 25^\circ\text{C}$		
Junction Temperature .....	150°C	2. 1/16" from case for 5 seconds.		
Lead Temperature <sup>(2)</sup> .....	260°C			

Parameter	Symbol	Conditions (Unless Otherwise Specified) $V_{DD} = 15$ V, COM = 0V $T_A = -40$ to 85°C	Min	Typ	Max	Units
<b>LOGIC</b>						
Input Current, High or Low	$I_{IH}, I_{IL}$	$V_{IH} = 4.0$ V	0	10	150	$\mu\text{A}$
		$V_{IL} = 1.0$ V	-20	0	20	
Input Voltage High	$V_{IH}$		4.0			V
Input Voltage Low	$V_{IL}$				1.0	V
Input Voltage Hysteresis	$V_{HY}$		0.3	0.7		V
<b>HSD OUTPUTS</b>						
Breakdown Voltage	$BV_{DSS}$	1 Suffix	600	700		V
		2 Suffix	800	900		
Off-State Output Current	$I_{HSD(OFF)}$	$V_{HSD1}, V_{HSD2} = 500$ V		0.1	15	$\mu\text{A}$
On-State Output Current	$I_{HSD(ON)}$	$V_{HSD1}, V_{HSD2} = 10$ V	5	25		mA
On-State Pulse Width	$t_{HSD(ON)}$				156	ns
Output Capacitance	$C_{OSS}$	$V_{HSD1}, V_{HSD2} = 25$ V		10		pF



Parameter	Symbol	Conditions (Unless Otherwise Specified) $V_{DD} = 15\text{ V}$ , $COM = 0\text{V}$ $T_A = -40\text{ to }85^\circ\text{C}$	Min	Typ	Max	Units
<b>LS OUT</b>						
Output Voltage High	$V_{OH}$	$I_o = -20\text{ mA}$	$V_{DD}-1.0$	$V_{DD}-0.5$		V
Output Voltage Low	$V_{OL}$	$I_o = 40\text{ mA}$		0.3	1.0	V
Output Short Circuit Current	$I_{OS}$	See Note 1	$V_o = 0\text{V}$		-150	mA
			$V_o = V_{DD}$	300		
Turn-on Delay Time	$t_{d(on)}$	See Figure 6		0.6	1.0	$\mu\text{s}$
Rise Time	$t_r$	See Figure 6		80	120	ns
Turn-off Delay Time	$t_{d(off)}$	See Figure 6		0.5	1	$\mu\text{s}$
Fall Time	$t_f$	See Figure 6		50	100	ns
<b>SYSTEM RESPONSE</b>						
Matching (Low On to High On)	$Mt_{p+}$	See Figure 7		0.3	1	$\mu\text{s}$
Matching (Low Off to High Off)	$Mt_{p-}$	See Figure 7		0.3	1	$\mu\text{s}$
<b>UNDERVOLTAGE LOCKOUT</b>						
Input UV Trip-off Voltage	$V_{DD(UV)}$		8.5	9.0	10	V
Input UV Hysteresis			175	350		mV
<b>SUPPLY</b>						
Supply Current	$I_{DD}$	See Note 2		1.5	3.0	mA
Supply Voltage	$V_{DD}$		10		16	V

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**NOTES:**

1. Applying a short circuit to the LS OUT pin for more than 500  $\mu\text{s}$  will exceed the thermal rating of the package, resulting in destruction of the part.
2.  $V_{DD}$  supply must have less than 30  $\Omega$  output impedance.

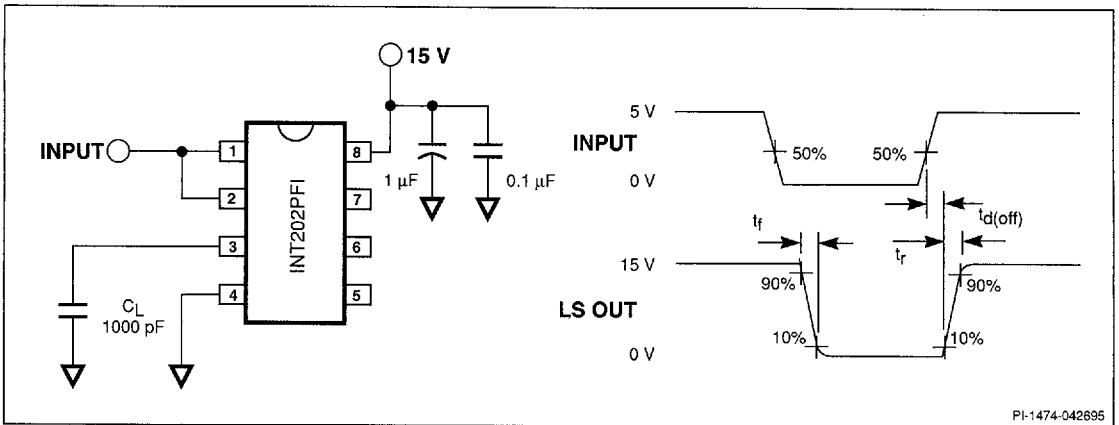


Figure 6. Switching Time Test Circuit.

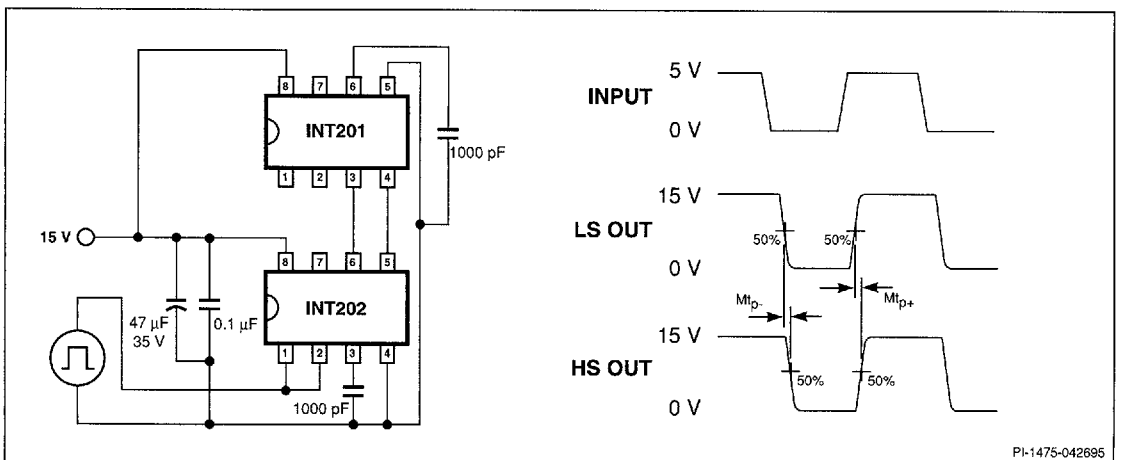
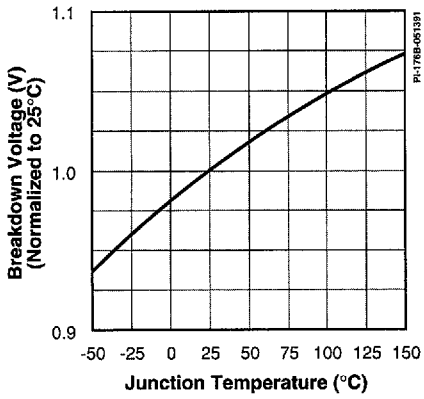


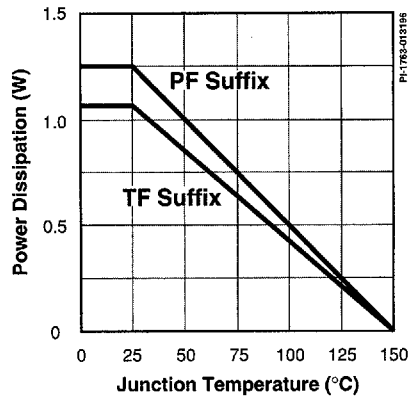
Figure 7. Matching Test Circuit.



**BREAKDOWN vs. TEMPERATURE**



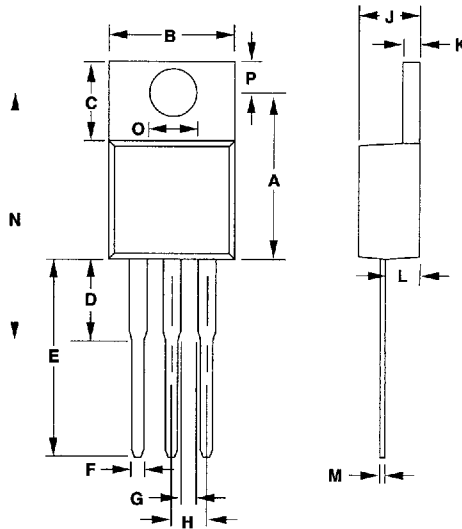
**PACKAGE POWER DERATING**



Y03A

Plastic TO-220/3

DIM	inches	mm
A	.460-.480	11.68-12.19
B	.400-.415	10.16-10.54
C	.236-.260	5.99-6.60
D	.240 - REF.	6.10 - REF.
E	.520-.560	13.21-14.22
F	.028-.038	.71-.97
G	.045-.055	1.14-1.40
H	.090-.110	2.29-2.79
J	.165-.185	4.19-4.70
K	.045-.055	1.14-1.40
L	.095-.115	2.41-2.92
M	.015-.020	.38-.51
N	.705-.715	17.91-18.16
O	.146-.156	3.71-3.96
P	.103-.113	2.62-2.87



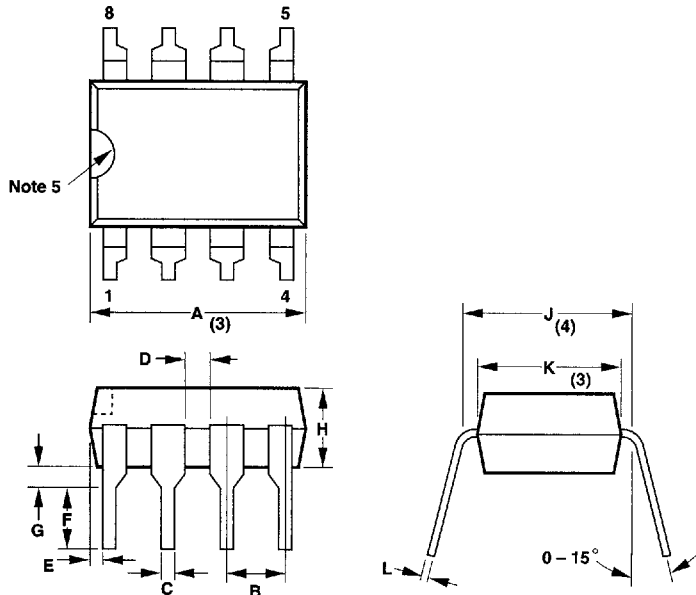
- Notes:
1. Package dimensions conform to JEDEC specification TO-220 AB for standard flange mounted, peripheral lead package; .100 inch lead spacing (Plastic) 3 leads (issue J, March 1987)
  2. Controlling dimensions are inches.
  3. Pin numbers start with Pin 1, and continue from left to right when viewed from the top.
  4. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15 mm) on any side.
  5. Position of terminals to be measured at a position .25 (6.35 mm) from the body.
  6. All terminals are solder plated.

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P08A

Plastic DIP-8

Dim.	inches	mm
A	.395 MAX	10.03 MAX
B	.090-.110	2.29-2.79
C	.015-.021	0.38-0.53
D	.040 TYP	1.02 TYP
E	.015-.030	0.38-0.76
F	.125 MIN	3.18 MIN
G	.015 MIN	0.38 MIN
H	.125-.135	3.18-3.43
J	.300-.320	7.62-8.13
K	.245-.255	6.22-6.48
L	.009-.015	0.23-0.38



- Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85).
  2. Controlling dimensions: inches.
  3. Dimensions are for the molded body and do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
  4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
  5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

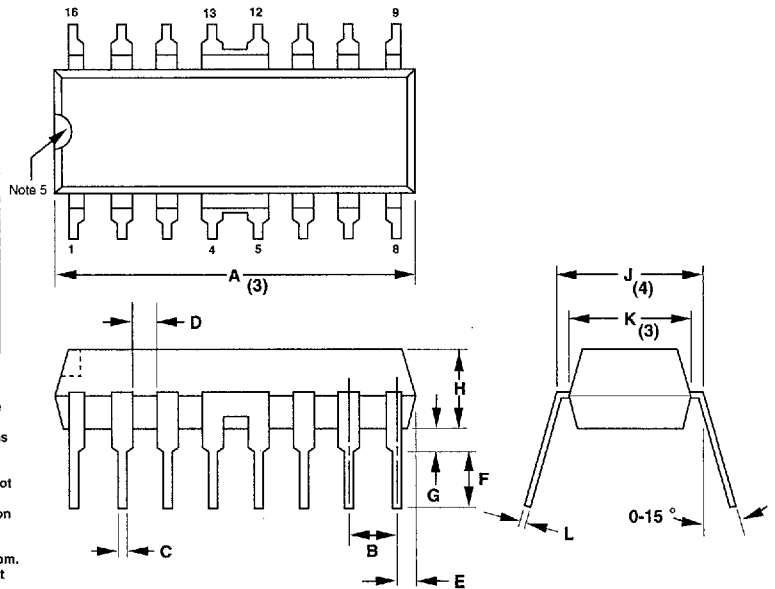
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**P16B**

**Plastic DIP-16**

DIM	Inches	mm			
A	.780 MAX	19.81 MAX			
B	.090-.110	2.29-2.79			
C	.015-.021	.38-.53			
D	.040 TYP	1.02 TYP			
E	.015-.030	.38-.76			
F	.125 MIN	3.18 MIN			
G	.015 MIN	.38 MIN			
H	.125-.135	3.18-3.43			
J	.300-.320	7.62-8.13			
K	.245-.255	6.22-6.48	L	.009-.015	.23-.38
L	.009-.015	.23-.38			



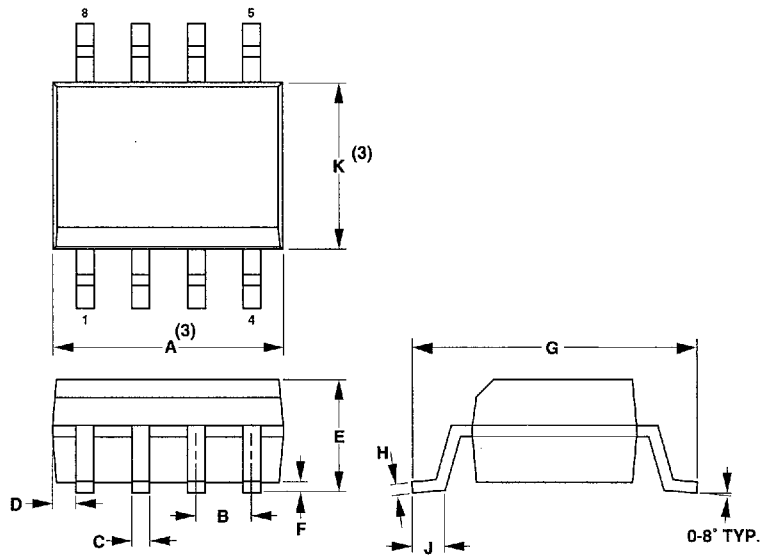
- Notes:
1. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (Issue B, 7/85). Except for joining of Pins 4-5 and Pins 12-13.
  2. Controlling dimension: inches.
  3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25 mm) on any side.
  4. These dimensions measured with the leads constrained to be perpendicular to package bottom.
  5. Pin 1 orientation identified by end notch or dot adjacent to Pin 1.

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**T08A**

**Plastic SO-8**

DIM	Inches	mm
A	0.189-0.197	4.80-5.00
B	0.050 TYP	1.27 TYP
C	0.014-0.019	0.35-0.49
D	0.012 TYP	0.31 TYP
E	0.053-0.069	1.35-1.75
F	0.004-0.010	0.10-0.25
G	0.228-0.244	5.80-6.20
H	0.007-0.010	0.19-0.25
J	0.021-0.045	0.51-1.14
K	0.150-0.157	3.80-4.00



- Notes:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75 mm (.150 inch) body width (Issue A, June 1985).
  2. Controlling dimensions are in mm.
  3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
  4. Pin 1 side identified edge by chamfer on top of the package body or indent on Pin 1 end.

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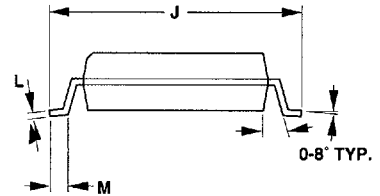
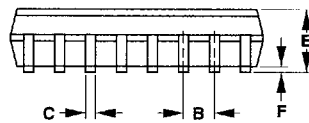
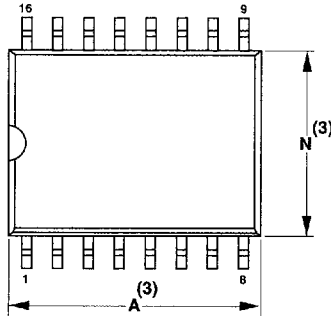
S16A

Plastic SO-16 (W)

DIM	Inches	mm
A	.398-.413	10.10-10.50
B	.050 BSC	1.27 BSC
C	.014-.018	0.36-0.46
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.418	10.01-10.62
L	.009-.012	0.23-0.32
M	.020-.040	0.51-1.02
N	.291-.299	7.40-7.60

Notes:

1. Package dimensions conform to JEDEC specification MS-013-AA for standard small outline (SO) package, 16 leads, 7.50 mm (.300 inch) body width (issue A, June 1985).
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.



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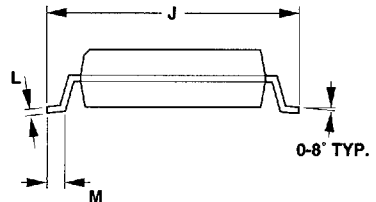
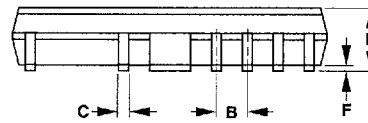
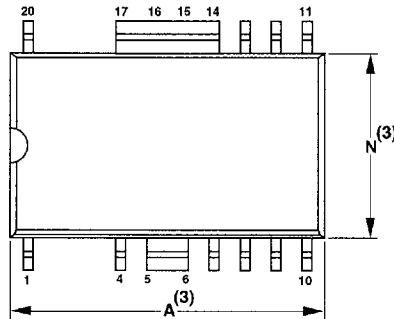
S20B

Plastic SO-20

DIM	Inches	mm
A	.496-.512	12.60-13.00
B	.050 BSC	1.27 BSC
C	.014-.019	0.35-0.49
E	.093-.104	2.35-2.65
F	.004-.012	0.10-0.30
J	.394-.419	10.00-10.65
L	.009-.013	0.23-0.32
M	.016-.050	0.40-1.27
N	.291-.299	7.40-7.60

Notes:

1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50 mm (.300 inch) body width (issue A, June 1985). Except for joining of Pins 5-6 and Pins 13-14-15.
2. Controlling dimensions are in mm.
3. Dimensions are for the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15 mm (.006 inch) on any side.
4. Pin 1 side identified by chamfer on top edge of the package body or indent on Pin 1 end.



PI-1847-050196



# Tape & Reel Ordering Information



Power Integrations, Inc. makes selected surface-mount parts available in tape and reel form for use with automatic pick-and-place equipment. Tape and reel specifications meet or exceed industry standard specification EIA-481.

## Ordering Information

Parts available in tape and reel form can be ordered by placing a T&R ordering suffix after the base part number. Standard orientation is Pin 1 Left. The ordering suffix for this orientation (see Figure 1) is TL. For example:

<b>Base Part #</b>	<b>T&amp;R Suffix</b>
INT100S	-TL

Please contact the factory for other options. Minimum order size is 1 reel per line item, and all orders will be in multiples of full reel quantities. The quantity per reel for each package type is shown in Table 1. Power Integrations normal terms and conditions apply.

## Electrical Specifications

Parts are subjected to the Power Integrations standard test flow, after which the parts are loaded into the tape cavities and sealed with a cover tape using standard anti-static handling procedures. The tape and cover are constructed of conductive modified polystyrene, providing a surface resistivity of  $\leq 10^6 \Omega/\text{square}$ . The reel is made of polystyrene with a topical anti-static coating, providing a surface resistivity of  $\leq 10^{11} \Omega/\text{square}$ .

## Physical Specifications

Physical specifications of the tape, cover, and reel are governed by EIA-481. Physical dimensions of the tapes are given in Figure 2 and Table 2, and physical dimensions of the reels are given in Figure 3 and Table 3.

## Packaging for Shipment

Power Integrations supplies the following information on the side of each reel for ease of product identification:

- Power Integrations part number (MPN), including orientation suffix
- Encapsulation date code (D/C)
- Assembly lot identification (LOT)
- Quantity (QTY)
- Tape and reel packing date code (R/D)

PACKAGE	TAPE		REEL DIA	REEL QTY
	WIDTH (W)	PITCH (P)		
SO-8	12mm	8mm	330mm	2500
SO-16 (W)	16mm	12mm	360mm	1000
SO-20	24mm	12mm	360mm	1000

Table 1. Primary Tape & Reel Dimensions and Reel Quantities.

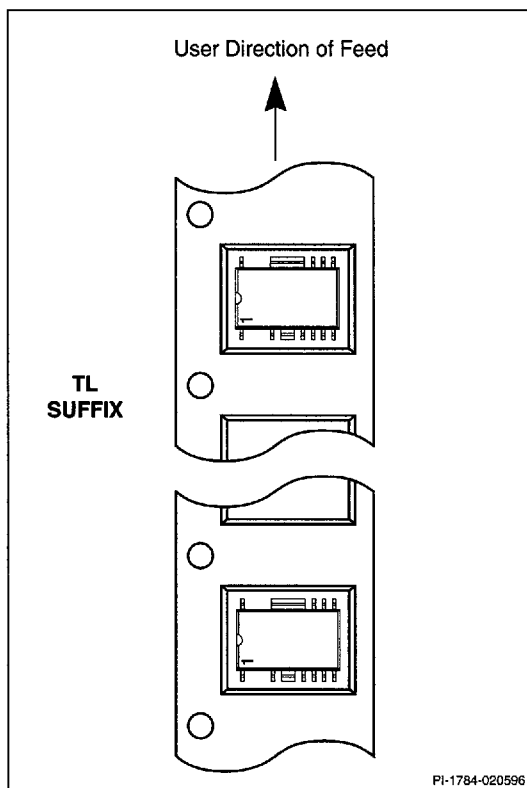


Figure 1. Part Orientation and Ordering Suffix.



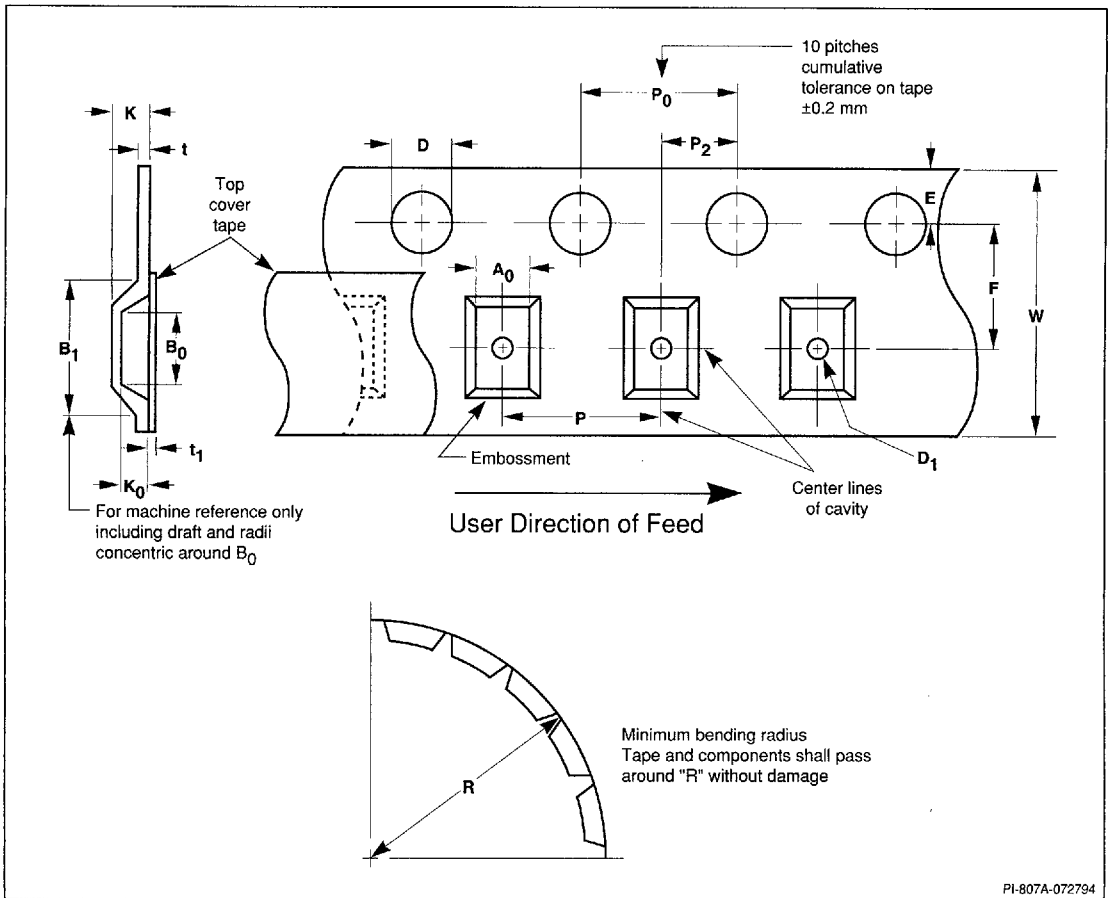


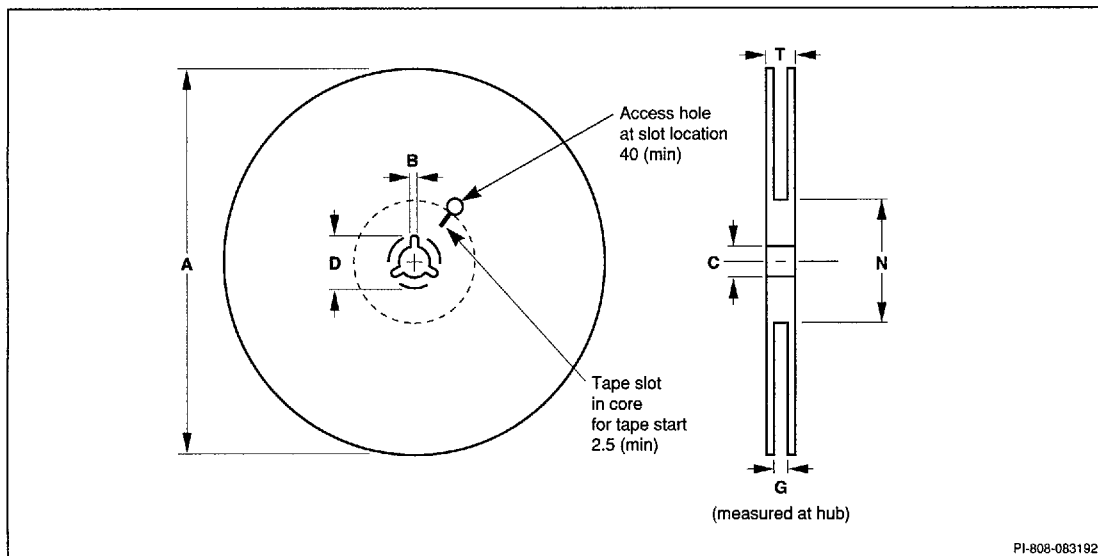
Figure 2. Tape Dimension Index.

Package Type	Tape Size	A <sub>0</sub>	B <sub>0</sub>	B <sub>1</sub>	D	D <sub>1</sub>	E	F	K
Plastic SO-8	12 mm	6.3-6.5	5.1-5.3	8.2 (max)	1.5-1.6	1.5 (min)	1.65-1.85	5.45-5.55	4.5 (max)
Plastic SO-16 (W)	16 mm	10.8-11.0	10.6-10.8	12.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	7.40-7.60	6.5 (max)
Plastic SO-20	24 mm	10.8-11.0	13.2-13.4	20.1 (max)	1.5-1.6	1.5 (min)	1.65-1.85	11.40-11.60	6.5 (max)

Package Type	Tape Size	K <sub>0</sub>	P	P <sub>0</sub>	P <sub>2</sub>	R	t	t <sub>1</sub>	W
Plastic SO-8	12 mm	2.00-2.20	7.9-8.1	3.9-4.1	1.95-2.05	30 (min)	0.400 (max)	0.10 (max)	11.7-12.3
Plastic SO-16 (W)	16 mm	2.90-3.10	11.9-12.1	3.9-4.1	1.90-2.10	40 (min)	0.400 (max)	0.10 (max)	15.7-16.3
Plastic SO-20	24 mm	2.90-3.10	11.9-12.1	3.9-4.1	1.90-2.10	50 (min)	0.400 (max)	0.10 (max)	23.7-24.3

Table 2. Tape Dimensions (in mm).





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Figure 3. Reel Dimension Index.

Package Type	Tape Size	A	B	C	D	G	N	T
Plastic SO-8	12 mm	330 (max)	1.5 (min)	12.80-13.20	20.2 (min)	12.4-14.4	50 (min)	18.4 (max)
Plastic SO-16 (W)	16 mm	360 (max)	1.5 (min)	12.80-13.20	20.2 (min)	16.4-18.4	50 (min)	22.4 (max)
Plastic SO-20	24 mm	360 (max)	1.5 (min)	12.80-13.20	20.2 (min)	24.4-26.4	50 (min)	30.4 (max)

Table 3. Reel Dimensions (in mm).

