



MOTOROLA

2N4851 thru 2N4853

SILICON ANNULAR UNIJUNCTION TRANSISTORS

... designed for pulse and timing circuits, sensing circuits, and thyristor trigger circuits.

- Low Peak-Point Current — $I_p = 0.4 \mu\text{A Max}$
- Low Emitter Reverse Current — $I_{EO} = 50 \text{ nA Max}$
- Fast Switching — 1.0 MHz Min

*MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|--------------------------------------|------------|-------------|------------------|
| RMS Power Dissipation (1) | P_D | 300 | mW |
| RMS Emitter Current | I_e | 50 | mA |
| Peak-Pulse Emitter Current (2) | i_e | 1.5 | Amp |
| Emitter Reverse Voltage | V_{B2E} | 30 | Volts |
| Interbase Voltage (3) | V_{B2B1} | 35 | Volts |
| Operating Junction Temperature Range | T_J | -65 to +125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +200 | $^\circ\text{C}$ |

* Indicates JEDEC Registered Data

(1) Derate 3.0 mW/ $^\circ\text{C}$ increase in ambient temperature.

(2) Duty cycle $\leq 1\%$, PRR = (see figure 6)

(3) Based upon power dissipation at $T_A = 25^\circ\text{C}$

FIGURE 1 — UNIJUNCTION TRANSISTOR SYMBOL AND NOMENCLATURE

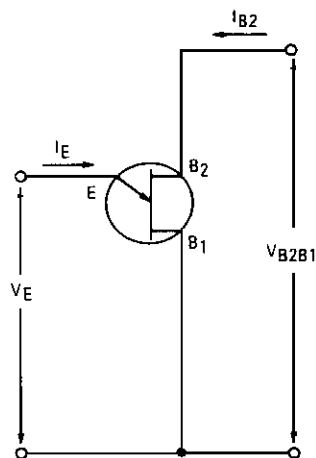
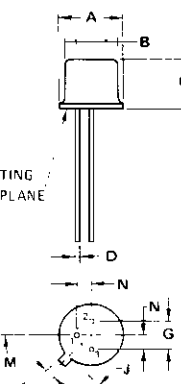
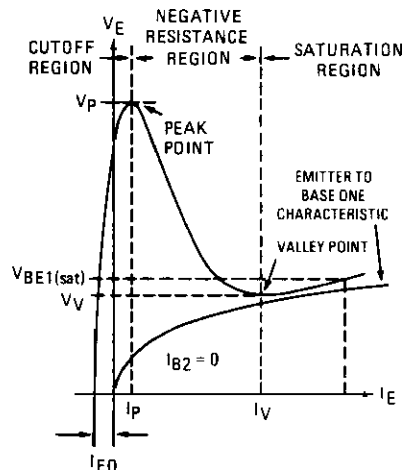


FIGURE 2 — STATIC EMITTER CHARACTERISTICS CURVES



| DIM | MILLIMETERS | | INCHES | |
|-----|-----------------|------|-----------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 5.31 | 5.84 | 0.209 | 0.230 |
| B | 4.52 | 4.95 | 0.178 | 0.195 |
| C | 4.32 | 5.33 | 0.170 | 0.210 |
| D | 0.41 | 0.48 | 0.016 | 0.019 |
| G | 2.54 TYP | | 0.100 TYP | |
| H | 0.91 | 1.17 | 0.036 | 0.046 |
| J | 0.71 | 1.22 | 0.028 | 0.048 |
| K | 12.70 | — | 0.500 | — |
| M | 45 $^\circ$ TYP | | 45 $^\circ$ TYP | |
| N | 1.27 TYP | — | 0.050 TYP | — |

CASE 22A

♦Annular Semiconductors Patented by Motorola Inc.

MOTOROLA Semiconductor Products Inc.



A SUBSIDIARY OF MOTOROLA INC

SI UNIJUNCTION TRANSISTORS
2N4851 thru 2N4853
DS 2502

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

| Rating | Figure No. | Symbol | Min | Typ | Max | Unit |
|---|------------|-----------------------|-------------------|-------------|--------------|--------|
| * Intrinsic Standoff Ratio (1) (V _{B2B1} = 10 V) 2N4851 2N4852, 2N4853 | 4, 8 | η | 0.56 0.70 | — — | 0.75 0.85 | — |
| * Interbase Resistance (V _{B2B1} = 3.0 V, I _E = 0) | 11, 12 | r _{BB} | 4.7 | — | 9.1 | k ohms |
| * Interbase Resistance Temperature Coefficient (V _{B2B1} = 3.0 V, I _E = 0, T _A = -65 to +125°C) | 12 | α _{BB} | 0.2 | — | 0.8 | %/°C |
| Emitter Saturation Voltage (2) (V _{B2B1} = 10 V, I _E = 50 mA) | | V _{EB1(sat)} | — | 2.5 | — | Volts |
| Modulated Interbase Current (V _{B2B1} = 10 V, I _E = 50 mA) | | I _{B2(mod)} | — | 15 | — | mA |
| * Emitter Reverse Current (V _{B2E} = 30 V, I _{B1} = 0) 2N4851, 2N4852 2N4853 | 7 | I _{EB2O} | — — | — — | 0.1 0.05 | μA |
| * Peak-Point Emitter Current (V _{B2B1} = 25 V) 2N4851, 2N4852 2N4853 | 9, 10 | I _P | — — | — — | 2.0 0.4 | μA |
| * Valley-Point Current (2) (V _{B2B1} = 20 V, R _{B2} = 100 ohms) 2N4851 2N4852 2N4853 | 13, 14 | I _V | 2.0 4.0 6.0 | — — — | — — — | mA |
| * Base-One Peak Pulse Voltage 2N4851 2N4852 2N4853 | 3, 17 | V _{OB1} | 3.0 5.0 6.0 | — — — | — — — | Volts |
| * Maximum Frequency of Oscillation | 5 | f _(max) | 1.0 | 1.25 | — | MHz |

* Indicates JEDEC Registered Data.

(1) η, Intrinsic standoff ratio, is defined in terms of the peak-point voltage, V_P, by means of the equation: V_P = η V_{B2B1} + V_F, where V_F is about 0.49 volt at 25°C, I_F = 10 μA and decreases with temperature at about 2.5 mV/°C. The test circuit is shown in Figure 4. Components R₁, C₁, and the UJT form a relaxation oscillator; the remaining circuitry serves as a peak-voltage detector. The voltage drop of Diode D₁ compensates for V_F. To use, the "cal" button is pushed, and R₃ is adjusted to make the current meter, M₁, read full scale. When the "cal" button is released, the value of η is read directly from the meter, if full scale on the meter reads 1.0

(2) Use pulse techniques: PW ≈ 300 μs, duty cycle ≤ 2.0% to avoid internal heating, which may result in erroneous readings.

FIGURE 3 — V_{OB1} TEST CIRCUIT

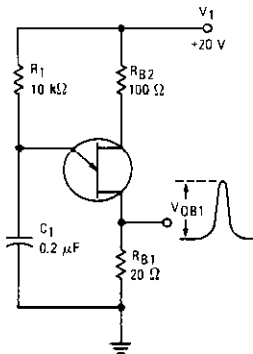


FIGURE 4 — η TEST CIRCUIT

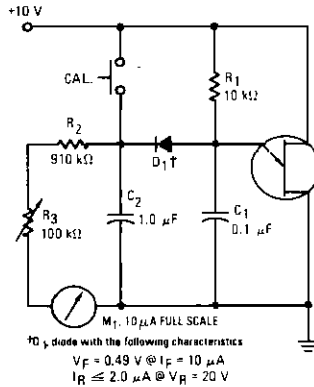


FIGURE 5 — f_(max) TEST CIRCUIT

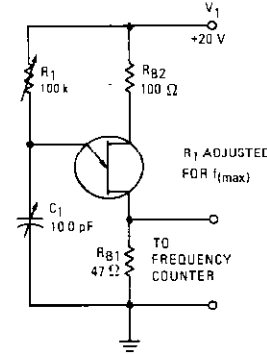
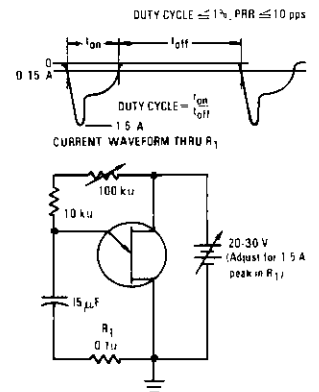
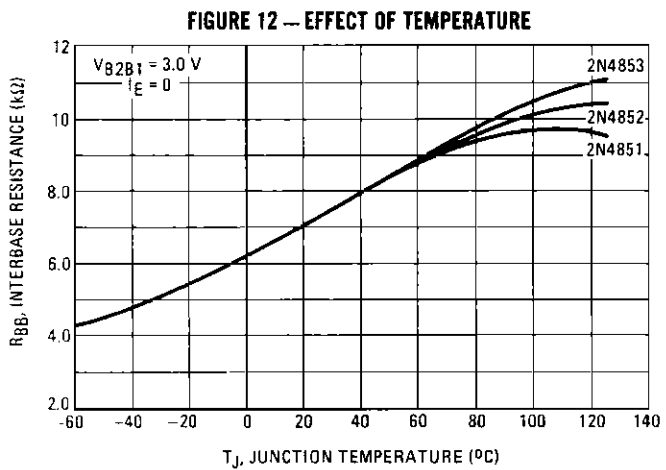
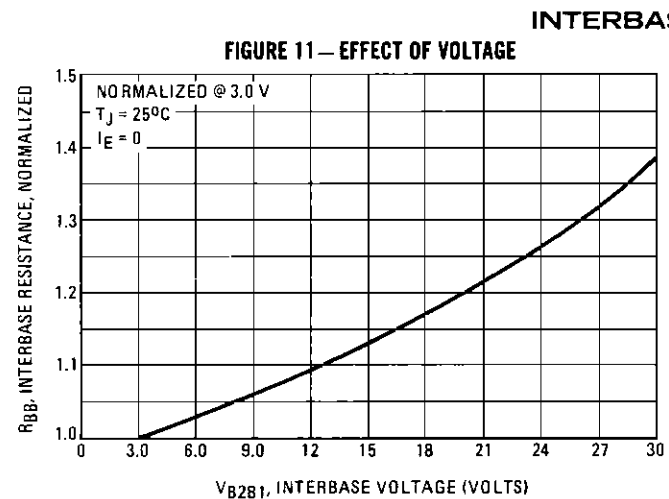
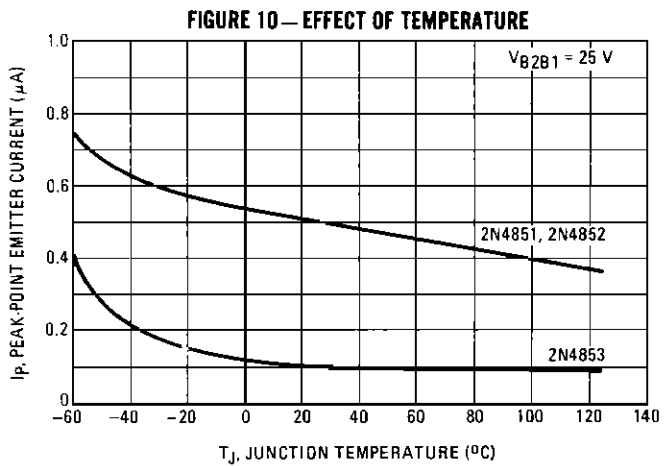
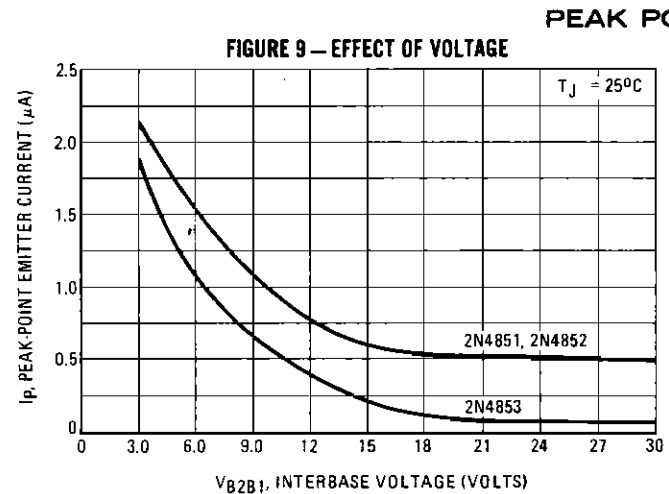
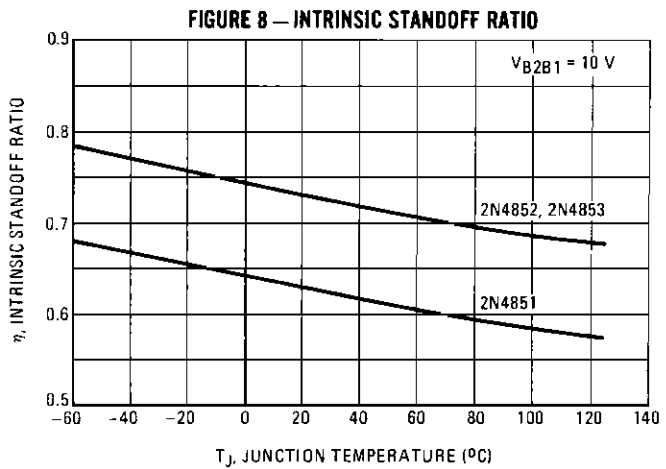
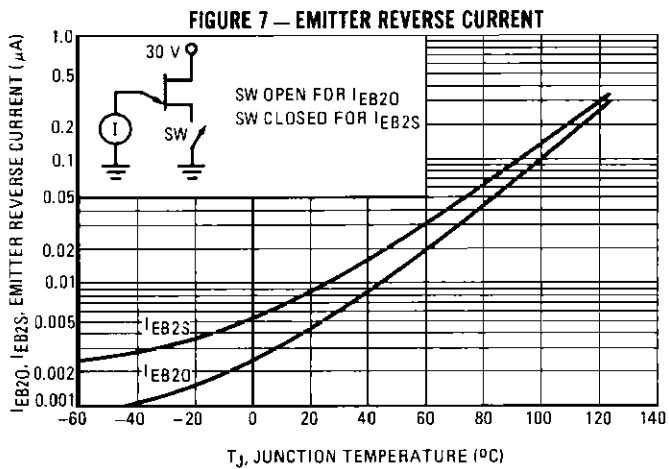


FIGURE 6 — PRR TEST CIRCUIT AND WAVEFORM



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

VALLEY CURRENT

FIGURE 13 — EFFECT OF VOLTAGE

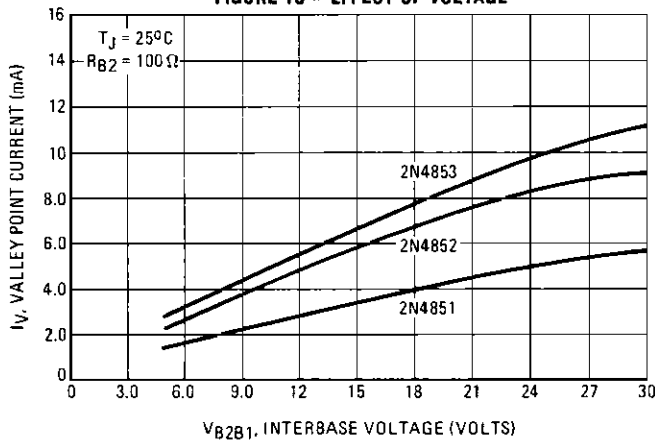
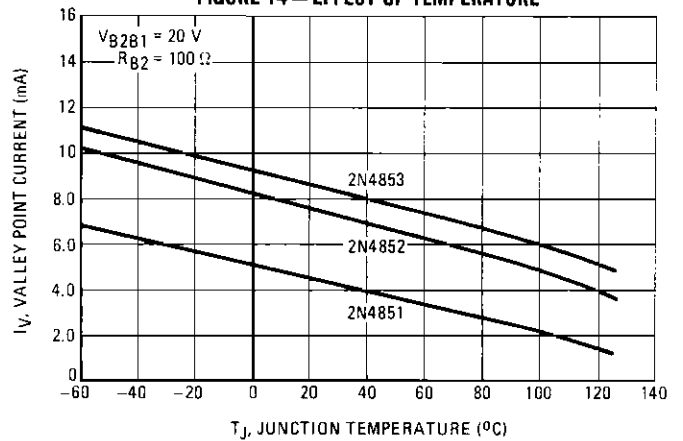


FIGURE 14 — EFFECT OF TEMPERATURE



VALLEY VOLTAGE

FIGURE 15 — EFFECT OF VOLTAGE

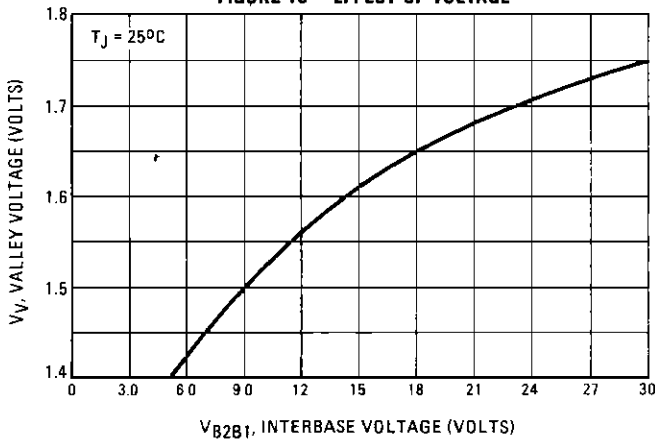


FIGURE 16 — EFFECT OF TEMPERATURE

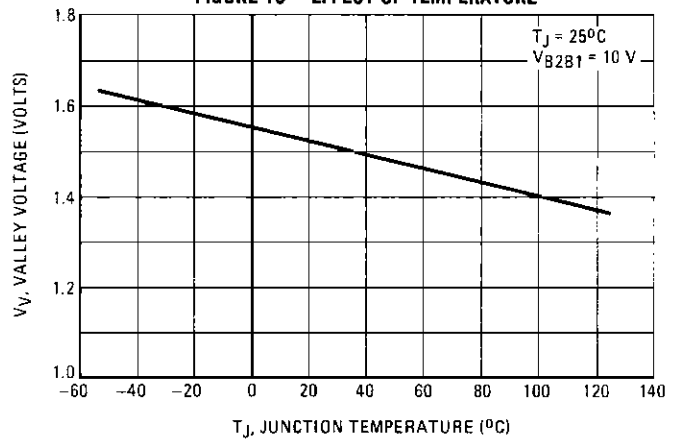
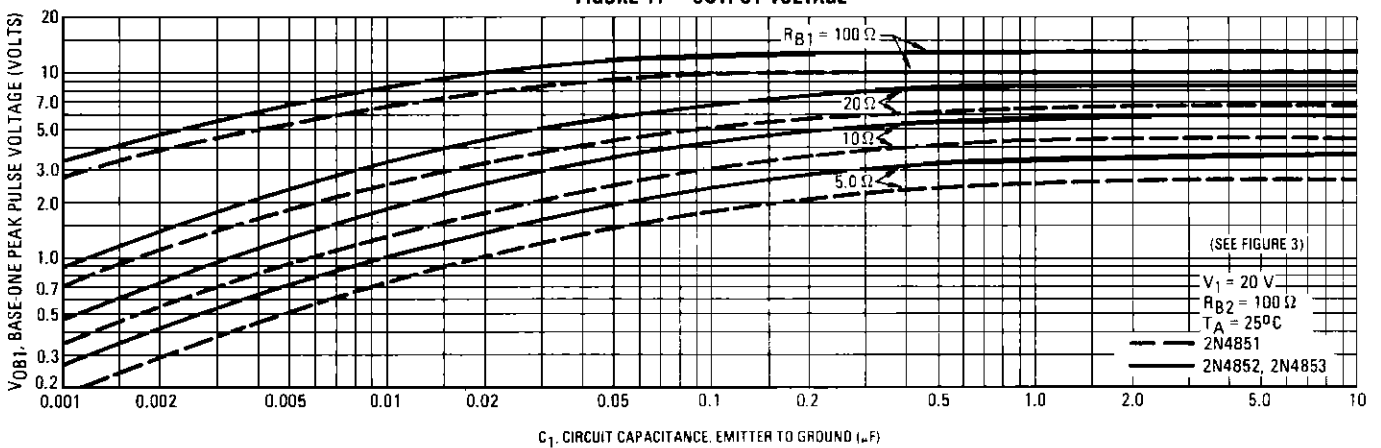



FIGURE 17 — OUTPUT VOLTAGE



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