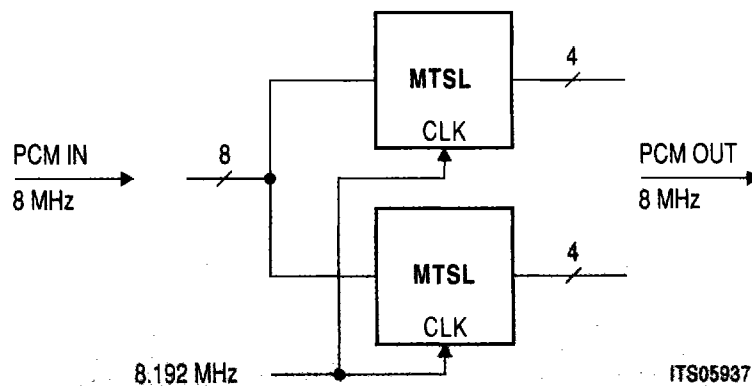


**Features**

- Time/space switch for 2048-, 4096- or 8192-kbit/s PCM systems
- Different modes programmable for input and output separately 2048 kbit/s (4096 kbit/s, 8192 kbit/s or mixed mode)
- Switching of up to 1024 incoming PCM channels to up to 5124 outgoing PCM channels
- Configurable for a 4096-kHz or 8192-kHz device clock 16 input and 8 output PCM lines
- Constant frame delay for switching of wideband data, e.g. ISDN H-channels or minimized delay for voice applications
- Tristate function for further expansion and tandem operation
- $\mu$ P read access to PCM data
- Programmable clock shift with half clock step resolution for input and output
- Individual line delay measurement and clock shift mechanism for 8 PCM inputs
- Built-in selftest
- 8-bit Motorola or Intel type  $\mu$ P interface
- Advanced low power 1  $\mu$ -CMOS technology
- Single 5-V-power supply

Type	Package
PEB 2047-N	P-LCC-44-1 (SMD)



**General Description**

The MTSL PEB 2047 is a memory time switch device. Operating with a device clock of 4096 kHz or 8192 kHz it can connect any of 1024 PCM-input channels to any of 512 output channels.

The input information of a complete frame is stored in the on-chip 8-kbit data memory DM. The incoming 1024 channels of 8 bits each are written in sequence into fixed positions in the DM. This is controlled by the input counter in the timing control block with an 8-kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the data memory. The byte in this data memory location is transferred into the current output time-slot. The read access of the CM is controlled by an output counter.

The synchronization of this procedure will be achieved by a rising edge of the synchronizing pulse SP, which is always sampled with the falling edge of the device clock.

Different modes of operation are configurable at the PCM-input interface. Also, 8 PCM-input lines can be synchronized with individual clock shift values to compensate different line delays. If more than 8 inputs are used one clock shift value controls up to two ports at the same time.

The input lines IN8 to IN15 can be used as additional frame-synchronization inputs FS. After synchronizing the device by the SP pulse, the FS inputs can be evaluated on a per port basis. This evaluation procedure is started by a

microprocessor command. As a result the input countervalue on the rising edge of the FS signal can be read from an internal register. Thus delay compensation is easily managed by programming appropriate clock shift values and/or a possible software offset.

During operation of the chip, a frame length check, which controls correct synchronization by the SP pulse and generates an interrupt in case of lost or achieved synchronization is also supplied.

The standard 8-bit  $\mu$ P interface can communicate with Intel multiplexed/demultiplexed microprocessors as well as with Motorola demultiplexed processors. It gives access to the internal registers and to the control – and data memory. Five directly addressable registers are provided. All other registers and the memories are accessed by a simple three byte indirect access method (similar to the MTSC PEB 2045).

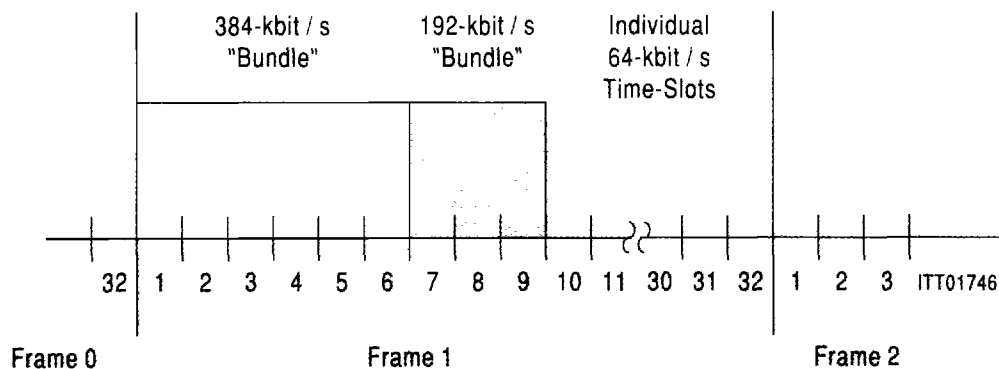
The switching path of the MTSL including input buffer, data memory, control memory, output buffer and timing control can be tested in the system by a built-in selftest. After activating this mechanism it takes 1.25 ms (8192 kHz) until the result "selftest ok/selftest not ok" can be read from the internal status register.

After test completion the control-memory is also reset.

In applications where 64-kbit/s channels are combined for higher data rates (e.g. ISDN H-channels) the MTSL ensures that all switched time-slots are output in the same frame.

In voice applications where a low delay is important, the MTSL can be programmed for minimized switching delays.

Wideband Switching of 64-kbit / s Time-Slots



**Data "Bundle":**  
 - switched time-slots have to be output in the same frame