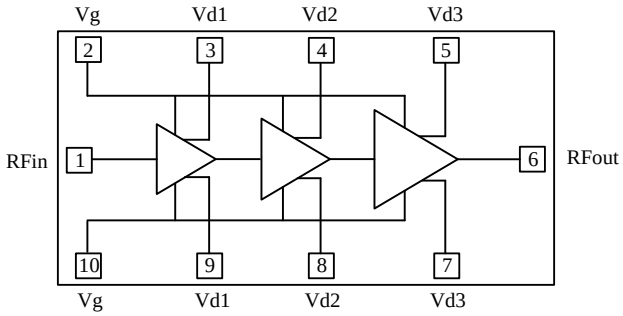
Feature

- Frequency：8.5GHz～10.5GHz
- Power Gain：19dB
- Psat：47dBm
- PAE：41%
- +28V@2.2A(Quiescent)
- Dimension：4.00mm×5.15mm×0.08mm

Function Diagram



DC Electrical Specification

Parameter	Min	Typical	Max	Unit
Vg	-2.4	-2.0	-1.6	V
Vd	-	28	-	V
Id	-	2.2	-	A
Idd	-	4.3	4.6	A
Igg	-	5	20	mA

Microwave Electrical Specification（T_A = +25℃，Vd = +28V，Vg = -1.8V）

Parameter	Min	Typical	Max	Unit
f	8.0～10.5			GHz
Psat	46.8	47.1	-	dBm
Gp	18.8	19.1	-	dB
ΔGp	-	-	±0.5	dB
PAE	38	41	-	%
Gain	23	28	33	dB
ΔGain	-	-	±2	dB
VSWR(in)	-	1.8	2.5	-

Note ： 1）The chip should be 100% DC and RF tested.

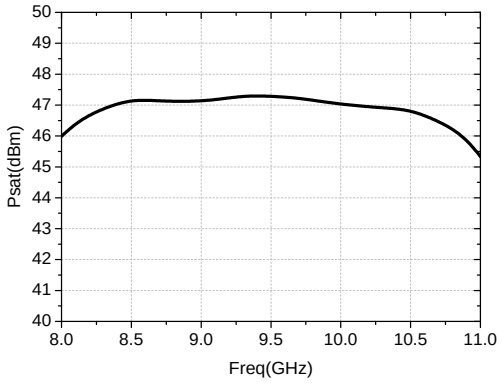
2）Test Condition：Vg=-2.0V，P_{in}=28dBm，Vd=+28V，CW

Max Limited Values

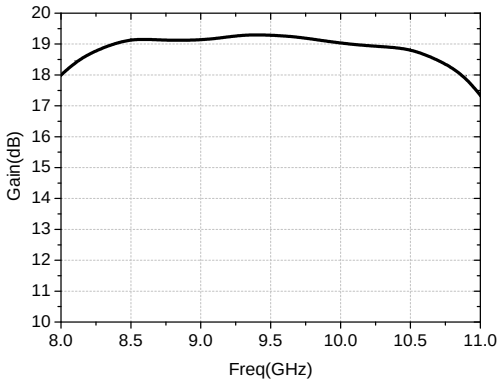
Parameter	Symbol	Values
Max Vd	Vd	+36V
Max Vg	Vg	-3V
Max Pin（CW）	P_p	+33dBm
Storage Temperature	T_{STG}	-65℃～+150℃
Max Operation Channel Temperature	T_{op}	+150℃
Load Impedance Mismatch （resistance to burn）	Z_0	5:1

Typical Test Curves（Vd=+28V，Vg=-2.0V）

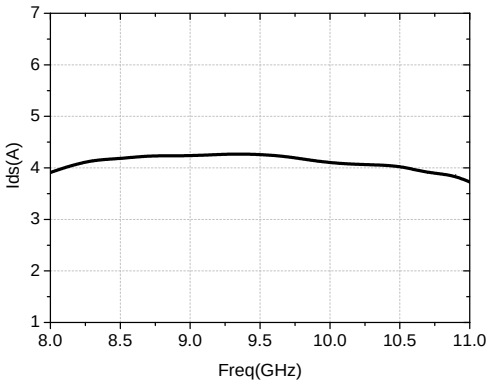
Psat / Effieciency vs. Frequency（P_{in}=28dBm）



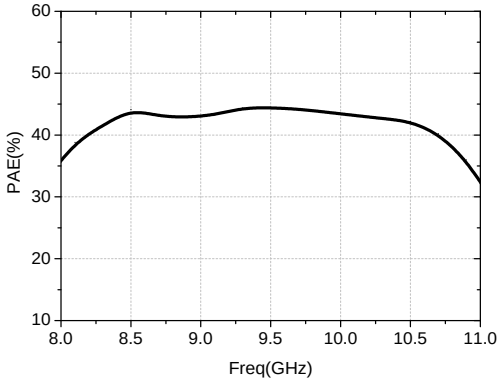
Power Gain vs. Freqneucy（P_{in}=28dBm）



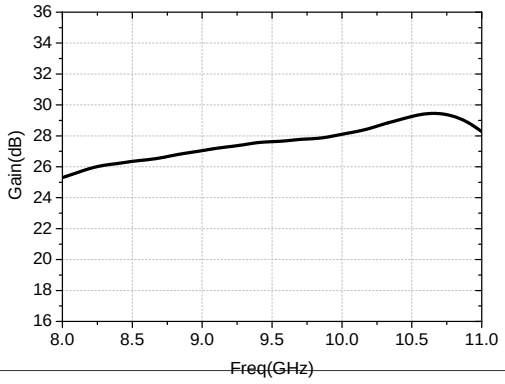
Ids vs. Frequency



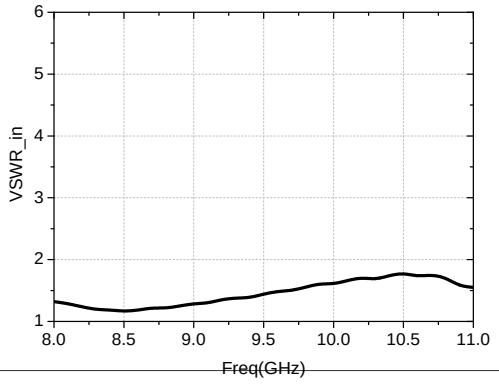
PAE vs. Frequency



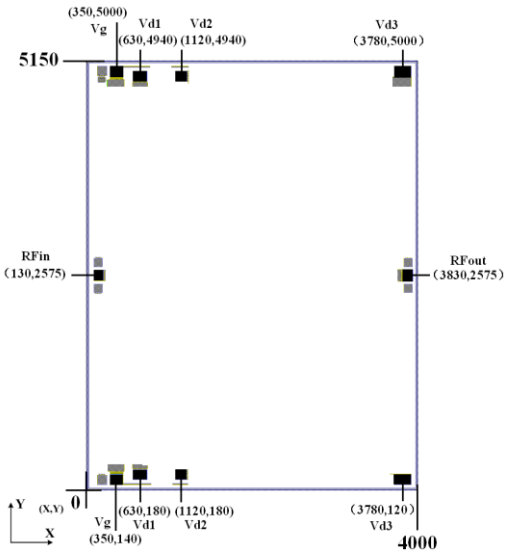
Small Signal Gain vs. Frequency（P_{in}=-10dBm）



VSWRin vs. Freqency（P_{in}=-10dBm）



Outline and Dimension



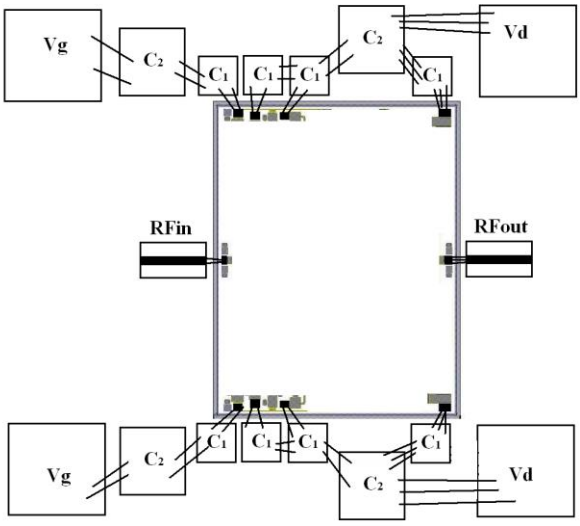
Pad Diagram

Pad No.	Symbol	Function	Dimension
1	RFin	Input Pad	100×120μm^2
2，10	Vg	Vg bonding pad	150×120μm^2
3，9	Vd1	Vd bonding pad	160×120μm^2
4，8	Vd2	Vd bonding pad	140×120μm^2
5，7	Vd3	Vd bonding pad	220×120μm^2
6	RFout	Output Pad	120×140μm^2

Note：All units should be in μm.

Dimension Tolerance: ±100μm

Assembly Diagram



Note: 1) Externally capacitor C1 = 100pF, C2 = 1000pF. It is recommended to use single-layer ceramic capacitors, where C1 should be as close as possible to the chip, please do not to exceed 750μm.

2) Ku band and below Ku band can be used power circuit microstrip line with 200μm ~ 300μm thick ceramic sintered on the carrier, the assembly process should be simplified. Ku Band and above Ku band can be used low dielectric constant material microstrip line with 125μm ~ 250μm bonding / sintering on the carrier to reduce transmission loss, input and output bonding wire length should be controlled within 350μm ± 150μm.

Attention

1） MMIC should be stored in a dry and clean N2 environment;

2） Chip Substrate GaN material is very brittle, must be used carefully, so as not to damage the chip;

3） There is no insulation layer on the chip surface, please pay attention to the cleanliness of the assembly environment to avoid excessive surface contamination;

4） The thermal expansion coefficient of the carrier should be close to that of the GaAs material with a linear thermal expansion coefficient of 4.2 × 10-6 / ℃. It is recommended that the carrier material be CuMoCu or CuMo or CuW.

5） When assembling the chip and the carrier should avoid the hole, at the same time, guarantee the good radiating of the case and the carrier;

6） It is recommended to use gold-tin solder to sinter, Au: Sn = 80%: 20%, the sintering temperature does not exceed 300 ℃, the time is not longer than 30 seconds, sintering process to avoid rapid changes in temperature,

7） It is recommended to use gold wire with a diameter of 25μm ~ 30μm. The temperature of bonding table chassis should not exceed 250 ℃. The bonding time should be as short as possible. The bonding process should avoid rapid changes of temperature.

8） When power on, please turn on Vg first and then Vd, when power down, drop Vd first and then Vg.

9） The chip has a DC blocking capacitor input and output, but the input port has the DC ground short circuit structure;

10） Chip use, anti-static in the assembly process, wearing anti-static grounding bracelet, sintering, bonding well grounding;

11） Available QF087-type metal-ceramic tube package products;

12） Please contact the supplier for any problem.

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