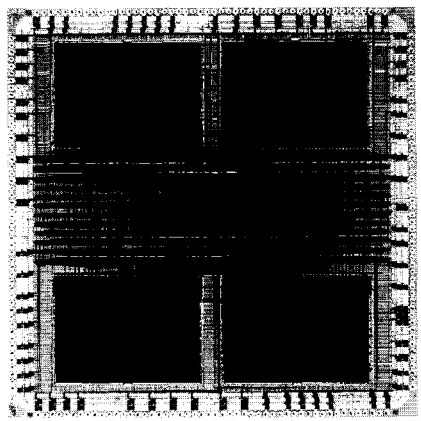
L64212 Variable-Length Video Shift Register (HVSR)

LSI LOGIC

Description

The L64212 is a high-speed variable-length video shift register. This device can be used individually or as video line delays for the L64200 family of processors. The delay of the L64212 can be set to any value between 11 and 4140. The L64212 features fully static operation and 40 MHz data rates. The L64212 can be operated in a circular buffer mode, in which the buffer is filled once and then read continuously.

The L64212 has four delay elements each with a maximum delay of 1035. Two data inputs allow operation in 18-bit applications with delays up to 2070 or as two independent 9-bit line delays. The L64212 is packaged in a 95-pin grid array.



L64212 Chip

Features

- Variable-length video shift register
- Acts as a variable-length line delay, reformatting serial (raster-scanned video) data into a two-dimensional video signal for image processing
- Contains four separate 9-bit shift registers whose length can be varied from 11 to 1035
- Programmable for any delay value between 11 and 4140
- High data rates

Commercial	Military
40 MHz	40 MHz
30 MHz	30 MHz

- Variable-length circular buffer
- 3-state outputs for double-buffered memories
- Available in 95-pin CPGA (Ceramic Pin Grid Array) package

Pin Listing and Description

DI0
9-bit input data bus. Data inputs are loaded into the first stage of the first shift register at the rising edge of CLK while SHIFT/HOLD is HIGH.

DI1
9-bit input data bus. Data inputs are loaded into the first stage of the third shift register at the rising edge of CLK while SHIFT/HOLD is HIGH. Only active when internal control signal 2inp is HIGH.

CLK
System clock (when SELCLK is LOW), active at the rising edge.

WCLK
System clock (when SELCLK is HIGH), active at the rising edge. Used to load circular buffer.

SELCLK
Selects either CLK (when LOW) or WCLK (when HIGH) as system clock.

SRWE
Enables writing of data into the shift registers. Held HIGH for line delay applications and during loading in circular buffer applications. Held LOW during reading in circular buffer applications.

CI.0 to CI.7
Control input bus. This bus is common to all L64200 series devices. On the L64212, the bus is used to load the length of each of the delay elements and other control information.

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Pin Listing and Description (Continued)

$\overline{WE}$
Active-LOW write enable for the CI inputs. When $\overline{WE}$ is LOW, new data is written into the register specified by the address on the REGADR pins.

REGADR.0 to REGADR.1
Control register address. Determines which of the control registers will be loaded with the data on CI when $\overline{WE}$ goes LOW.

SHIFT/$\overline{HOLD}$
Disables the action of the CLK input when LOW. When SHIFT/$\overline{HOLD}$ is connected to the horizontal blanking signal in a video system, data will not be loaded during the horizontal blanking period. SHIFT/$\overline{HOLD}$ must be asserted for a multiple of 4 cycles. Failing to meet this requirement results in unreliable data output.

DOX.Y
Data output buses where X and Y represent the output bus numbers and bit numbers, respectively. The L64212 has four 9-bit output buses, DO0.0–DO0.8, DO1.0–DO1.8, DO2.0–DO2.8, DO3.0–DO3.8.

OUTEN
Enables data output 3-state buffers when HIGH. DO0–DO3 go to a high-impedance state when OUTEN is LOW. OUTEN should be LOW when the outputs of another L64212 have been wired in parallel and are driving the output buses or when driving the bidirectional lines of the L64240 before the L64240 has been initialized.

$\overline{RESET}$
Sets the internal shift registers to access the first data element. Used to initialize the circular buffer pointer before loading data. Normally held HIGH.

Pin Description Summary

Pin	No. of Pins	I/O	Description
DI0.0–DI0.8 DI1.0–DI1.8	18	I	2* 9 bit inputs
DO0.0–DO0.8 DO1.0–DO1.8 DO2.0–DO2.8 DO3.0–DO3.8	36	O	4* 9 bit outputs
CI.0–CI.7	8	I	Control input bus
REGADR.0– REGADR.1	2	I	Control register address
CLK	1	I	System clock
WCLK	1	I	System clock
SELCLK	1	I	Selects between CLK and WCLK
$\overline{WE}$	1	I	Active-LOW write enable for CI inputs
SHIFT/$\overline{HOLD}$	1	I	Disables clock
OUTEN	1	I	Enables output 3-state buffers
$\overline{RESET}$	1	I	Sets internal registers to select first element

L64212
Variable-Length Video Shift Register (HVSR)

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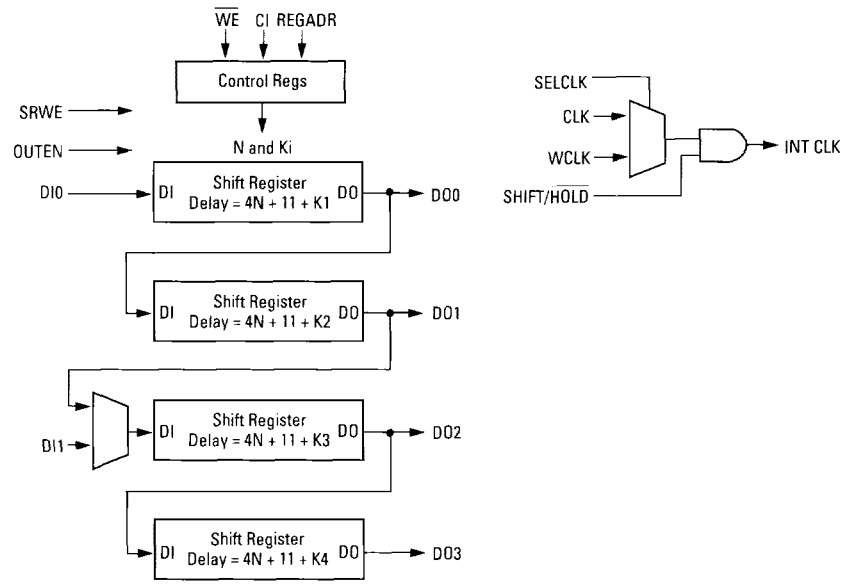
Block Diagram



Architecture

The L64212 contains four individual 9-bit variable-length shift registers which can be used as video line delays. The length of each shift register is controlled by the values residing in the level-triggered control registers. The length of each of the four shift registers can be varied from 11 to 1035 bit according to:

Number of Shifts = (4 • N) + 11 + Ki

Where $0 \leq N \leq 255$ and $0 \leq Ki \leq 4$, N is the same for all four shift-registers but there are four different K values. Having a different value of K for each shift register makes it possible to achieve single-cycle delay resolution even when multiple shift-registers are cascaded.

The values of N and Ki are determined by the following equations.

Desired Delay (D)	N	K	Number of Outputs
11–1035	D–11 4	all Ki = (D–11) mod 4	4
1036–2070	D–22 8	K1 + K2 = (D–22) mod 8 K3 + K4 = (D–22) mod 8	2
2071–4140	D–44 16	K1 + K2 + K3 + K4 = (D–44) mod 16	1

For larger delays, several L64212s can be connected in cascade.

The device has two independent 9-bit data inputs. This allows the device to be used as two independent 9-bit shift registers with delays up to 2070, one 18-bit shift register with a delay of up to 2070 or one 9-bit shift register with delays up to 4140. The internal control bit 2inp controls whether one or both of the inputs is active. If 2inp is LOW then only DI0 is active.

In video or image processing systems, the length of each shift register is normally set to the number of pixels per video line. When used in this fashion (as a video line delay or as a front end to any of the LSI Logic real-time image-processing chips), the line delay outputs the pixels vertically adjacent to (in the same column as) the input pixel.

To accommodate the blanking periods of a standard video signal (which contain no video data), the shift register can be deactivated during the horizontal blanking periods by tying SHIFT/$\overline{\text{HOLD}}$ to the horizontal blanking signal. This disables the clock, thus disabling data input into the chip.

Circular Buffer Mode

The L64212 can be operated as a circular buffer with a length of 4N + 4 up to a maximum of 1024. In this mode the user loads data into the shift register once. This data is subsequently read out repeatedly in the same order in which it was written. Data can be loaded in at a lower rate than the normal system clock, if desired. Holding SELCLK HIGH selects WCLK rather than CLK as the clock on which data is read in. If the data is to be read in and out at the same rate, then SELCLK should be held LOW and CLK used for both operations. In this mode, all Ki should be set to zero at initialization. First, the RESET signal is brought LOW and SWRE is set HIGH. Five cycles later, the user begins placing the data on the DI0 bus. The data is loaded in the order that it is to appear at the output, starting with the 4N + 4 data values to appear on the DO3 outputs, followed by the data values to appear on the DO2 and DO1 outputs and ending with the 4N + 4 data values to appear on the DO0 outputs. Each block of 4N + 4 data values is separated by seven cycles.

After all data has been loaded and four additional cycles are completed, SRWE and SELCLK are set LOW. Now the data in each buffer will be read out in a circular order and will change on the rising edge of CLK. Setting SHIFT/HOLD LOW will cause the data to hold at the output.

The above description assumes that the internal control signal, 2inp, is LOW. If 2inp is HIGH, then data will be loaded simultaneously over the DI0 and DI1 inputs, with data on the DI0 input eventually appearing on the DO0 and DO1 outputs and with data on the DI1 input appearing on the DO2 and DO3 outputs.

Before operation as a circular buffer or shift register can begin, the operation of the L64212 must be specified by loading control parameters into the control registers. Data on the CI bus is loaded into the register with address specified on the REGADR pins when WE is LOW. A control memory map is shown in the following table.

REGADR	CI.7	CI.6	CI.5	CI.4	CI.3	CI.2	CI.1	CI.0
0	N.7	N.6	N.5	N.4	N.3	N.2	N.1	N.0
1	K4.1	K4.0	K3.1	K3.0	K2.1	K2.0	K1.1	K1.0
2	–	–	–	2inp	L4	L3	L2	L1
3	–	–	–	–	–	–	–	PDWN

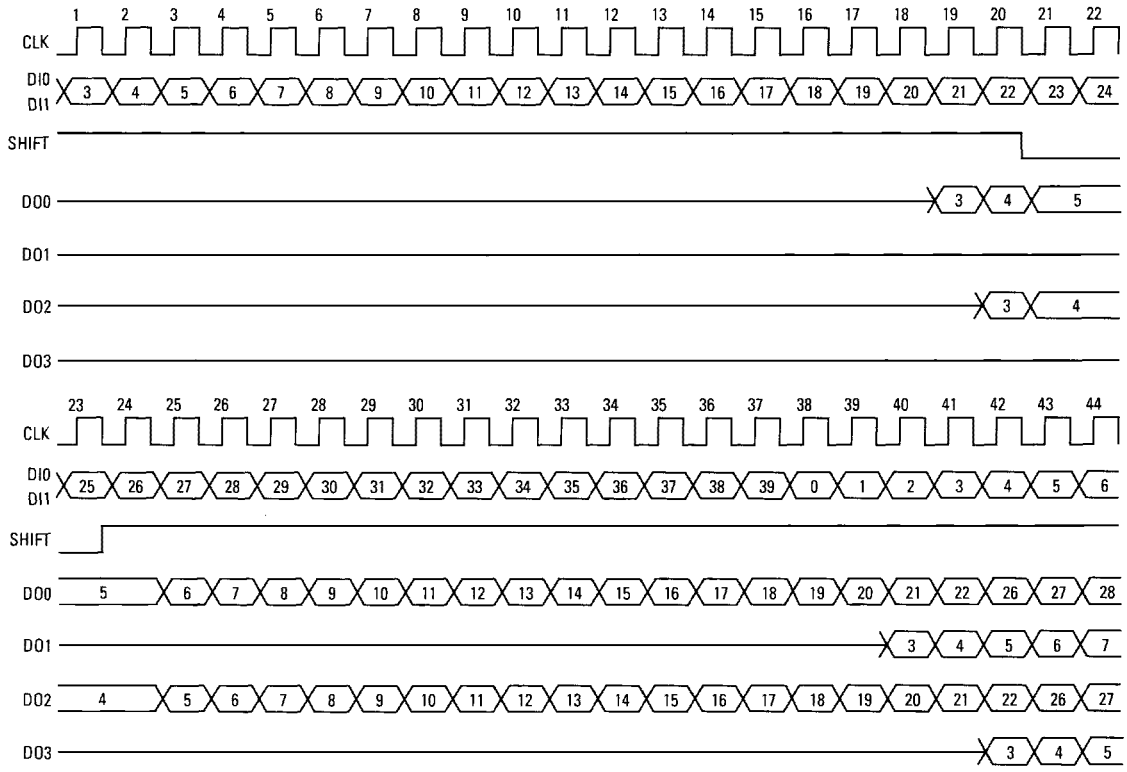
Note: Three bits are used to specify each K value. Ki = 2Ki + Ki.0 + Li.

Power Down Mode

This mode allows the device to be put into an inactive state with low IDD. In order to put the device in this power down mode, both REGADR pins should be held HIGH and the internal control word PDWN taken HIGH. In order to return the device to an active state PDWN should be taken LOW.

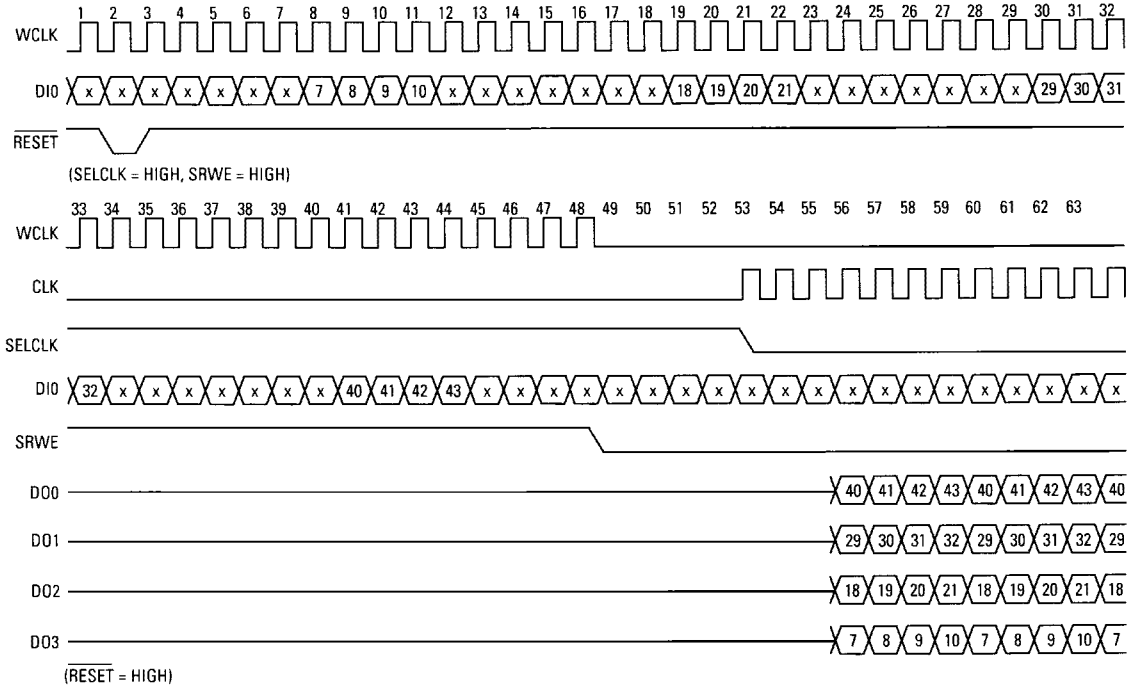
In power down mode the L64212 will retain the current data. To ensure the integrity of this data the device must be in an inactive state before, during and after it is put into power down mode. This can be achieved by taking SHIFT/HOLD LOW at least four complete cycles before taking PDWN HIGH, and continuing to hold it LOW for at least four complete cycles after taking PDWN LOW again.

Functional Waveforms **Shift Register Operation (SELCLK LOW, N = I, K1, K2 = 3, K3, K4 = 4, 2inp = HIGH)**



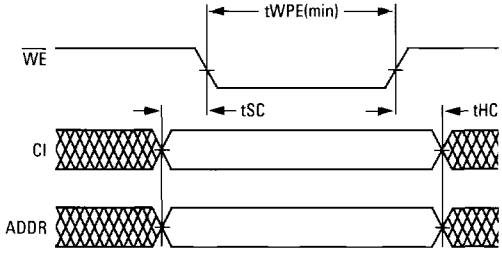
Functional Waveforms (Continued)

Circular Buffer Operation (N = 0, K1, K2, K3 K4 = 0, 2inp = LOW)

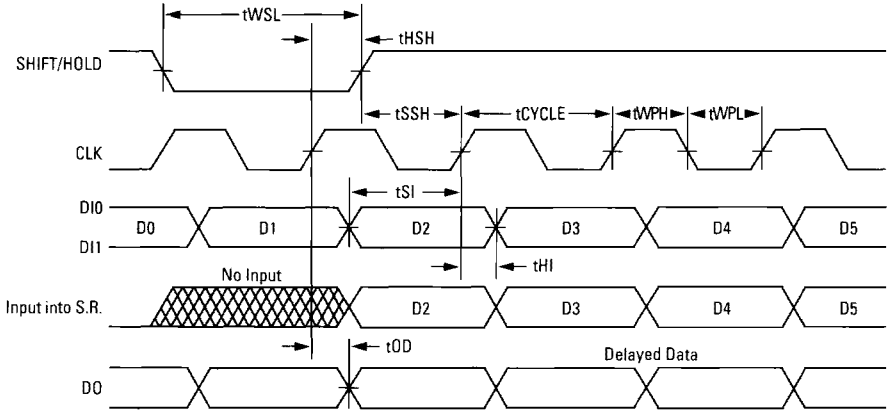


AC Timing Waveforms

Coefficient/Control Section



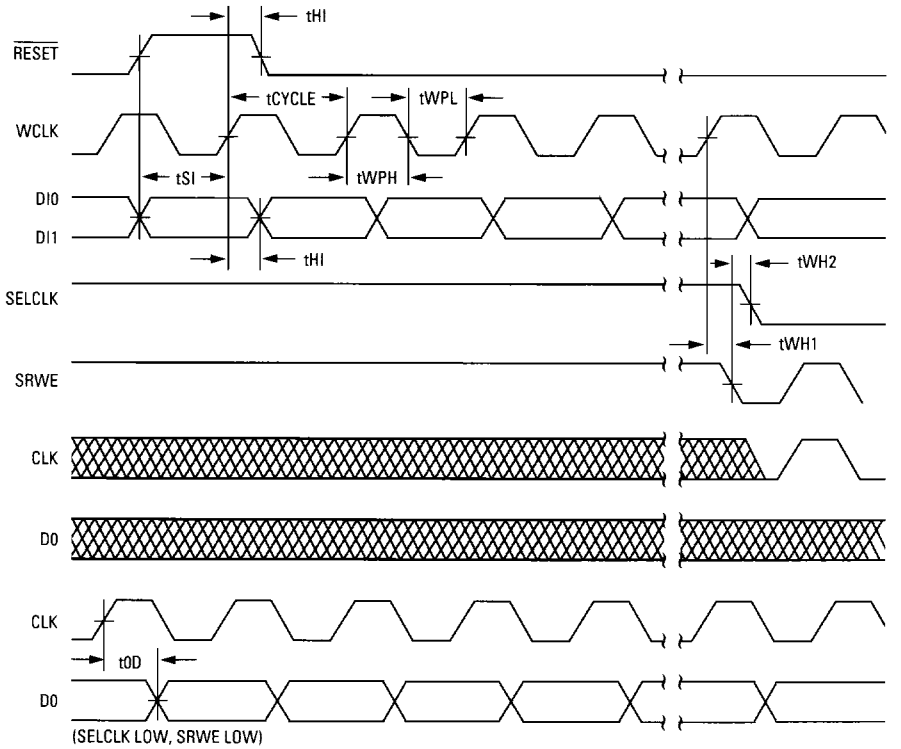
Shift Register Input/Output Timing (SRWE = HIGH, SELCLK = LOW)



(tWSL = 2 clock minimum)

AC Timing Waveforms
(Continued)

Circular Buffer Timing (Top-Loading, Bottom-Reading)



AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75V to 5.25V)
Military (TA = -55°C to 125°C, VDD = 4.5V to 5.5V)

Symbol	Parameter	L64212-40		L64212-30	
		Min (ns)	Max (ns)	Min (ns)	Max (ns)
tCYCLE	Clock cycle time	25		33	
tPWH(min)	Minimum clock pulse width, HIGH	10		14	
tPWL(min)	Minimum clock pulse width, LOW	10		14	
tSI	Input data setup time	5		7	
tHI	Input data hold time	5		7	
tWPE	WE pulse width	10		15	
tSC	CI input setup time	5		6	
tHC	CI input hold time	7		8	
tOD	Output delay time		18		20
tSSH	SHIFT/HOLD setup time	5		7	
tHSH	SHIFT/HOLD hold time	5		7	
tWH1	SRWE hold time	5		6	
tWH2	SELCLK hold time	10		13	

Note: All times are in ns.
tWSL = 2 rising edges of the clock.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition			Min	Typ	Max	Unit
VIL	Low level input voltage						0.8	V
VIH	High level input voltage Commercial temperature range Military temperature range				 2.0 2.25			 V V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	High level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current[2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = 0V			-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS					10	mA
IDD	Operating supply current[3]	tCYCLE = 25 ns				400		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 40 MHz device.

L64212 Package Pin Information (95-Pin PGA, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	VSS	B4	VSS	D2	SHIFT/HOLD	H2	DO0.2	M2	DO1.8	N14	VDD
A3	VDD	B5	DI0.5	D13	CI.1	H13	DO2.0	M13	DO2.8	P1	VDD
A4	DI0.4	B6	DI0.7	D14	CI.2	H14	VDD	M14	DO2.7	P2	VSS
A5	DI0.6	B7	DO3.0	E1	DO0.7	J1	DO0.1	N1	VSS	P3	DO1.5
A6	DI0.8	B8	DO3.3	E2	DO0.8	J2	DO0.0	N2	DO1.7	P4	VDD
A7	DO3.1	B9	DO3.5	E13	CI.3	J13	DO2.2	N3	DO1.6	P5	DO1.3
A8	DO3.2	B10	VDD	E14	CI.4	J14	DO2.1	N4	VSS	P6	DO1.1
A9	DO3.4	B11	DO3.7	F1	DO0.5	K1	NC	N5	DO1.4	P7	SRWE
A10	DO3.6	B12	WE	F2	DO0.6	K2	CLK	N6	DO1.2	P8	DI1.7
A11	VSS	B13	REGADR.0	F13	CI.5	K13	DO2.4	N7	DO1.0	P9	DI1.6
A12	DO3.8	B14	VSS	F14	CI.6	K14	DO2.3	N8	DI1.8	P10	DI1.4
A13	VSS	C1	DI0.0	G1	VSS	L1	WCLK	N9	DI1.5	P11	VSS
A14	VDD	C2	DI0.1	G2	DO0.4	L2	SELCLK	N10	VDD	P12	DI1.2
B1	VDD	C13	REGADR.1	G13	VSS	L13	DO2.6	N11	DI1.3	P13	VDD
B2	DI0.2	C14	CI.0	G14	CI.7	L14	DO2.5	N12	DI1.1	P14	VSS
B3	DI0.3	D1	RESET	H1	DO0.3	M1	OUTEN	N13	DI1.0		

L64212 Package Pin Information (95-Pin PGA, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
C14	CI.0	B6	DI0.7	F1	DO0.5	K14	DO2.3	B13	REGADR.0	P13	VDD
D13	CI.1	A6	DI0.8	F2	DO0.6	K13	DO2.4	C13	REGADR.1	A2	VSS
D14	CI.2	N13	DI1.0	E1	DO0.7	L14	DO2.5	D1	RESET	A11	VSS
E13	CI.3	N12	DI1.1	E2	DO0.8	L13	DO2.6	L2	SELCLK	A13	VSS
E14	CI.4	P12	DI1.2	N7	DO1.0	M14	DO2.7	D2	SHIFT/HOLD	B4	VSS
F13	CI.5	N11	DI1.3	P6	DO1.1	M13	DO2.8	P7	SRWE	B14	VSS
F14	CI.6	P10	DI1.4	N6	DO1.2	B7	DO3.0	K1	NC	G1	VSS
G14	CI.7	N9	DI1.5	P5	DO1.3	A7	DO3.1	A3	VDD	G13	VSS
K2	CLK	P9	DI1.6	N5	DO1.4	A8	DO3.2	A14	VDD	N1	VSS
C1	DI0.0	P8	DI1.7	P3	DO1.5	B8	DO3.3	B1	VDD	N4	VSS
C2	DI0.1	N8	DI1.8	N3	DO1.6	A9	DO3.4	B10	VDD	P2	VSS
B2	DI0.2	J2	DO0.0	N2	DO1.7	B9	DO3.5	H14	VDD	P11	VSS
B3	DI0.3	J1	DO0.1	M2	DO1.8	A10	DO3.6	N10	VDD	P14	VSS
A4	DI0.4	H2	DO0.2	H13	DO2.0	B11	DO3.7	N14	VDD	L1	WCLK
B5	DI0.5	H1	DO0.3	J14	DO2.1	A12	DO3.8	P1	VDD	B12	WE
A5	DI0.6	G2	DO0.4	J13	DO2.2	M1	OUTEN	P4	VDD		

Note: NC means do not connect.

Packaging **95-Pin Ceramic Pin Grid Array:** See FQ Package in Package Selector Guide

Ordering Information

L64212 G M -XX

- -XX — Speed in MHz
- M — Temperature Range/Flow Option
  - C = Commercial (0°C to 70°C)
  - M = Military (-55°C to +125°C), Processed to MIL-STD-883C Level B
- G — Package Code
  - G = 95-Pin Ceramic Pin Grid Array
- L64212 — Device Type
  - High Speed Video Shift Register