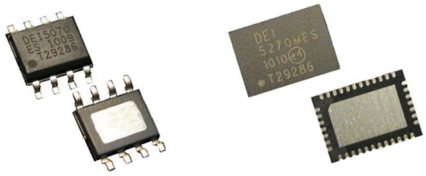
DEVICE ENGINEERING INCORPORATED

deiaz.com

DEI5070, 5071, 5072, 5270 ARINC 429 ±5 V LINE DRIVER FAMILY

FEATURES

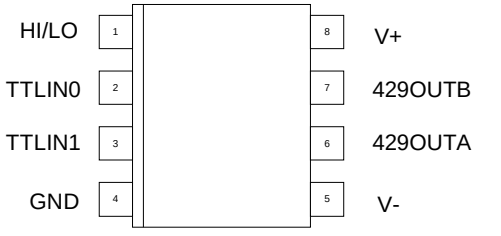
- TTL/CMOS TO ARINC 429 Line Driver.
- Rate control input set Hi (100 kbps) or Lo (12.5 kbps) speed slew rates.
- Operates from ±5V power supply.
- Drives full ARINC load.
- Output resistor options: 7.5, 27.5 or 37.5 Ω.
- Packages:
  - 8L SOIC Exposed Pad (single driver)
  - 38L MLPQ (QFN) (dual driver)



GENERAL DESCRIPTION

The DEI5x7x family of CMOS integrated circuits are line drivers designed to directly drive the ARINC 429 avionics serial digital data bus. The device converts TTL/CMOS serial input data to the tri-level RZ bipolar differential modulation format of the ARINC bus. A TTL/CMOS control input selects the output slew rate for HI (100 kbps) and LOW (12.5 kbps) speed operation. No external timing capacitors are required.

The DEI5070 has internal 37.5 Ω output resistors, the DEI5071 has 27.5 Ω resistors, the DEI5072 has 7.5 Ω resistors, and the DEI5270 has two drivers with all output resistor options. The 27.5 and 7.5 Ω options require external series resistors which are typically used to implement a transient voltage protection network.



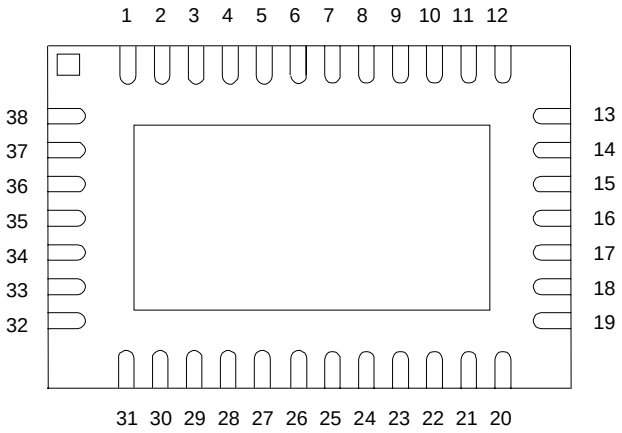
Note: Heatsink pad is electrically isolated

Table 1 5070/71/72 PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	HI/LO	LOGIC INPUT: Slew rate control.
2	TTLIN0	LOGIC INPUT: Serial digital data input 0
3	TTLIN1	LOGIC INPUT: Serial digital data input 1
4	GND	POWER INPUT: Ground
5	V-	POWER INPUT: -5 VDC
6	429OUTA	429 OUTPUT: ARINC 429 format serial digital data output A
7	429OUTB	429 OUTPUT: ARINC 429 format serial digital data output B
8	V+	POWER INPUT: +5 VDC

Notes:

1. Package: 38 Lead 5.0 x 7.0 mm MLP
2. Exposed Pad is electrically isolated

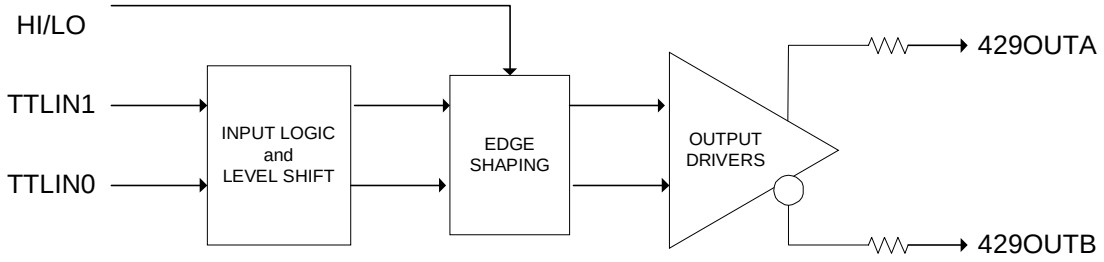


BOTTOM VIEW

Table 2 5270 PIN DESCRIPTION

SIGNAL NAME	Channel 1 Pin	Channel 2 Pin	DESCRIPTION
HI/LO_n	5	24	LOGIC INPUT: Slew rate control. 1 = Hi speed. 0 = Low speed.
TTLIN0_n	6	25	LOGIC INPUT: Serial digital data input 0.
TTLIN1_n	26	7	LOGIC INPUT: Serial digital data input 1.
429OUTA_7_n	34	15	429 OUTPUTS: ARINC 429 format serial digital data output A, 7.5 Ω
429OUTA_27_n	33	14	429 OUTPUTS: ARINC 429 format serial digital data output A, 27.5 Ω
429OUTA_37_n	32	13	429 OUTPUTS: ARINC 429 format serial digital data output A, 37.5 Ω
429OUTB_7_n	36	17	429 OUTPUTS: ARINC 429 format serial digital data output B, 7.5 Ω
429OUTB_27_n	37	18	429 OUTPUTS: ARINC 429 format serial digital data output B, 27.5 Ω
429OUTB_37_n	38	19	429 OUTPUTS: ARINC 429 format serial digital data output B, 37.5 Ω
V+	2	20	POWER INPUT: +5 VDC
GND	28	9	POWER INPUT: Ground
V-	30	12	POWER INPUT: -5 VDC
NC	1, 3, 4, 8, 10, 11, 16, 21, 22, 23, 27, 29, 31, 35		No Internal Connect

FUNCTIONAL DESCRIPTION



Block Diagram (single channel shown)

Table 3 Speed Control Function Table

HI/LO	OUTPUT TRANSITION TIME
0	10 us (12.5 kbps data)
1	1.5 us (100 kbps data)

Table 4 Transmit Data Function Table

TTLIN1	TTLIN0	429OUTA (V)	429OUTB (V)	NOTES
0	0	0	0	Null output
0	1	-5	5	Zero output
1	0	5	-5	One output
1	1	0	0	Null output

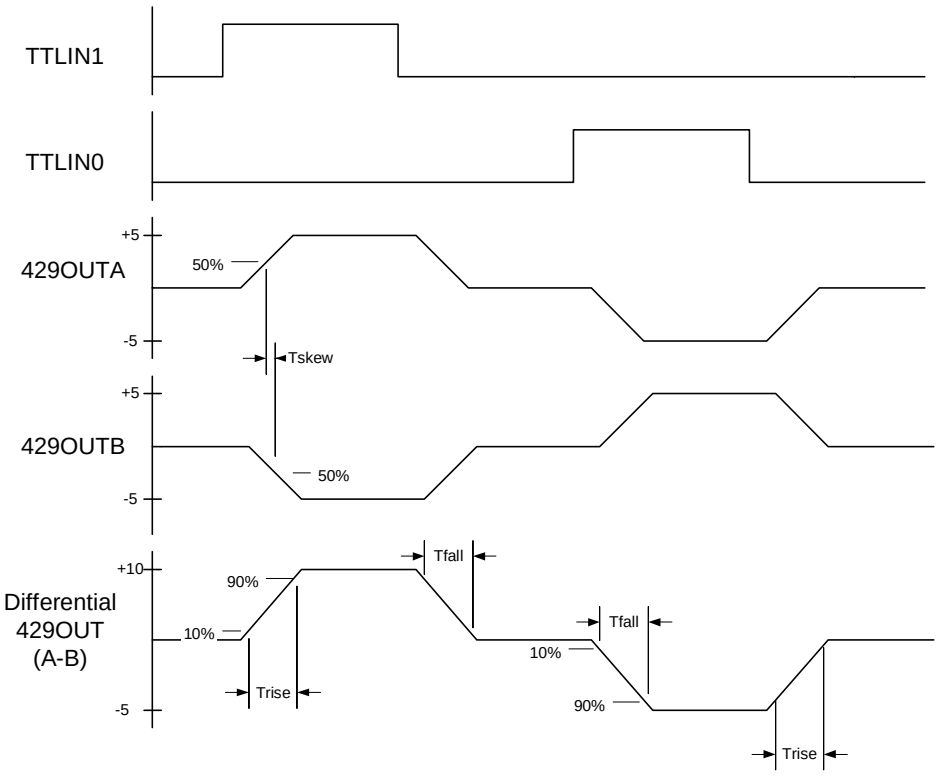


Figure 1 Timing Waveforms

ELECTRICAL DESCRIPTION

Table 5 Absolute Maximum Ratings

PARAMETER Voltages referenced to Ground	MIN	MAX	UNIT
V+ Supply Voltage	-0.3	+7	V
V- Supply Voltage	0.3	-7	V
Storage Temperature	-65	+150	°C
Input Voltage TTLIN and HI/LO Inputs 429OUT Outputs	 Gnd – 0.3 V- – 0.3	 V+ + 0.3 V+ + 0.3	 V V
Power Dissipation @ 85 °C: (> 10 Sec), Thermal pad soldered to heat spreader -Sxx package, derate 20mW/C above 85°C -Mxx package, derate 28.3mW/C above 85°C		 1.2 1.7	W
Junction Temperature: Tjmax, Plastic Packages (Limited by molding compound Tg)		 145	°C
ESD per JEDEC A114-A Human Body Model		2000	V
Peak Body Temperature (Pb Free solder profile)		260	°C
Notes: 1. Stresses above absolute maximum ratings may cause permanent damage to the device. 2. The device is tolerant of one or both outputs shorted to Ground and of both outputs shorted together.			

Table 6 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	V+ V-	4.8 to 5.3 V -4.8 to -5.3 V
Operating Temperature -xEx variants -xMx variants	T_{OP}	 -55 to +85 °C -55 to +125 °C

Table 7 Electrical Characteristics

Conditions (Unless otherwise noted):
Temperature: -55 to +85 °C (-xEx) or -55 to +125 °C (-xMx)
V+ = +4.8 to +5.3 V and V- = -4.8 to -5.3 V

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
LOGIC INPUTS						
Input Voltage, Logic 1		V_{IH}	2.0		V+	V
Input Voltage, Logic 0		V_{IL}	-0.3		0.8	V
Input Current	VIN = 0 to 5V	I_{IH}	-10		10	µA
ARINC OUTPUTS						
ARINC Output Voltage (Differential) One Null Zero	Differential Output Voltage = 429OUTA – 429OUTB. No Load.	 V_{DIF1} $V_{DIFnull}$ V_{DIF0}	 9.0 -0.5 -11.0	 10.0 0 -10.0	 11.0 +0.5 -9.0	 V V V
ARINC Output Voltage (Single Ended) Hi Null Lo	Referenced to Ground No Load.	 Vo_{HI} $Vo_{null,}$ Vo_{LO}	 4.5 -0.25 -5.5	 5.0 0 -5.0	 5.5 +0.25 -4.5	 V V V
ARINC Output Short Circuit Current	Outputs shorted to Ground with Rout = 37 Ω	 Isc_{LO} Isc_{HI}		 133 -133		 mA mA
Output Resistance: DEI5070 DEI5071 DEI5072	Room Temperature	Rout		 37.5 27.5 7.5		Ω
Output Slew Rate Hi Speed	HI/LO = 1 No Load 10% to 90% voltage amplitude of differential output.	T_{rise} T_{fall}	1.0	1.5	2.0	µs
Output Slew Rate Lo Speed	HI/LO = 0 No Load 10% to 90% voltage amplitude of differential output.	T_{rise} T_{fall}	5.0	10	15	µs
Output skew time between A and B outputs.	HI/LO = 1 Measured at 50% voltage amplitude of both outputs.	Tskew			200	ns
SUPPLY CURRENT						
Quiescent Operating Supply Current: IV+ IV-	V+ =5V, V- = -5V HI/LO = 0 or 1 TTLIN0=TTLIN1= 0V No Load	 I_{V+} I_{V-}	 - -10	 6 -6	 10 -	 mA mA

DESIGN CONSIDERATIONS

Power Supplies and Bypass Capacitors

The DEI507X Line Driver operates from ±5 V dual supplies. Proper bypassing capacitor ensures stability while driving large capacitive loads. The Line Driver requires a minimum of a 0.1uF bypass capacitor placed as close as possible to the V+ and V- pins.

Transient Voltage Protection

The DEI507X Line Driver requires external components to achieve immunity from surges such as those defined by DO160D Section 22, "Lightning Induced Transient Susceptibility". Typical surge protection includes silicon Transient Voltage Suppressor (TVS) devices and may include part of the 37.5 Ω output resistance as external resistors to limit the surge current.

The 507X has a robust output stage which includes large driver devices and clamp diodes to the V+ and V- power rails as shown in Figure 2. It withstands surge currents of ±0.5 A for 175 us without damage when powered with ±5V supplies. At that surge current, the diodes clamp at ~1V above (below) the V+ (V-) supply rail. ~350 mA flows to the V- (V+) supply through the output amplifier, and ~150 mA flows to the V+ (V-) supply through the clamp diode. The outputs may be damaged by surges greater than 1 A / 175 us. At that current, the diodes clamp at ~1.8 V above (below) the supply.

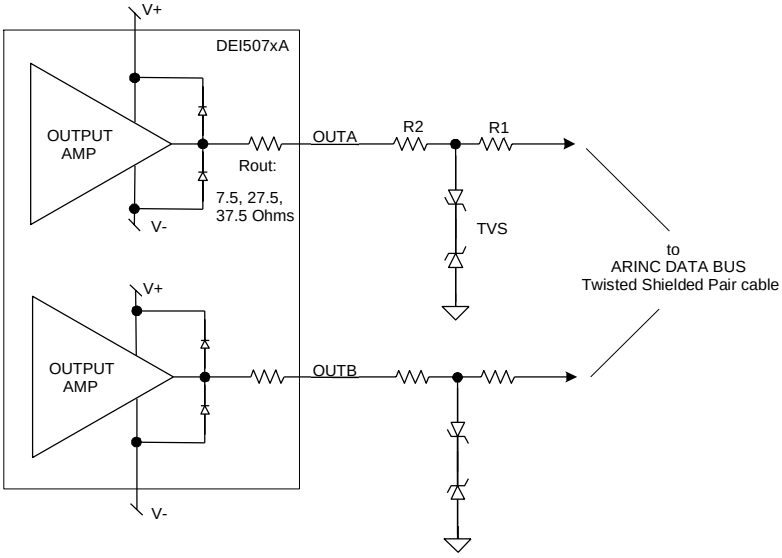


Figure 2 Surge Protection Network

The external lightning protection network should be designed to meet the specific requirements and constraints of the application equipment. The protection network should limit the OUTA/B pin surge current to the 0.5 A / 175 us maximum. The generalized circuit of Figure 2 represents several TVS protection network options:

- The on-chip Rout value is 7.5, 27.5, or 37.5 Ω depending on the 5070 – 5072 part number
- Select the total output resistance, Rout + R1 + R2, = 37.5 Ω to meet ARINC bus requirements
  - Select R1 = 20 Ω, R2 = 10 Ω, Rout = 7.5 Ω to use low TVS surge current rating (small TVS devices)
  - Select R1 = 0 Ω, Rout + R2 = 37.5 Ω to use high TVS clamp voltage (20 V + V+/-)
  - If the V+/V- supplies are un-powered or below operating voltage during the surge event, large currents may flow through the internal clamp diodes and damage the driver. If the application requires lightning immunity while un-powered, Select R1 = 0 Ω, Rout + R2 = 37.5 Ω, and select the TVS clamp voltage for <20 V.
- Select TVS devices for the following
  - TVS Surge power/current rating must withstand the application requirements for Lightning Induced Transient Levels and Waveforms. Microsemi Corporation publishes an application note specific to the DO160 lightning requirements, available at: http://www.microsemi.com/micnotes/126.pdf
  - Select low capacitance TVS devices to minimize the load on the line driver. (Examples: Microsemi LC and HSMBJSA series TVS) This is a priority for Hi Speed ARINC applications where the low capacitance is important for optimum signal integrity and power consumption. Note that the maximum total capacitance on the ARINC bus is 30 nF line to line.
  - Select the TVS clamp voltage at the lightning surge conditions such that the voltage/current into the 507X OUT pin is within the safe region.
- If R1 is used to limit the TVS surge current, the resistor must withstand the surge current and voltage.

Alternate protection methods may be appropriate in some applications.

- External clamp diodes to the supply rails may be used to shunt surge current to the supply rails rather than to Ground.
- PTC "resetable fuses" may be used for R1 to protect the driver and TVS from shorts to 28 V aircraft power.

Some general considerations related to Lightning Immunity:

- Analyze the TVS high current signal and ground return path to insure adequate surge current capability. The IR voltage and L*di/dt voltage in the ground return will add additional stress beyond the TVS clamp voltage.
- Observe suitable PCB design rules for traces subject to high voltage and high current surges.
- When possible, locate TVS devices close to the equipment connector to minimize the length of the surge voltage/current traces within the equipment.
- The shields of ARINC 429 data bus cables should be terminated to aircraft ground at all ends and at all bulkhead disconnects.

Thermal Management

Good thermal management is fundamental to Line Driver device reliability. It is particularly important in designs operating at the HI speed data rate (100 kbps) with high capacitive loads as this produces maximum power dissipation. While the 507X device will function at a junction temperature (Tj) above 190 °C, it is inappropriate to continuously operate the plastic package above 150 °C. Like all microcircuits, long term reliability is improved with lower operating temperatures.

The Line Driver's operating Tj is determined by internal power dissipation, package thermal resistance, and ambient temperature. The internal power dissipation (Pd) varies greatly with several variables:

- Data Rate – The Hi Speed (100 kbps) rate produces maximum power dissipation
- Load – The maximum ARINC 429 load is 30 nF||400 Ω line-to-line. Many applications only drive a fraction of the full load.
- Data Duty Cycle – ARINC bus activity, averaged over 10 seconds = Bits transmitted / total possible bits. Many applications are active <70%.
- Supply Voltage +V / -V supplies are ±5 V
- Rout configuration – The power dissipated in the two 37.5 Ω output resistors is internal to the IC for the 5070 and external for the 5072.

The internal power dissipation for 100 kbps applications can be estimated from Figures 4-7. Power dissipation for low speed operation (12.5 kbps) is normally not an issue, so is not considered here. he curves in indicate power dissipation for various loads, supply voltage, and Rout configuration. It represents Pd for 100% Data Duty Cycle (DDC) at 100 kbps with no word gap null times. Thus, the indicated Pd values are considered maximum values and should be reduced to account for the Data Duty Cycle as follows:

- Estimate DDC = total bits transmitted in 10 sec period / 1,000,000
  = 32 x total ARINC words transmitted in 10 sec period / 1,000,000
- Select an indicated Pd for the application supply voltage and load. This may involve estimating the Line Driver's load and interpolating between the curves.
- Calculate adjusted Pd = DDC * (Pd - 0.1) + 0.1 (W)

The operating junction temperature is calculated as follows:

$Tj = Ta + Pd*\Theta ja$

where

Tj = junction temperature (°C)

Ta = Ambient temperature (°C)

Pd = Internal power dissipation (W)

Θja = IC package thermal resistance from junction to ambient (°C/W). Refer to package details.

The ARINC 429 Line Driver outputs may be subject to short circuit conditions due to cable wiring errors or faults which typically occur during equipment test and aircraft installation environments. The common cases are one or both outputs shorted to Ground, or both outputs shorted together. These conditions may cause considerable internal power dissipation depending on the following:

- Data Duty Cycle – The line-to-line and line-to-Ground shorts cause little or no power dissipation when the outputs are in the Null state. However when the output is driving a HI/LO state, the short circuit current is limited by the 37.5 Ω Rout at about ~133 mA. This is modulated by the ARINC waveform, producing an effective current of ~88 mA* DDC. This current causes heating in the output amplifier and Rout resistor.

- Supply Voltage – A lower supply voltage results in lower Pd during short circuit conditions. The internal Pd for both outputs shorted while operating at 100% DDC is ~750 mW with ±5 V supplies but is reduced to ~650 mW with ±4.8 V supplies. This is for 37.5 Ω Rout configurations.

- Rout configuration – Each of the two 37.5 Ω Rout resistors dissipates ~0.7 W when shorted at 100% DDC. This power is dissipated in the external resistors for the 5072 parts, and internal to the IC for the 5070 parts. Thus the 5072 have a lower Tj and are more tolerant to short circuit conditions.

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the Line Driver IC package. Use maximum trace width on all power and signal connections at the IC. These traces serve as heat spreaders which improve heat flow from the IC leads. The exposed heat sink pad of the SOIC package should be soldered to a heat-spreader land pattern on the PCB. The IC exposed pad is electrically isolated, so the PCB land may be at any potential; typically Ground for the best heat sink. Maximize the PCB land size by extending it beyond the IC outline if possible. A grid of thermal VIAs, which drop down and connect to the buried copper plane(s), should be placed under the heat-spreader land. A typical VIA grid is 12mil holes on a 50 mil pitch. The barrel is plated to about 1.0 oz copper. Use as many VIAs as space allows. VIAs should be plugged to prevent voids being formed between the exposed pad and PCB heat-spreader land due to solder escaping by the capillary effect. This can be avoided by tenting the VIAs with solder mask.

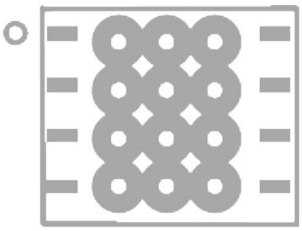


Figure 3 Example of a Thermal VIA Land Pattern

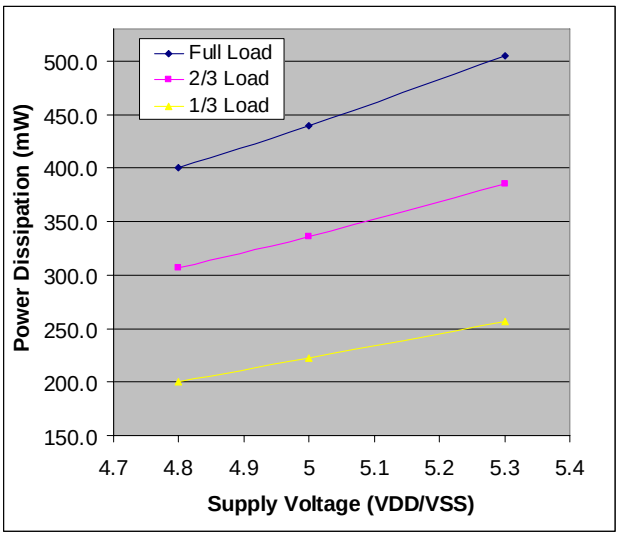


Figure 4 5070 Power Dissipation Comparison

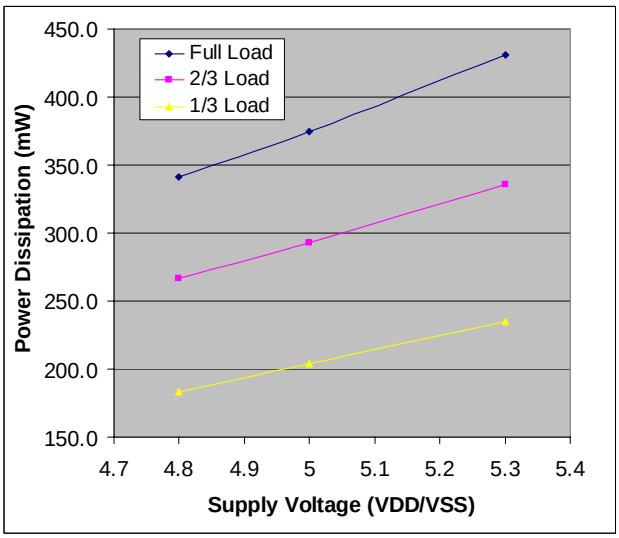


Figure 5 5071 Power Dissipation Comparison

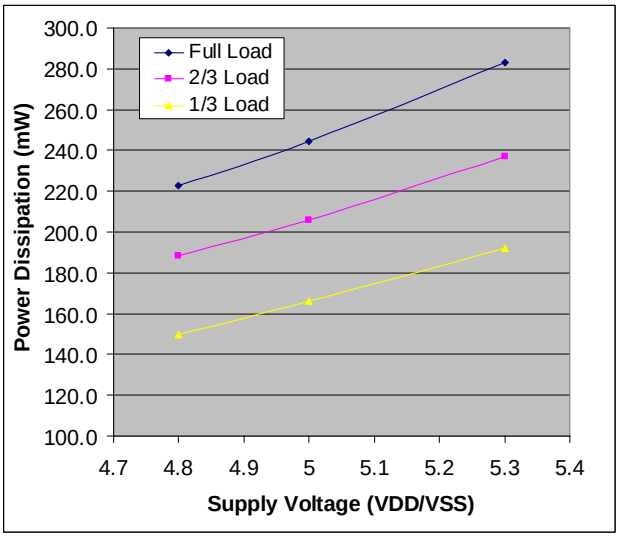


Figure 6 5072 Power Dissipation Comparison

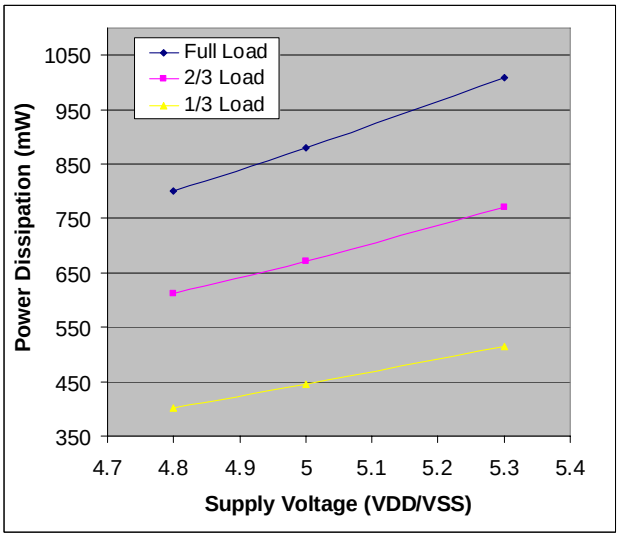


Figure 7 5270 Power Dissipation Comparison (2 chan, OUT_27)

Note:

1. 100% Data Duty Cycle.
2. Full Load: 400 Ω//30 nF, Mid Load: 600 Ω //20 nF, Light Load: 1200 Ω//10 nF

PACKAGE DESCRIPTIONS

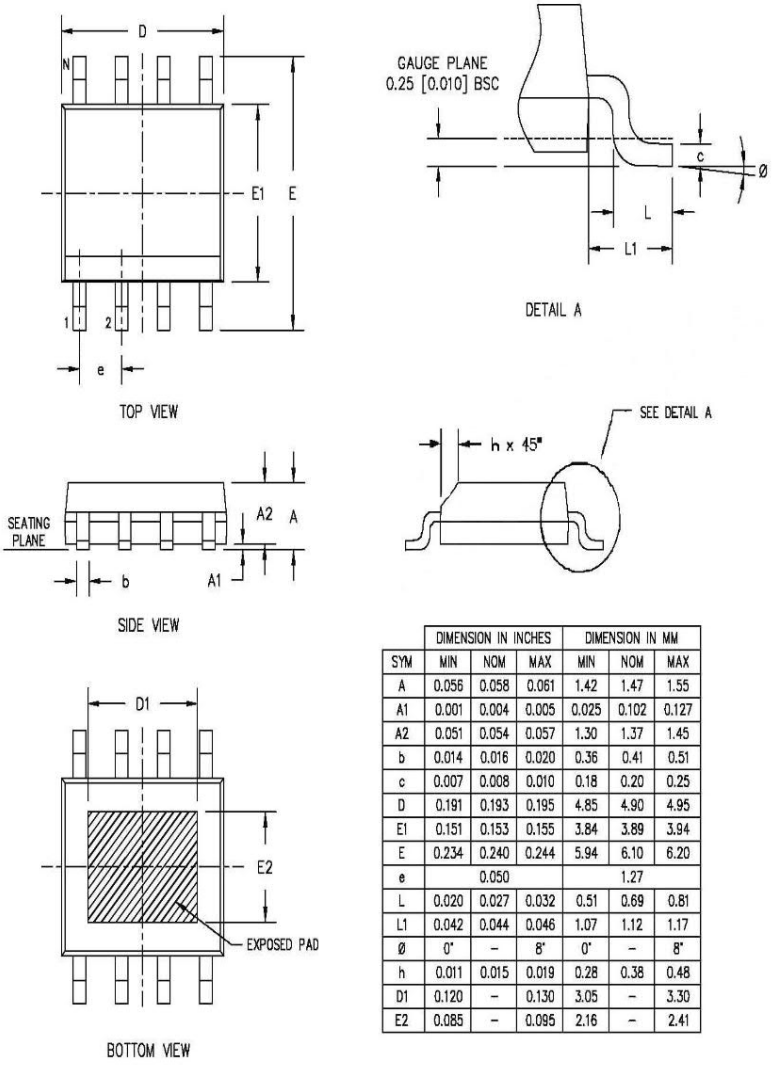
Table 8 Package Characteristics

PACKAGE TYPE	PACKAGE REF	THERMAL RESIST. θJC / θJA (°C/W)	JEDEC MOISTURE SENSITIVITY LEVEL & PEAK BODY TEMP	LEAD FINISH MATERIAL / JEDEC Pb-Free CODE	Pb Free DESIGNATION
8L EP SOIC	8 EP SOIC G	10 / 49 (1)	MSL 1 / 260 °C	NiPdAu / e4	RoHS Compliant
38L 5X7 MLPQ	38 5X7 I MLPQ G	8 / 34 (1)	MSL 3 / 260 °C	NiPdAu / e4	RoHS Compliant

Notes:

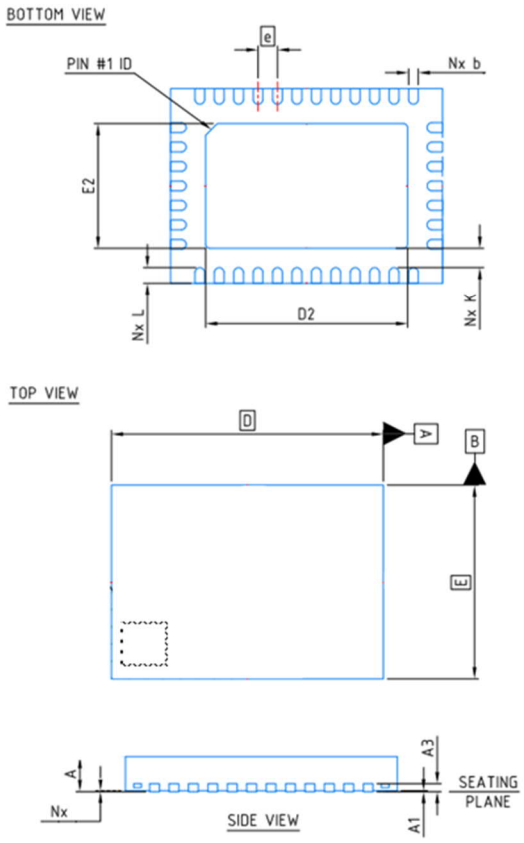
1. θJA with the exposed pad soldered to a PCB land with thermal vias connected to an internal ground plane which is one of the 2 center layers on a 4 layer board .

8 Lead EP SOIC



	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.056	0.058	0.061	1.42	1.47	1.55
A1	0.001	0.004	0.005	0.025	0.102	0.127
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.234	0.240	0.244	5.94	6.10	6.20
e		0.050			1.27	
L	0.020	0.027	0.032	0.51	0.69	0.81
L1	0.042	0.044	0.046	1.07	1.12	1.17
Ø	0°	–	8°	0°	–	8°
h	0.011	0.015	0.019	0.28	0.38	0.48
D1	0.120	–	0.130	3.05	–	3.30
E2	0.085	–	0.095	2.16	–	2.41

38 Lead MLPQ 5.0 x 7.0



Dimension Table				
Variation / Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref.	---	
b	0.18	0.25	0.30	6
D		7.00 BSC		
E		5.00 BSC		
e		0.50 BSC		
D2	5.10	5.20	5.30	
E2	3.10	3.20	3.30	
K	0.20	---	---	
L	0.30	0.40	0.50	
aaa		0.05		
bbb		0.07		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		38		3
ND		12		5
NE		7		5
NOTES		1, 2		
LF PART NO.		445707		
LF DWG. NO.		038L152650DCEr0		

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND refers to the number of terminals on D side.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

ORDERING INFORMATION

PART NUMBER	MARKING	PACKAGE	OUTPUT RESISTOR (Ω)	TEMPERATURE (ºC)
DEI5070-SES-G	DEI5070 / ES	8 EP SOIC G	37.5	-55 / +85
DEI5071-SES-G	DEI5071 / ES	8 EP SOIC G	27.5	-55 / +85
DEI5072-SES-G	DEI5072 / ES	8 EP SOIC G	7.5	-55 / +85
DEI5270-MES-G	DEI5270 MES	38 5x7 I MLPQ G	7.5/27.5/37.5	-55 / +85
DEI5070-SMS-G	DEI5070 / MS	8 EP SOIC G	37.5	-55 / +125
DEI5071-SMS-G	DEI5071 / MS	8 EP SOIC G	27.5	-55 / +125
DEI5072-SMS-G	DEI5072 / MS	8 EP SOIC G	7.5	-55 / +125
DEI5270-MMS-G	DEI5270 MMS	38 5x7 I MLPQ G	7.5/27.5/37.5	-55 / +125