Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) CACHE-TAG RAM

IDT 7174S

4

FEATURES:

- High-speed address to MATCH comparison time
  - Military: 25/35/45/55ns (max.)
  - Commercial: 20/25/35/45ns (max.)
- High-speed address access time
  - Military: 25/35/45/55ns (max.)
  - Commercial: 20/25/35/45ns (max.)
- High-speed chip select access time
  - Military: 15/20/25/30ns (max.)
  - Commercial: 10/15/20/25ns (max.)
- Low-power operation
  - IDT7174S
    Active: 300mW (typ.)
- High-speed asynchronous RAM Clear on Pin 1 (Reset Cycle Time = 2 x t_{AA})
- MATCH Output on Pin 26
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Standard 28-pin DIP (600 mil and 300 mil), 28-pin SOIC (gull-wing or J-bend), 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7174 is a high-speed cache address comparator subsystem consisting of a 65,536-bit static RAM organized as 8K x 8 and an 8-bit comparator. A single IDT7174 can map 8K cache words into a 1 megabyte address space by comparing 20 bits of address organized as 13 word cache address bits and 7 upper address bits. Two IDT7174s can be combined to provide 28 bits of address comparison, etc. The IDT7174 also provides a single RAM clear control, which clears all words in the internal RAM to zero when activated. This allows the tag bits for all locations to be cleared at power-on or system-reset, a requirement for cache comparator systems. The IDT7174 can also be used as an 8K x 8 high-speed static RAM.

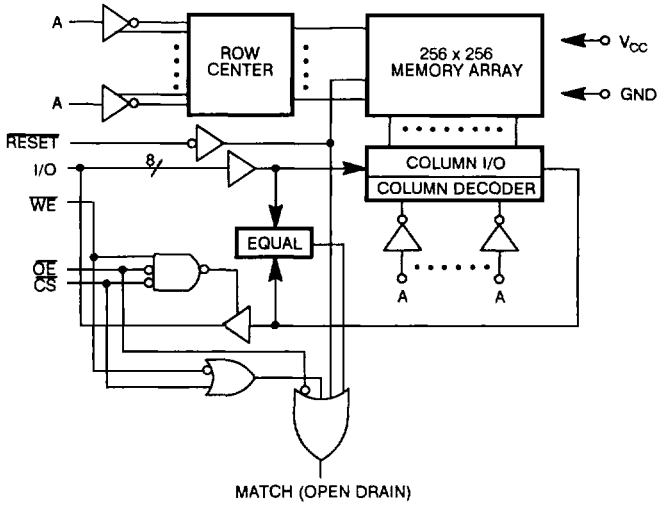
The IDT7174 is fabricated using IDT's high-performance, high-reliability technology – CEMOS. Address access times as fast as 20ns, chip select times of 10ns and address-to-comparison times of 20ns are available with maximum power consumption of 825mW.

All inputs and outputs of the IDT7174 are TTL-compatible and the device operates from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7174 is packaged in a 28-pin DIP (600 mil and 300 mil), a 28-pin SOIC (gull-wing or J-bend) and 32-pin LCC and PLCC, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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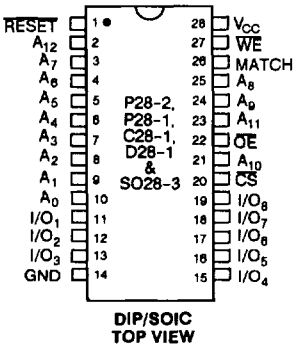
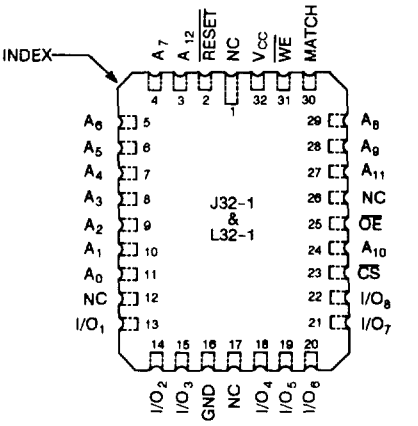
PIN CONFIGURATIONS

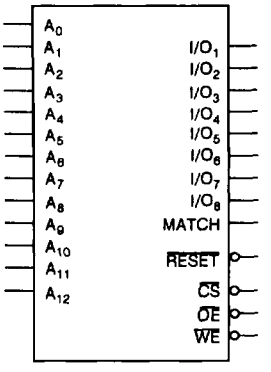


DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_{0-12}	Address	$\overline{WE}$	Write Enable
I/O_{1-8}	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
$\overline{RESET}$	Memory Reset	V_{CC}	Power
MATCH	Data/Memory Match (Open Drain)		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage (1)	2.2	–	6.0	V
V_{IHR}	$\overline{RESET}$ Input High Voltage	2.5 (2)	–	6.0	V
V_{IL}	Input Low Voltage	-0.5 (3)	–	0.8	V

NOTES:

1. All inputs except $\overline{RESET}$.
2. When using bipolar devices to drive the $\overline{RESET}$ input, a pullup resistor of 1kΩ-10kΩ is usually required to assure this voltage.
3. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7174S MIN.	IDT7174S TYP.(1)	IDT7174S MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	µA
			COM'L.	–	–	5	
$\|I_{LO}\|$	Output Leakage Current(2)	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	µA
			COM'L.	–	–	5	
V_{OL}	Output Low Voltage	I_{OL} = 18mA MATCH	MIL.	–	–	0.5	V
		I_{OL} = 22mA MATCH	COM'L.	–	–	0.5	V
		I_{OL} = 10mA, V_{CC} = Min. (All outputs except MATCH)		–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min. (All outputs except MATCH)		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA, V_{CC} = Min. (Except MATCH)		2.4	–	–	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. Data and MATCH

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	IDT7174S20 COM'L.	IDT7174S20 MIL.	IDT7174S25(2) COM'L.	IDT7174S25(2) MIL.	IDT7174S35 COM'L.	IDT7174S35 MIL.	IDT7174S45 COM'L.	IDT7174S45 MIL.	IDT7174S55 COM'L.	IDT7174S55 MIL.	UNIT
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0	110	–	110	125	110	125	110	125	–	125	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	190	–	170	190	150	170	140	150	–	145	mA

NOTES:
1. All values are maximum guaranteed values.
2. Military values are preliminary only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

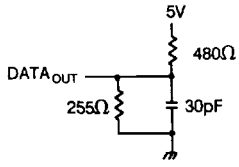


Figure 1. Output Load

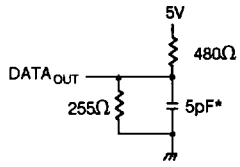


Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

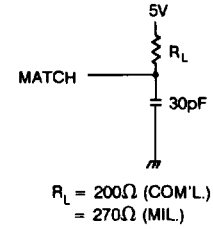


Figure 3. Output Load for MATCH

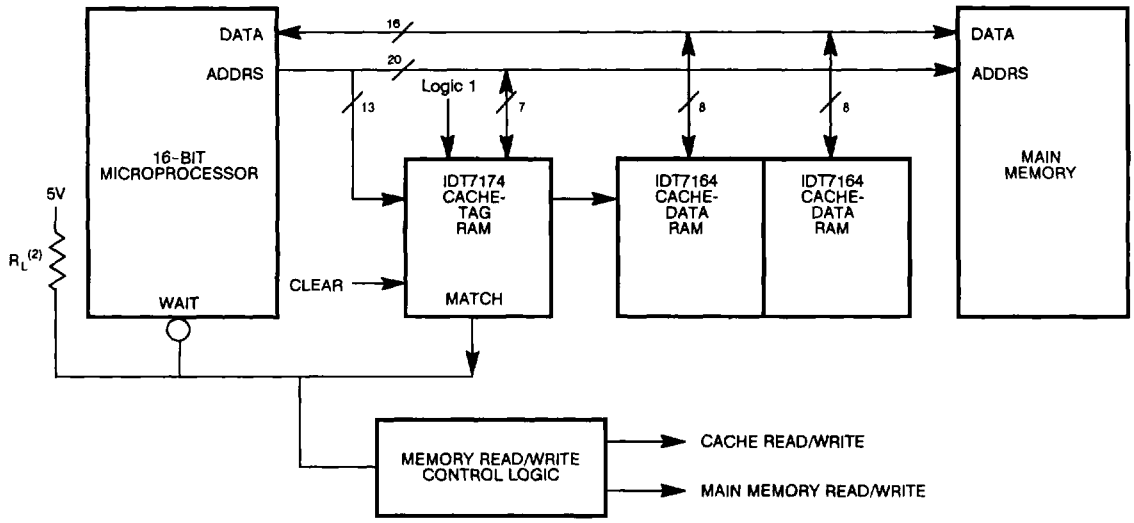


Figure 4. Example of Cache Memory System Block Diagram

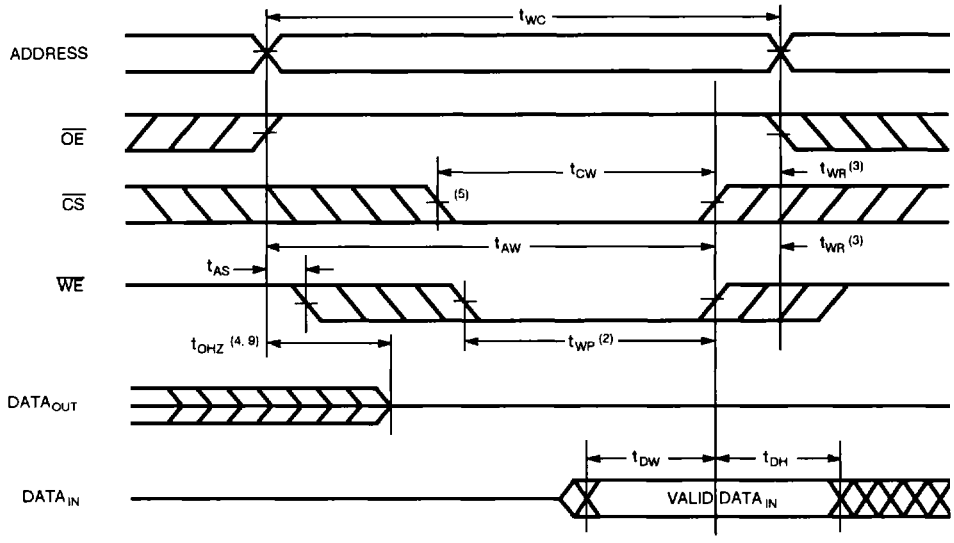
NOTES:
1. For more information, see application note AN-07 "Cache-Tag RAM Chips Simplify Cache Memory Design".
2. R_L = 200Ω (commercial) or 270Ω (military)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

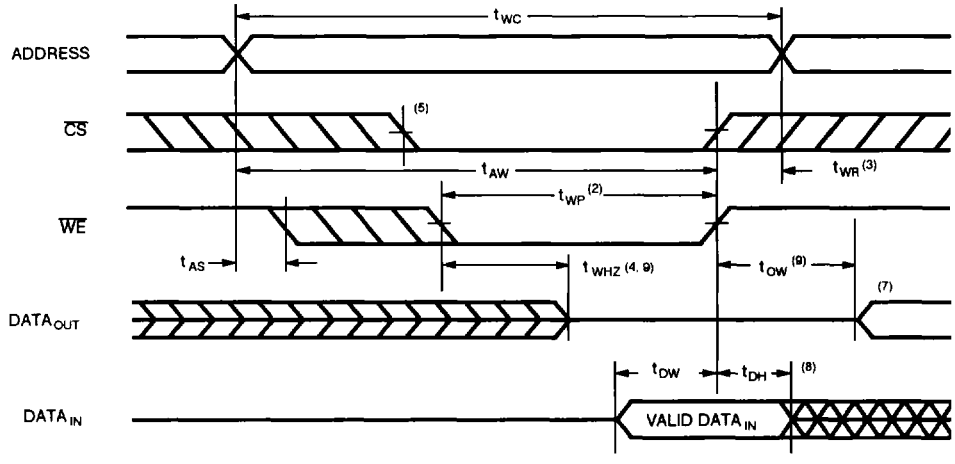
SYMBOL	PARAMETER	IDT7174S20(1)		IDT7174S25		IDT7174S35(1)		IDT7174S45		IDT7174S55(2)		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
WRITE CYCLE												
t_{WC}	Write Cycle Time	20	–	25	–	35	–	45	–	55	–	ns
t_{CW}	Chip Select to End of Write	12	–	15	–	20	–	25	–	30	–	ns
t_{AW}	Address Valid to End of Write	15	–	20	–	30	–	40	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	21	–	30	–	40	–	50	–	ns
t_{WR}	Write Recovery Time (CS, WE)	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write Enable to Output in High Z(3)	–	8	–	10	–	15	–	20	–	25	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	15	–	20	–	25	–	ns
t_{DH}	Data Hold From Write Time	2	–	2	–	2	–	2	–	2	–	ns
t_{OW}	Output Active from End of Write(3)	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary data for -55°C to +125°C temperature range only.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 [1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 [1, 6]



NOTES:

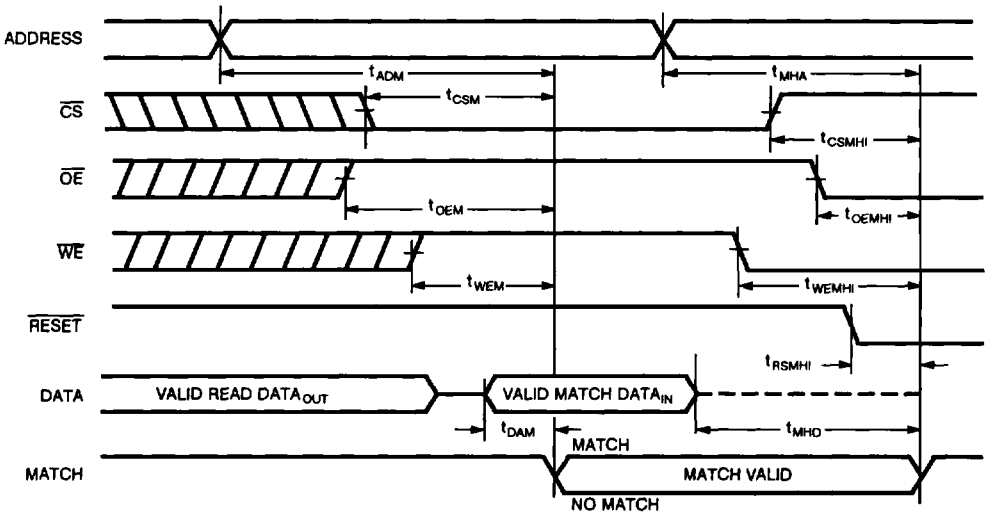
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{WE}$ and a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S20[1] MIN.	IDT7174S20[1] MAX.	IDT7174S25 MIN.	IDT7174S25 MAX.	IDT7174S35[3] MIN.	IDT7174S35[3] MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55[2] MIN.	IDT7174S55[2] MAX.	UNIT
MATCH												
t_{ADM}	Address to MATCH Valid	–	20	–	25	–	35	–	45	–	55	ns
t_{CSM}	Chip Select to MATCH Valid	–	10	–	15	–	20	–	25	–	30	ns
t_{CSMHI}	Chip Deselect to MATCH High	–	10	–	15	–	20	–	25	–	30	ns
t_{DAM}	Data Input to MATCH Valid	–	15	–	20	–	25	–	35	–	45	ns
t_{OEMHI}	$\overline{OE}$ Low to MATCH High	–	15	–	20	–	25	–	35	–	45	ns
t_{OEM}	$\overline{OE}$ High to MATCH Valid	–	15	–	20	–	25	–	35	–	45	ns
t_{WEMHI}	$\overline{WE}$ Low to MATCH High	–	15	–	20	–	25	–	35	–	45	ns
t_{WEM}	$\overline{WE}$ High to MATCH Valid	–	15	–	20	–	25	–	35	–	45	ns
t_{RSMHI}	$\overline{RESET}$ Low to MATCH High	–	15	–	20	–	25	–	35	–	45	ns
t_{MHA}	MATCH Valid Hold From Address	5	–	5	–	5	–	5	–	5	–	ns
t_{MHD}	MATCH Valid Hold From Data	5	–	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Preliminary data for -55°C to +125°C temperature range only.

MATCH TIMING



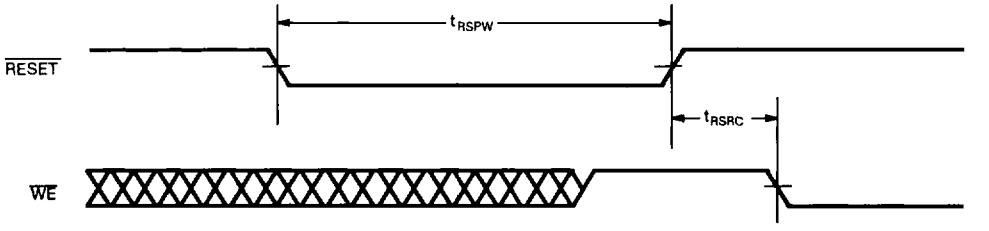
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S20[1] MIN.	IDT7174S20[1] MAX.	IDT7174S25 MIN.	IDT7174S25 MAX.	IDT7174S35[4] MIN.	IDT7174S35[4] MAX.	IDT7174S45 MIN.	IDT7174S45 MAX.	IDT7174S55[2] MIN.	IDT7174S55[2] MAX.	UNIT
RESET												
t_{RSPW}	$\overline{RESET}$ Pulse Width[3]	45	–	55	–	65	–	80	–	100	–	ns
t_{RSRC}	$\overline{RESET}$ High to $\overline{WE}$ Low	5	–	5	–	5	–	10	–	10	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. Recommended duty cycle 10% maximum.
4. Preliminary Information for -55°C to +125°C temperature range only.

4

RESET TIMING



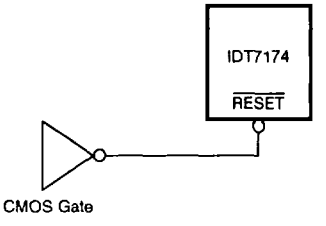
CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

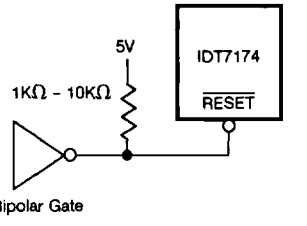
NOTE:
1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	$\overline{RESET}$	MATCH	I/O	FUNCTION
X	X	X	L	H	–	Reset all bits to low
X	H	X	H	H	High Z	Deselect chip
H	L	H	H	L	D_{IN}	No MATCH
H	L	H	H	H	D_{IN}	MATCH
H	L	L	H	H	D_{OUT}	Read
L	L	X	H	H	D_{IN}	Write



Driving the $\overline{RESET}$ pin with CMOS logic.



Driving the $\overline{RESET}$ pin with bipolar logic.

Figure 4.

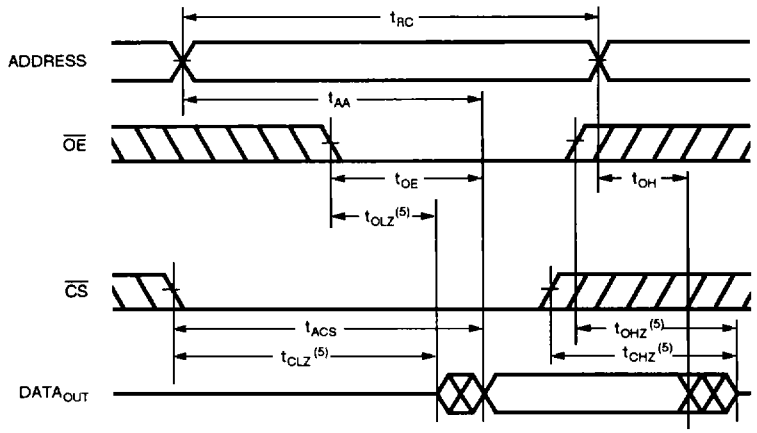
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT7174S20[1]		IDT7174S25		IDT7174S35[4]		IDT7174S45		IDT7174S55[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE												
t_{RC}	Read Cycle Time	20	–	25	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	10	–	12	–	20	–	25	–	30	ns
t_{CLZ}	Chip Select to Output in Low Z	0	–	0	–	0	–	0	–	0	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	12	–	20	–	25	–	30	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	3	–	3	–	3	–	3	–	3	–	ns
t_{CHZ}	Chip Select to Output in High Z[3]	–	9	–	13	–	15	–	20	–	25	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8	–	12	–	15	–	20	–	25	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	ns

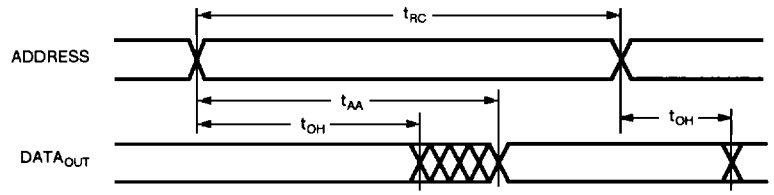
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Preliminary information for -55°C to +125°C temperature range only.

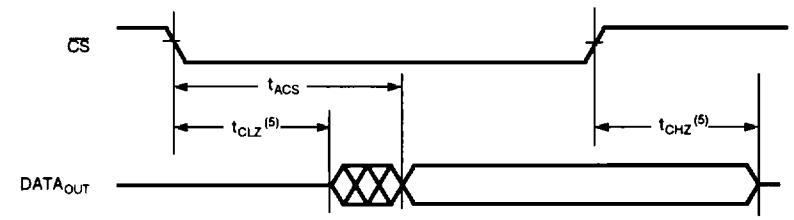
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±200mV from steady state.

ORDERING INFORMATION