SEEQ
Technology, Incorporated

83C97

10BASE-T Ethernet Transceiver With On Chip Filters and Digital Interface and Serial Port

PRELIMINARY

October 1994

SEEQ AutoDUPLEX™ Designation

Symbol indentifies product as AutoDUPLEX device

Features

- *Integrated 10BASET Transceiver With Output Waveshaping And On Chip Filters*
- *Few External Components*
- *Flexible Digital Hub Interface: Clocked or Nonclocked, Single or Differential*
- *Meets All Applicable IEEE 802.3 and 10BASET Standards*
- *Jitter Attenuation On Digital Input*
- *Serial Port for Configuration and Status with Interrupt*
- *Many User Features And Options*
  - *Full Duplex/AutoDUPLEX Mode*
  - *Autopolarity*
  - *Smart Squelch*
  - *Adjustable Transmit Level*
  - *Output High Impedance*
  - *Link Disable*
  - *Long Cable Option*
  - *100/150Ω Cable Interface*
  - *PowerDown*
  - *SQE Disable*
  - *Loopback*
- *Receive Data Valid Output*
- *Status Outputs*
  - *Link*
  - *Transmit Activity*
  - *Receive Activity*
  - *Collision*
  - *Polarity*
  - *Jabber*
  - *Full Duplex*
- *20 Pin PLCC*

Description

The 83C97 is a highly integrated analog interface IC for twisted pair Ethernet applications (10BASET).

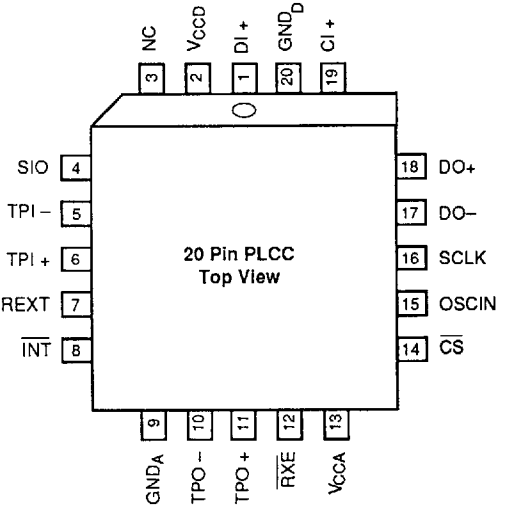
The device consists of transmit waveshaping circuitry, transmit filter, twisted pair line driver, receive filter, twisted pair receiver, a flexible digital interface to an external hub or other device, and a serial port for configuration and status.

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters and common mode chokes normally required in 10BASET applications.

The 83C97 is ideal as a media interface for 10BASET hubs and can also be used for adapter cards.

The 83C96 is implemented in CMOS technology.

Pin Configuration



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Pin Description

Pin No.	Name	I/O	Description
1	DI+	O	Digital Transmit Output. This pin transmits receive TP data.
2	V_{CCD}	--	Positive Supply, Digital. +5 volts.
3	NC		
4	SIO	I/O	Serial I/O Data. This bidirectional pin contains serial port data that is clocked in on rising edges of SCLK and clocked out on falling edges of SCLK.
5	TPI–	I	Twisted Pair Receive Input, Negative
6	TPI+	I	Twisted Pair Receive Input, Positive
7	REXT	--	Transmit Current Set. An external resistor connected between this pin and GND will set the output current supplied on TPO+, TPO–.
8	$\overline{INT}$	O. D. Pullup	Interrupt Output. $\overline{INT}$ is asserted active low whenever there is a change in certain Serial Port Read bits and deasserted after each Serial Port Read operation. This pin consists of an open drain output transistor with a resistor pullup.
9	GND_A	--	Negative Power Supply, Analog. 0 volts.
10	TPO–	O	Twisted Pair Transmit Output, Negative
11	TPO+	O	Twisted Pair Transmit Output, Positive
12	$\overline{RXE}$	O	Receive Data Valid Output $\overline{RXE}$ = 1 No Receive Data $\overline{RXE}$ = 0 Receive Data Valid
13	V_{CCA}	--	Positive Supply, Analog. +5 volts.
14	$\overline{CS}$	I Pulldown	Chip Select Input. This pin enables the serial port for I/O operation. $\overline{CS}$ = 1 Serial Port Deselected $\overline{CS}$ = 0 Serial Port Selected
15	OSCIN	I	Clock oscillator input. There must be either a 20 MHZ crystal or a 20 MHZ clock tied between this pin and GND.
16	SCLK	I	Serial Port Clock Input. This pin shifts serial port data into SIO on rising edges and out of SIO on falling edges.

Pin Description (continued)

PinNo.	Name	I/O	Description
17	DO–	I	Digital Receive Input, Negative. This pin also selects the receive digital interface mode type. DO– = V_{cc} DO+ is single ended, clocked DO– = GND DO+ is single ended, nonclocked DO– = Data DO± is differential, nonclocked
18	DO+	I	Digital Receive Input, Positive.
19	CI+	O	Digital Collision Output, Positive
20	GND_D	--	Negative Supply, Digital. 0 volts.

Functional Description

General

The 83C97 has five main sections: digital transmitter, digital receiver, twisted pair transmitter, twisted pair receiver, and miscellaneous.

The digital receiver receives incoming Manchester encoded data from an external hub controller or other device and converts the data to internal digital levels.

The data then goes to the twisted pair transmitter. The TP transmitter is composed of special circuitry to remove excess jitter, a waveform generator that preshapes the output, a filter to remove high frequency components, and an output driver to drive the 100 ohm twisted pair cable. In addition, the transmitter generates link pulses, start of idle pulses (SOI), and detects the jabber condition.

The twisted pair receiver receives incoming Manchester encoded data from the twisted pair cable, removes high frequency noise from the input, determines if the input signal is a valid packet, and then converts the data from twisted pair levels to internal digital levels. The twisted pair receiver also detects link pulses, detects start of idle (SOI) pulses, detects and corrects for reverse polarity on the twisted pair inputs, implements a squelch algorithm to reject invalid signals, and detects and enables full duplex operation.

The output of the twisted pair receiver then goes to the digital transmitter which drives the data to an external hub controller or other device. There is a second digital transmitter for collision.

The miscellaneous blocks are the crystal oscillator, collision detect circuitry, digital select inputs, digital status outputs, and serial port.

Each block plus the operating modes are described in more detail in the following sections. A block diagram of the 83C97 is shown in Figure 1.

Twisted Pair Transmitter

TP Transmit

The transmitter consists of a jitter attenuator, waveform generator, and line driver.

The jitter attenuator is designed to reduce the jitter that was present on the digital receive input. The jitter attenuator reduces input jitter by typically 0.2, that is, only 20% of the jitter that is present on the digital input propagates to the twisted pair output. This block also synchronizes the digital receiver data transitions to the waveform generator clock.

The purpose of the waveform generator is to preshape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a second order low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM addresses; the ROM addresses are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Section 14 and also shown in Figure 2.

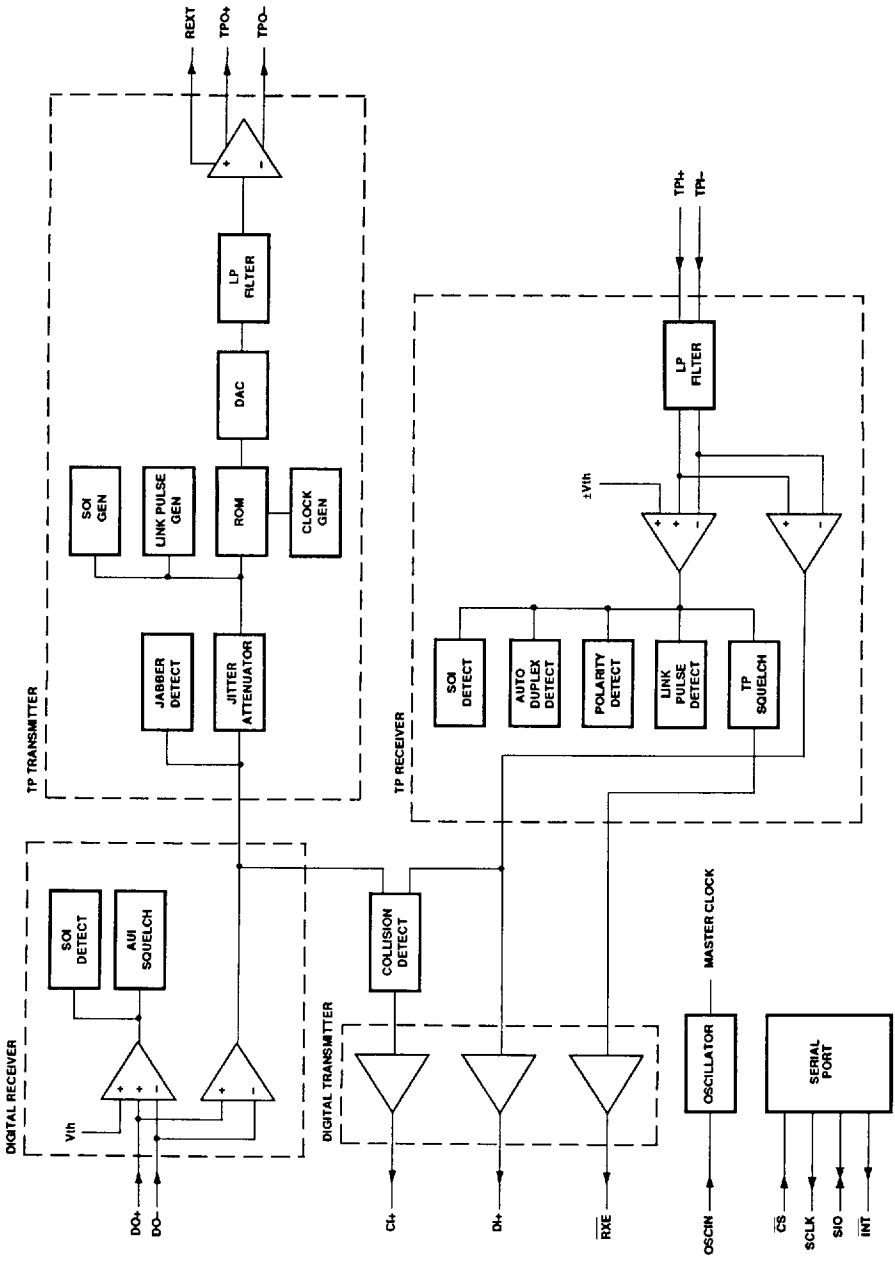

Figure 1. 83C97 Block Diagram

The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the preshaped and smoothed waveform to a current output that can drive the twisted pair cable directly without any external filters.

The 83C97 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications.

During the idle period, no output signal is transmitted on TPO± (except link pulse), but the current sources still remain active, thus eliminating glitches at the beginning and end of packet.

Transmit activity can be monitored through a bit in the serial port. See the Serial Port section for more details.

STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 ohm cable, or shielded twisted pair cable. When STP mode is enabled, the output current is reduced the appropriate amount to keep the amplitude of the transmit signal unchanged from the specified transmit levels and template.

The STP mode can be selected through a bit in the serial port. See the Serial Port section for more details.

TP Receiver

TP Receive

The TP receiver is intended to receive input signals from the twisted pair cable that reside inside the template shown in Figure 3.

The TPI± inputs are internally biased to $V_{cc}/3$ by internal 10K bias resistors. The TPI± inputs pass through a 3rd order low pass filter designed to eliminate high frequency noise on the input.

The receive filter output then goes to two different types of receive comparators, threshold and zero crossing. The threshold comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid data. The output of the threshold comparator is

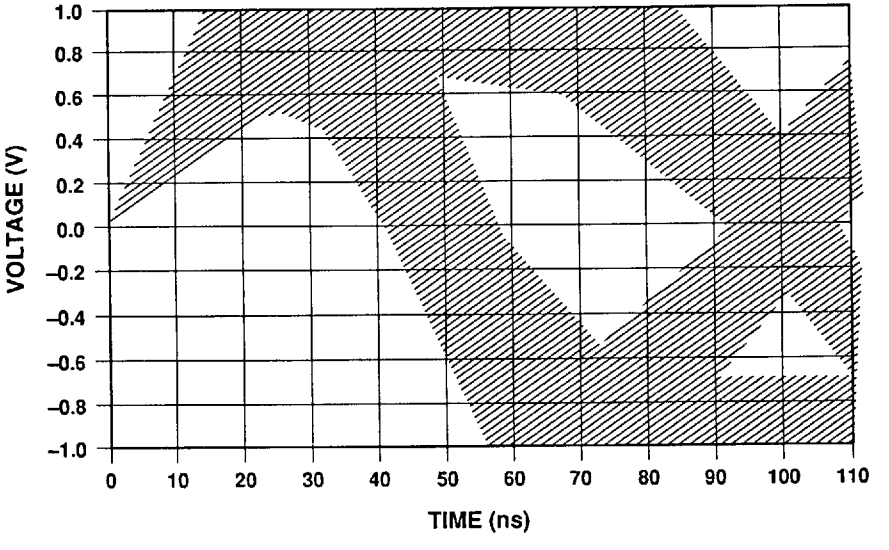

Figure 2. Twisted Pair Output Voltage Template with IEEE 802.3 Line Model.

used for squelch, link pulse detect, SOI detect, reverse polarity detect, and full duplex detect. Each of these are described in separate sections. The output of the zero crossing comparator goes to the digital transmitter.

Receive activity can be monitored through the serial port. See the Serial Port section for more details.

TP Squelch

The threshold comparator compares the TP± inputs against fixed positive and negative thresholds, called squelch levels. The output from the threshold comparators goes to a receive squelch circuit which determines if the receive input data is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 100 - 250 ns interval, the data is considered to be valid and the receiver now enters into the unsquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. While in the unsquelch state, the receive squelch circuit looks for SOI (Start Of Idle) pulse at the end of a packet. When the SOI signal is detected, the receive squelch is turned on again. The receiver meets the squelch requirements defined in IEEE 802.3 Section 14.

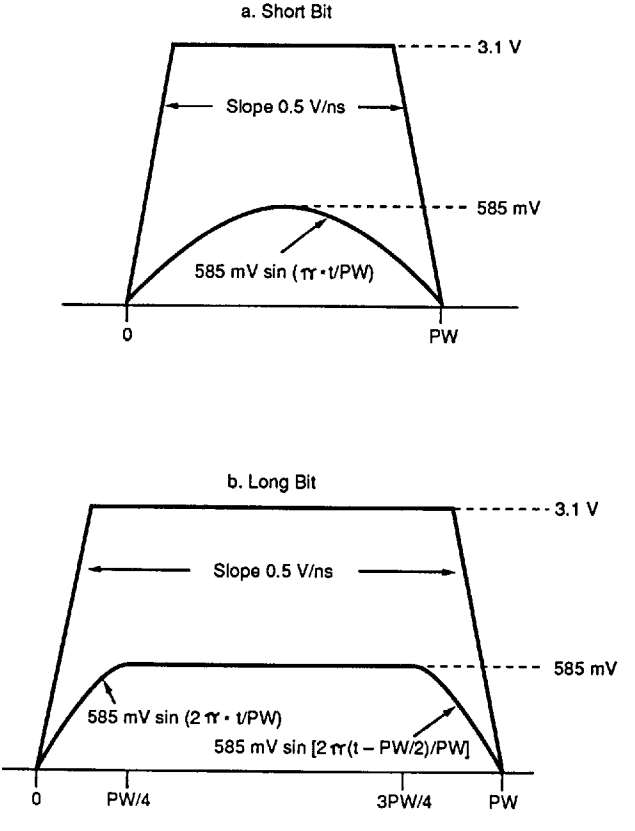

Figure 3. TP Receive Input Differential Voltage Template

Long Cable Mode

The device can support cable lengths exceeding 100 meters by setting a bit in the serial port. See the Serial Port section for more details. When the long cable mode is enabled, the threshold levels of the internal threshold comparators are lowered to accommodate an additional 4.5 dB of cable attenuation.

Digital Transmitter

The digital transmitter consists of three digital output drivers: data, data valid and collision. The data output on pin DI+ contains a digital representation of the TP receive data. The data valid output on $\overline{RXE}$ contains an active low signal that is asserted when the TP receive data is considered valid by the TP squelch circuit. The collision output on CI+ contains a 10 MHz square wave that is asserted when the collision condition is detected. The digital transmitter outputs are not affected by the receive interface mode selection.

Digital Receiver

The digital receive has three possible interface modes to an external hub controller or other device: differential, single ended non-clocked, and single ended clocked. The selection of the digital receiver interface mode is done with the pin DO– as shown in Table 1.

Table 1. Digital Receiver Interface Mode Select

Interface Mode	DO+	DO–
Differential	Data+	Data–
Single Ended Nonclocked	Data	Tie To GND
Single Ended Clocked	Data	Tie To V_{cc}

The differential interface mode is automatically sensed when there are transitions on both DO+ and DO– data input pins. In this mode, data is inputted as differential digital signals on DO+ and DO–. The input voltage trip level on DO± is set to zero volts, differential.

The single ended, non-clocked interface mode is selected by tying DO– to GND and applying data to DO+. In this mode, data is inputted as a single ended signal on DO+. The input voltage trip level on DO+ is set to $V_{cc}/2$.

The single ended, clocked interface mode is selected by tying DO– to V_{cc} and applying data to DO+ In this mode, data is inputted as a single ended signal on DO+ and is clocked in on rising edges of the OSCIN input clock. The input voltage trip level on DO+ is set to normal TTL levels.

In both the differential and single ended, nonclocked interface modes, the input data pulse width on DO± must be at least 20 ns to be considered a valid data pulse.

SOI (Start of Idle)

The SOI pulse is a positive pulse inserted at the end of every transmitted packet to indicate the end of transmission and the start of idle.

Both the TP and digital transmitters must generate SOI pulses. The TP transmitted SOI output pulse is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Section 14 and shown in Figure 4.

The receiver detects the SOI pulse by sensing missing data transition. Once the SOI pulse is detected, the device goes into the idle state.

Link Integrity

The TP transmitter generates link pulses during idle to indicate that the network link is intact. The transmitted link pulses are single positive pulses sent out at 8-24 ms intervals and are preshaped by the transmit waveform generator to meet the pulse template specified in IEEE 802.3 Section 14 and shown in Figure 5.

The TP receiver monitors the TP± pins continuously for valid data and link pulse activity. If neither data nor link pulses are detected, the 83C97 enters the Link Fail State, the TP transmit, digital transmit, and SQE functions are disabled, and collision signals are asserted. For the device to exit the Link Fail State, three consecutive link pulses or one valid data packet need to be detected on the TP± inputs.

Link pulse detection can be monitored through a bit in the serial port. The link pulse function can also be disabled by setting the appropriate bit in the serial port. See the Serial Port section for more details.

Collision

Collision occurs whenever transmit and receive occur simultaneously on TPO± outputs and TP± inputs. Collision is indicated on the 83C97 by transmitting a 10MHz signal on the collision digital transmitter output CI+, and

through a bit in the serial Status Port. The collision signal is also asserted on CI+ when the jabber condition has been detected and when the SQE test is performed. Collision function is disabled if the device is in the Link Fail State.

Signal Quality Error (SQE)

The 83C97 tests the digital transmitter output connection by sending out a 1 µs collision burst on the collision outputs, CI±, after each transmit packet. This is known as the signal quality error (SQE) test.

The SQE test is disabled when the device is in the Link Fail State or when Jabber is detected. SQE can also be disabled by setting a bit in the serial port. See the Serial Port section for more details

Jabber

Jabber condition occurs when the transmit packet exceeds its maximum allowable length. When jabber is detected, the transmit outputs on TPO± are forced to the idle state and collision is asserted.

The Jabber condition is indicated through a bit in the serial port. The Jabber function can also be disabled by setting a bit in the serial port. See the Serial Port section for more details.

Receive Polarity Correction

The polarity of the signal on the receive input twisted pair pins, TPI±, is continuously monitored. If either 3 consecutive SOI or 3 consecutive link pulses indicate incorrect polarity on TPI±, the polarity is internally determined to be incorrect. The 83C97 can automatically correct a detected reverse polarity condition (called autopolarity).

The reversed polarity condition is indicated through a Register/Bit in the serial port. The autopolarity function can also be disabled by setting a bit in the serial port. See the Serial Port section for more details.

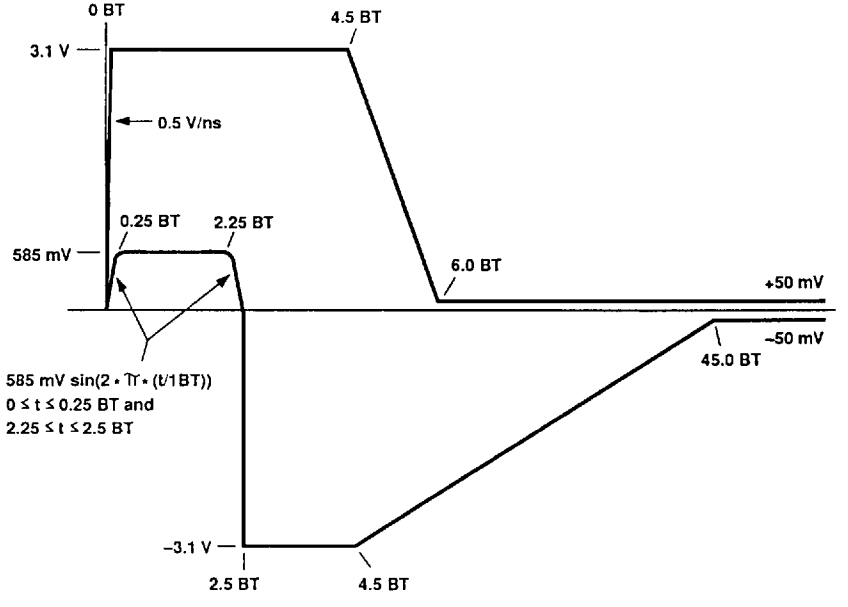

Figure 4. TP Transmit SOI Pulse Voltage Template

Full Duplex Mode

The 83C97 can be configured for full duplex mode. When the device is in the full duplex mode, transmission and reception can occur simultaneously because collision is disabled, internal loopback is disabled, and SQE pulse is disabled.

The device can either be forced into the full duplex mode, or it can detect and place itself into full duplex mode automatically (AutoDUPLEX mode). When the device is in the AutoDUPLEX mode, the transmitter transmits a double link pulse (two link pulses spaced 5 µs apart) every 16th link pulse. The receiver constantly looks for these double link pulses. If the double link pulses are detected by the receiver, the device places itself in the full duplex mode automatically. In this way, the 83C97 can select either full and half duplex without a hardwire jumper.

A Full Duplex detect output is available as a register bit in the serial port. Forced Full Duplex or AutoDUPLEX modes can also be enabled by setting the appropriate serial port bits. See the Serial Port section for more details.

Powerdown

The 83C97 can be powered down by setting a register bit in the serial port. In powerdown mode, the outputs are tristated and the power consumption is reduced to less than 0.5 mW. See the Serial Port section for details.

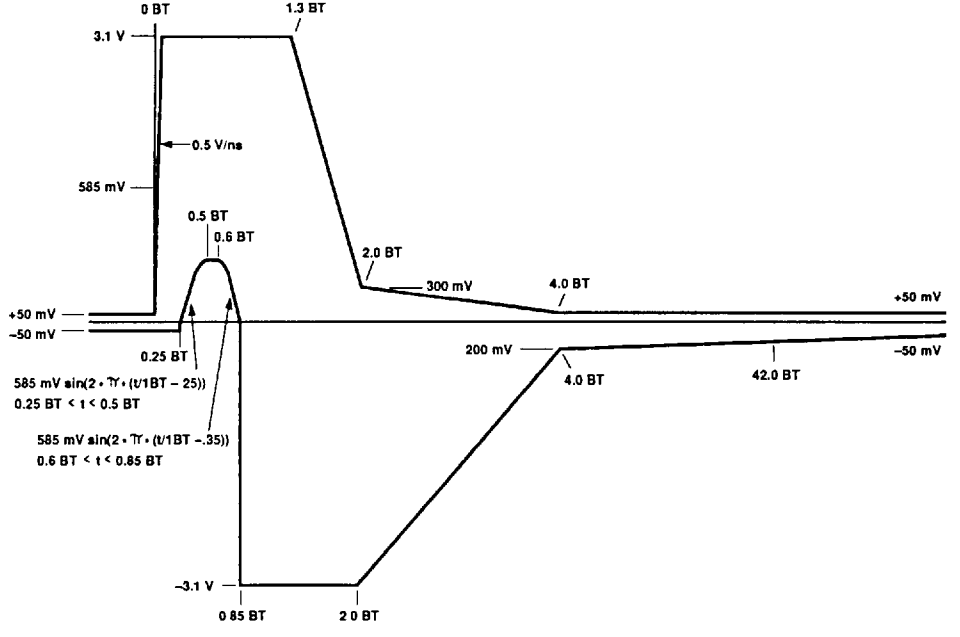

Figure 5. Transmit Link Pulse Voltage Template

Oscillator

The 83C97 requires a 20Mhz reference frequency for internal signal generation. This 20Mhz reference frequency is generated by either connecting an external crystal or an external clock between OSCIN and GND.

Serial Port

A Serial Port was added to the 83C97 to expand the number of configuration inputs and status outputs.

Signal Description

The serial port has four pins, SCLK, SIO, $\overline{CS}$ and $\overline{INT}$. SCLK is the serial shift clock input. SIO is a bidirectional data I/O pin. $\overline{CS}$ is a serial port select input. $\overline{INT}$ is an interrupt output.

Timing

$\overline{CS}$ initiates a serial shift cycle. When $\overline{CS}$ goes low, input data on SIO is written into the device on rising edges of SCLK, and output data is read out onto SIO on falling edges of SCLK. When $\overline{CS}$ goes high, the serial shifting process is halted, the data is latched into the device, and SIO goes into the high impedance state. $\overline{INT}$ is an output pin that goes low whenever any one of the following read bits changes state inside the device: LNK_FAIL, RPOL, FDPLX, JAB, INT. After $\overline{INT}$ is set low, it stays low until another read cycle is done. When the read cycle is completed, the interrupt is cleared forcing $\overline{INT}$ back to high. In addition to $\overline{INT}$ pin, there is also a read register bit for interrupt named INT.

Register Structure

Since the serial port is bidirectional, some bits are write bits and some bits are read bits. Write bits are defined to be inputs, read bits are defined to be outputs. R/IC bits are read bits with interrupt clear capability, or interrupt bits. When an interrupt bit changes state, it automatically latches itself into its register location and interrupt is asserted. The interrupt bit stays latched until the next read cycle when it is updated and interrupt deasserted.

The serial port register structure is shown in Figure 6. Each serial port shift cycle consists of 16 bits. The first eight bits are always write bits (inputs). Depending on the value written to bit 4, R/W, the second eight bits are either write bits (inputs), or read bits (outputs). Bit 0 is always shifted in first. Bits 6 and 7 are high impedance and allow some turnaround time for SIO to change from write to read during read cycles.

The definition of each serial port register bit is shown in Table 2.

0	1	2	3	4	5	6	7
TEST	XMT_DIS	PDN	0	R/W*	0		

If Bit 4 = 0 (Write Bits)

8	9	10	11	12	13	14	15
LNK_DIS	APOL_DIS	SQE_DIS	ADPLX_DIS	FDPLX	LONG	STP	INT_DIS

If Bit 4 = 1 (Read Bits)

8	9	10	11	12	13	14	15
TX_ACT	RX_ACT	COLL	LINK_FAIL	RPOL	FDPLX	JAB	INT

Bit 0 is Shifted First

Figure 6. Serial Port Register Structure

Table 2. Serial Port Register Bit Definition

Symbol	Name	Definition	R/W
TEST	Test Mode Enable	1 = Test Mode Enabled 0 = Normal	W
XMT_DIS	TP Transmit Disable	1 = TP Transmitter Disabled 0 = Normal	W
PDN	Powerdown	1 = Powerdown Enabled 0 = Normal	W
$\overline{R/W}$	Read/Write Select	1 = Read Cycle for Bits 8 - 15 0 = Write Cycle for Bits 8 - 15	W
LINK_DIS	Link Pulse Disable	1 = Link Pulse Function Disabled 0 = Normal	W
APOL_DIS	Autopolarity Disable	1 = Autopolarity Function Disabled (Automatic Reverse Polarity Correction) 0 = Normal	W
SQE_DIS	SQE Test Disable	1 = SQE Disabled 0 = SQE Enabled	W
ADPLX_DIS	AutoDUPLEX Disable	1 = AutoDUPLEX Function Disabled 0 = Normal	W
FDPLX	Full Duplex Enable	1 = Full Duplex Mode Enabled 0 = Normal	W
LONG	Long Cable Mode Enable	1 = Long cable Mode Enabled, Squelch Levels Reduced by 4.5 dB 0 = Normal	W
STP	Shielded Twisted Pair Mode Enabled	1 = STP (150 ohm) 0 = UTP (100 ohm)	W
INT_DIS	Interrupt Disable	1 = Interrupt Function Disabled 0 = Normal	W
TX_ACT	Transmit Activity	1 = Transmit Packet Occurred, Latched for 100 ms 0 = Transmit Idle	R
RX_ACT	Receive Activity	1 = Receive Packet Occurred, Latched for 100 ms 0 = Receive Idle	R
COLL	Collision	1 = Collision Occured, Latched for 100 ms 0 = Normal	R
LNK_FAIL	Link Pulse Fail	1 = Link Pulse Not Detected On Receive TP 0 = Link Pulse Detected	R
RPOL	Reverse Polarity Detect	1 = Reverse Polarity Detected On Receive TP 0 = Normal	R
FDPLX	Full Duplex Detect	1 = Full Duplex Mode Detected 0 = Normal	R
JAB	Jabber Detect	1 = Jabber Detected 0 = Normal	R
INT	Interrupt	1 = Interrupt Bit Changed Since Last Read 0 = Normal	R

APPLICATION INFORMATION

A typical example of the 83C97 in a hub application is shown in Figure 7. The device can also be used in other Ethernet applications provided that the interface to the device is digital.

TP Transmit Interface

The interface between the TP outputs on TPO± and the twisted pair cable requires a transformer and two resistors as shown in Figure 7.

The transformer for the TP transmitter is a 2:1 CT type. Sources for the TP interface transformer are listed in Table 3.

Table 3. TP Transformer Sources

Vendor	Part Number	Telephone
Valor	PT4152	(619) 537-2500
Coilcraft	Q4430-A	(708) 639-6400
PCA	EPE6047S	(818) 892-0761
FEE Filmag	23Z435	(619) 569-6577
Bel Hybrids and Magnetics	A-553-1084-01	(201) 432-0463
NANO Pulse	000-6115-00	(714) 529-2600

Two external 200 ohm 1% resistors are needed between V_{CC} and TPO± to provide a 100 ohm termination impedance when looking back through the transformer from the twisted pair cable. This is shown in Figure 7.

The 83C97 has special circuitry to reduce common mode noise on the twisted pair output. Common mode chokes may not be needed to meet emissions requirements in most applications and have been eliminated from the application schematic in Figure 7.

To minimize noise pickup, the loading on TPO± should be minimized and both outputs should always be loaded equally.

TP Receive Interface

Receive data is typically transformer coupled into the receive inputs on TPI± and terminated with an external resistor as shown in Figure 7.

The receiver requires a 1:1 transformer. Sources for the TP interface transformer are listed in Table 3.

The receive input needs to be terminated with 98 ohms in order to meet input impedance requirements of IEEE 802.3 Section 14. Notice that in Figures 8, the receive input has this input termination resistor broken up into two 48.7 ohm 1% resistors with a 0.1μF capacitor tied between the center points and GND. The optional 0.1μF capacitor is needed if the device is required to meet the receive common mode input AC voltage specification in IEEE 802.3 Section 14. This capacitor attenuates common mode input noise. If the capacitor is not needed, then the two termination resistors can be combined into one 97.6 ohm 1% resistor across TPI±.

In order to minimize noise pickup into the receive path, loading on TPI± should be minimized and both inputs should be loaded equally.

TP Transmit Output Current Set

The TPO± output current level is set by an external resistor tied between REXT and GND. The output current is determined by the following equation where R is the value of REXT:

$$I_{OUT} = (R/10K) * 50mA$$

REXT should be a 1% resistor in order to meet IEEE 802.3 specified levels.

The value of REXT should be ideally set to 10K to meet the templates and levels specified in Section 14 of IEEE 802.3. However, since the output is a current source, capacitive and inductive loading can reduce the output voltage level from the ideal. Thus, in actual application, it might be necessary to adjust the value of this resistor to compensate for the loading involved. For example, if the output loading is 10 pF, the value of the external resistor will have to be reduced to approximately 8.5K to meet the IEEE levels.

Keep REXT as close to the REXT and GND pins as possible in order to reduce noise pickup into the transmitter.

Digital Transmitter Interface

The data on DI+ digital transmitter output is the digital representation of the data received on the TP receive inputs. The internal data path has been carefully laid out to minimize jitter on the data output. To keep the jitter low, the external parasitic load on DI+ should be kept to a minimum.

Since the data on DI+ is Manchester encoded, an external hub controller or other device can look at activity on DI+ to sense beginning of packet and detect SOI to sense end of packet. An alternative way to determine beginning and

end of packet is to use the digital output, $\overline{RXE}$. $\overline{RXE}$ is asserted at beginning of packet and deasserted at the end of packet. Using $\overline{RXE}$ eliminates external circuitry needed to determine start and end of packet, and hence, when the data is valid.

Digital Receive Interface

The digital receiver has three interface types in order to offer a flexible digital interface to a hub controller or other device. The three different modes, as described in the Digital Receiver section, are differential, single ended clocked, and single ended non-clocked. The first two interface types, differential and single ended clocked, provide low jitter methods of transferring data from an external hub controller or other device to the 83C97. The last interface type, single ended non-clocked, is offered because of its simplicity even though it has higher jitter.

The differential interface mode is useful when complementary digital signals are available to the 83C97 on DO± form an external device. The internal data transition is detected when the difference between the DO+ and DO– input voltages crosses zero. This scheme eliminates the data jitter caused by unequal rise and fall times on the digital inputs.

Some external hub controllers or other devices might have only a single ended digital input signal for the data input on DO+. The single ended clocked interface mode allows single ended digital inputs to be clocked into the device on the rising edge of a 20 MHz clock applied to OSCIN. Since the data on DO+ is clocked in on OSCIN rising edges, data jitter associated with the DO+ width variations and rise/fall times is eliminated.

The single ended non-clocked interface mode is the simplest interface mode on the 83C97. It has only a single digital input on DO+. Data presented on DO+ propagates directly through the device. This mode is the simplest but has greater jitter because the pulse width jitter and rise/fall time variations can directly propagate through to the TP transmit output. To reduce jitter on the input DO+, the input trip level is set at $V_{CC}/2$, and a jitter attenuation circuit was placed inside the TP transmitter which reduces the input jitter by 80%, typically.

Oscillator

The 83C97 requires a 20Mhz reference frequency for internal signal generation. This 20Mhz reference frequency can be generated by either connecting an external crystal or an external clock between OSCIN and GND.

If the crystal oscillator is used, it needs only an external crystal. No other external capacitors or other components are required. The crystal must have the characteristics shown in Table 4. The crystal must be placed as close as possible to OSCIN and GND, keeping parasitics to a minimum.

Serial Port

The 83C97 has a serial port in order to expand the number of configuration inputs and status outputs. Most microcontrollers can easily interface to the serial port without any extra logic, as shown in Figure 7. As described earlier, the serial port consists of four signals; SCKL, SIO, $\overline{CS}$, $\overline{INT}$. Since the $\overline{INT}$ pin is asserted with one of the status outputs changes, it eliminates the need to continually monitor the serial port outputs.

Table 4. Crystal Specifications

Parameter	Spec
Type	Parallel Resonant
Frequency	20 Mhz +/- 0.01%
Equivelent Series Resistance	25 ohms max
Load Capacitance	18 pF typ
Case Capacitance	7 pF max
Power Dissipation	1 mW max

Power Supply Decoupling

There are two V_{CC}'s on the 83C96 (V_{CCA} and V_{CCD}) and two GND's (GND_A and GND_D).

V_{CCA} and V_{CCD} should be connected together as close as possible to the device with a large V_{CC} plane.

GND_A and GND_D should also be connected together as close as possible to the device with a large ground plane.

A 0.1 µF decoupling capacitor should be connected between V_{CCA} and GND_A as close as possible to the device pins, preferably within 0.5". The same should be repeated for V_{CCD} and GND_D.

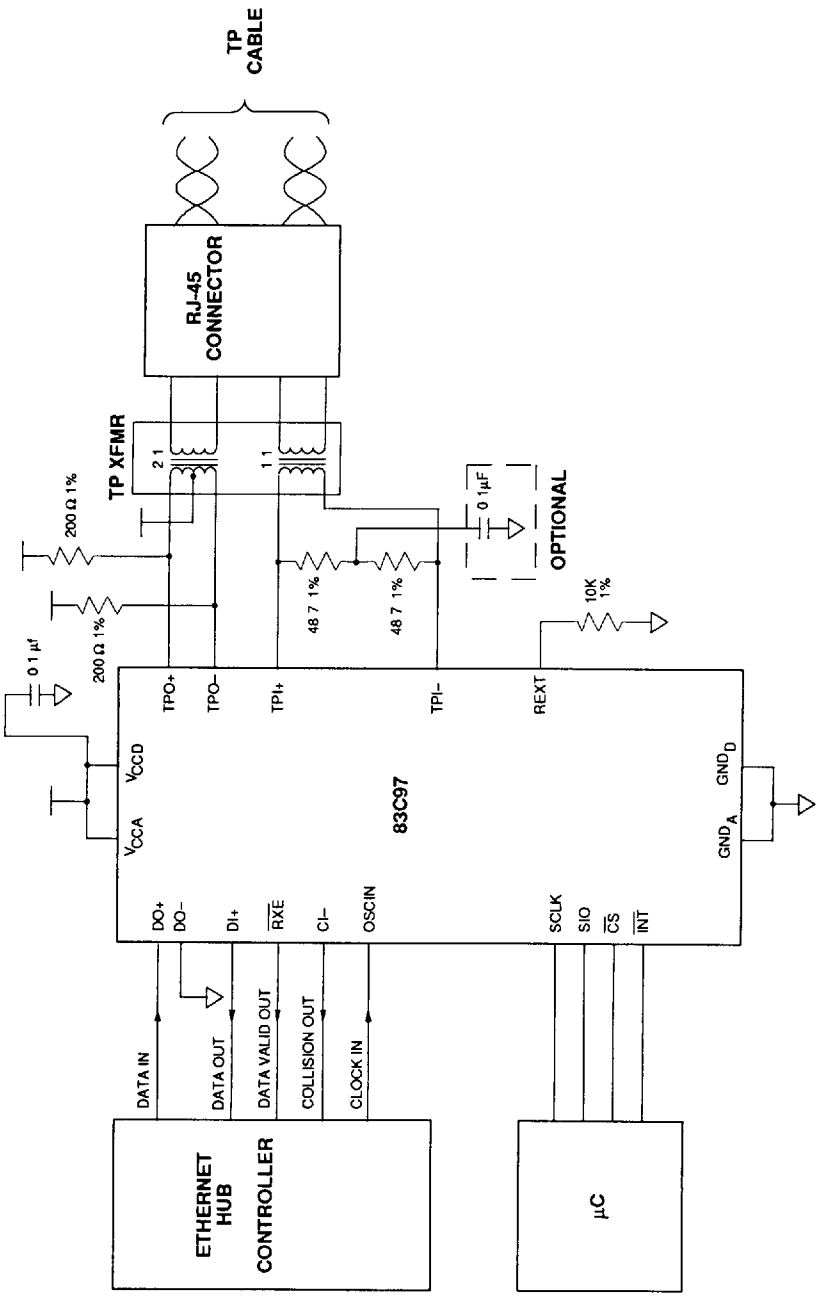

Figure 7. Hub Schematic Using 83C97

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND_A, GND_D unless otherwise specified.

AV_{CC}, DV_{CC} Supply Voltage ..... –0.3V to 7V
All Inputs and Outputs ..... –0.3V to V_{CC} + 0.3V
Input Latchup Current ..... ±25 mA
Package Power Dissipation ..... 1 Watt @ 25°C
Storage Temperature ..... –65 to +150°C
Operating Temperature ..... –65 to +125°C
Lead Temperature (Soldering, 10 Sec) ..... 250°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage			0.8	Volt	All Except OSCIN, DO+ in Single Ended Nonclocked Mode
				1.5	Volt	OSCIN
				2.0	Volt	DO+ in Single Ended Nonclocked Mode
V_{IH}	Input High Voltage	2.0			Volt	All Except OSCIN, DO+ in Single Ended Nonclocked Mode
		3 5			Volt	OSCIN
		3.0			Volt	DO+ in Single Ended Nonclocked Mode
I_{IL}	Input Low Current			–1.0	µA	V_{IN} = GND $\overline{CS}$, SCLK, SIO
				–150	µA	V_{IN} = GND OSCIN
I_{IH}	Input High Current			1.0	µA	V_{IN} = V_{CC} SCLK, SIO
		30	60	120	µA	V_{IN} = V_{CC} $\overline{CS}$
				150	µA	V_{IN} = V_{CC} OSCIN
V_{OL}	Output Low Voltage			0.4	Volt	I_{OL} = –2.0 mA
				1.0	Volt	I_{OL} = –20 mA
V_{OH}	Output High Voltage	4 0			Volt	I_{OL} = 2 0 mA All Except $\overline{INT}$
		2.4			Volt	I_{OL} = 50 µA $\overline{INT}$
C_{IN}	Input Capacitance		5 0		pF	
I_{CC}	V_{CC} Supply Current			150	mA	Transmitting
				0.1	mA	Powerdown Mode

TWISTED PAIR CHARACTERISTICS TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 50 OHM LOAD FROM TPO± TO V_{CC}

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{OV}	TPO± Differential Output Voltage	2.2	2.5	2.8	V pk	
T_{OVT}	TPO± Differential Output Voltage Template	See Figure 2				
T_{SOI}	TPO± SOI Output Voltage Template	See Figure 4				
T_{LPT}	TPO± Link Pulse Output Voltage Template	See Figure 5				
T_{OIV}	TPO± Differential Output Idle Voltage			± 50	mV	
T_{OIA}	TPO± Output Current	44	50	56	mA pk	
T_{OIR}	TPO± Output Current Adjustment Range	30	50	80	mA pk	V_{CC} = 5V Adjustable with REXT
T_{CMA}	TPO± Common Mode AC Output Voltage		10	50	mV pk	
T_{HD}	TPO± Harmonic Distortion			–27	dB	All 1's Output
T_{OR}	TPO± Output Resistance		10 K		Ohm	
T_{OC}	TPO± Output Capacitance		15		pF	

TWISTED PAIR CHARACTERISTICS RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. 10 MHz sinewave on TPI±

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
R_{ST}	TPI± Squelch Threshold	310		540	mV pk	
R_{UT}	TPI± Unsquelch Threshold	190		330	mV pk	
R_{ZT}	TPI± Zero Cross Switching Threshold			±20	mV pk	
R_{OCV}	TPI± Input Open Circuit Voltage	$V_{CC}/3$ –0.25	$V_{CC}/3$	$V_{CC}/3$ +0.25	Volt	
R_{CMR}	TPI± Input Common Mode Voltage Range	$V_{CC}/3$ –1.0		$V_{CC}/3$ +1.0	Volt	
R_{DR}	TPI± Input Differential Voltage Range	V_{SS}		V_{CC}	Volt	
R_{CRR}	TPI± Input Common Mode Rejection Ratio			–20	dB	0 – 10 Mhz
R_{IR}	TPI± Input Resistance	5K			ohm	
R_{IC}	TPI± Input Capacitance		10		pF	

AC TEST TIMING CONDITIONS

Unless otherwise noted, all test conditions are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5V ±5%
3. 20 Mhz ±0.01%
4. REXT = 10K ±1%, no load
5. Input conditions:
   - All Inputs: tr, tf ≤ 10 ns, 20 - 80%
6. Output Loading
   - TPO±: 50 Ohms To V_{CC} On Each Output, 10 pF
   - Open Drain Digital Outputs: 1K Pullup, 50 pF
   - All Other Digital Outputs: 50pF
7. Measurement Points:
   - TPO±, TPI±: 0v During Data, ±0.30V at start/end of packet
   - DO±: 0v (Differential Interface)
     1.5 Volts (Single Ended Clocked Interface)
     2.5 Volts (Single Ended Non-Clocked Interface)
   - DI+, CI+: 2.5 Volts
   - All other inputs and outputs: 1.5 Volts

TRANSMIT TIMING CHARACTERISTICS

Refer To Figure 8 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_1	DO± To TPO± Bit Loss			2.0	BT	
t_2	DO± To TPO± Propagation Delay			200	ns	
t_3	DO± SOI Pulse Width Required For Idle Detection	150		200	ns	
t_4	TPO± SOI Pulse Width To 0.3V Point	225		325	ns	See Figure 4. Measure TPO± from last zero crossing to 0.3V point
t_5	TPO± SOI Pulse Width To 50 mV Point			4500	ns	See Figure 4. Measure TPO± from last zero crossing to 50 mV point
t_6	TPO± Output Jitter			± 8.0	ns	

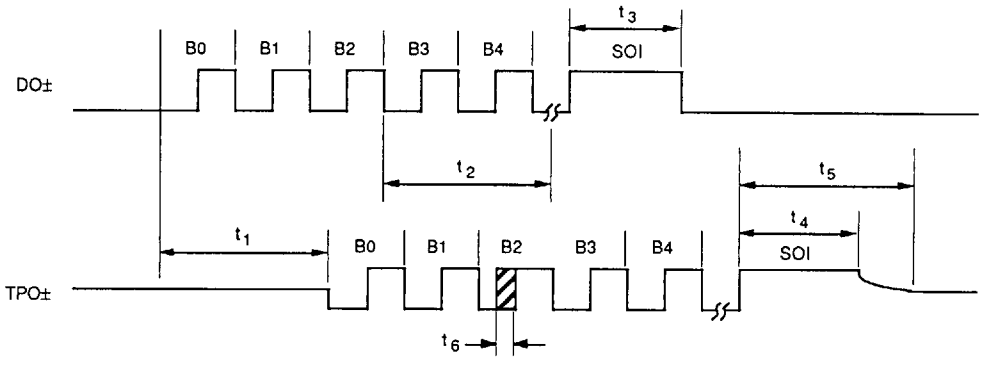

Figure 8. Transmit Section Timing

RECEIVE SECTION TIMING CHARACTERISTICS

Refer To Figure 9 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{21}	TPI± To DI+ Bit Loss			5.0	BT	
t_{22}	TPI± to DI+ Propagation Delay			200	ns	
t_{23}	TPI± SOI Pulse Width Required For Idle Detection	150		200	ns	Measure TPI± from last zero crossing to 0.3V Point
t_{24}	DI+ SOI Pulse Width	225		325	ns	
t_{25}	DI+ Output Jitter			± 1.5	ns	
t_{26}	TPI± to $\overline{RXE}$ Assert			500	ns	
t_{27}	TPI± Stop to $\overline{RXE}$ Deassert			250	ns	

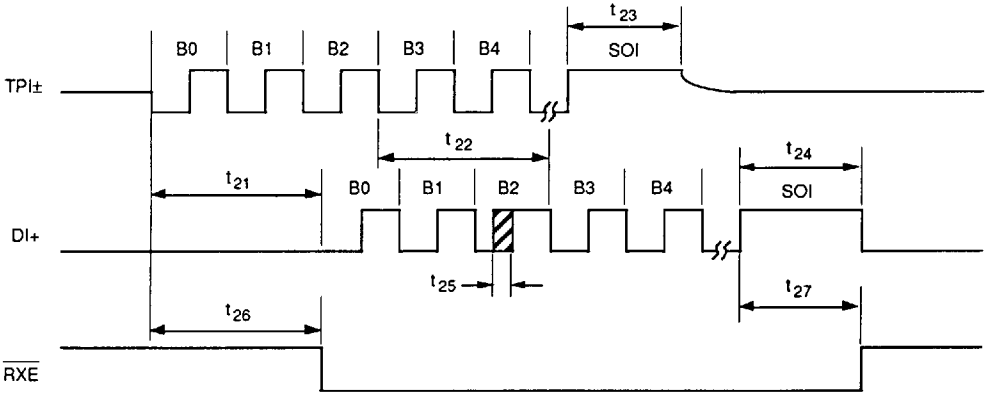

Figure 9. Receive Section Timing

COLLISION TIMING CHARACTERISTICS

Refer To Figure 10 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{31}	Collision Start To CI+ Assert Delay			600	ns	
t_{33}	Collision Start To End Of Loopback On DI+			600	ns	
t_{34}	Collision Start To Start Of Receive Data On DI+			700	ns	
t_{35}	CI+ Cycle Time	99 9	100	100.1	ns	
t_{36}	CI+ Low Or High Time	45	50	55	ns	
t_{37}	Collision Stop To CI+ Deassert			600	ns	
t_{39}	Collision Stop To End Of Receive Data On DI+			600	ns	
t_{40}	Collision Stop To Start Of Loopback On DI+			700	ns	

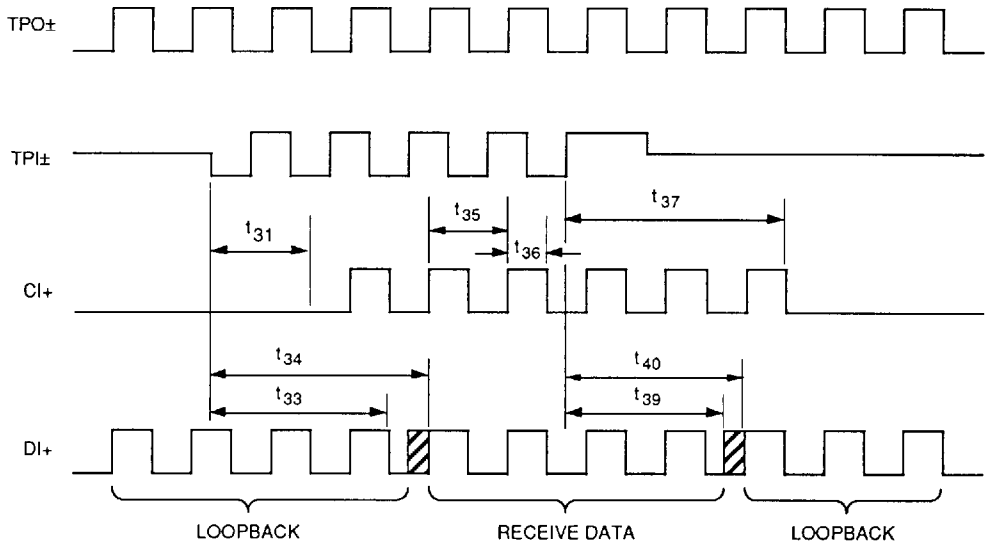

Figure 10. Collision Timing

SQE TIMING CHARACTERISTICS

Refer To Figure 11 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	DO+ SOI to CI+ Assert Delay	0.8		1.2	µs	
t_{52}	CI+ Assert Time	0.8		1.2	µs	

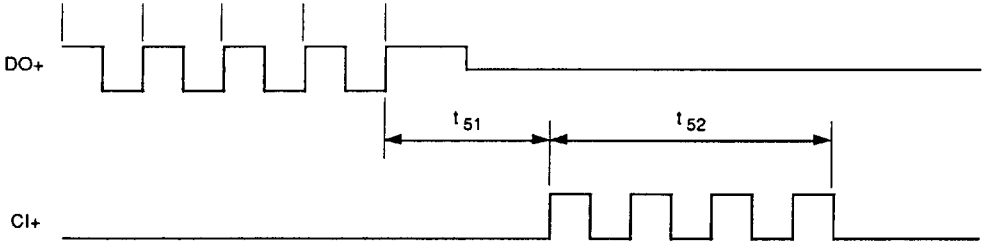

Figure 11. SQE Timing

LINK PULSE TIMING CHARACTERISTICS

Refer To Figure 12 For Timing Diagram

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{61}	Transmit Link Pulse Width	100		150	ns	See Figure 5
t_{62}	Transmit Link Pulse Period	8		24	ms	
t_{63}	Transmit Link Pulse To Double Link Pulse Spacing	5 0	5.2	5.4	µs	Full Duplex Mode
t_{64}	Transmit Double Link Pulse Interval Spacing	16		16	Link Pulses	Full Duplex Mode
t_{65}	Receive Link Pulse Width Required For Detection	50			ns	
t_{66}	Receive Link Pulse Minimum Period Required For Detection	2		7	ms	Link_Test_Min
t_{67}	Receive Link Pulse Maximum Period Required For Detection	50		150	ms	Link_Loss and Link_Test_Max
t_{68}	Receive Link Pulse To Double Link Pulse Spacing Required For Full Duplex Mode Detection	4.8		5.6	µs	Full Duplex Mode
t_{69}	Receive Double Link Pulse Minimum Period Required For Full Duplex Mode Detection	80		120	ms	Full Duplex Mode
t_{70}	Receive Double Link Pulse Maximum Period Required for Full Duplex Detection	380		420	ms	Full Duplex Mode
t_{71}	Receive Link Pulse Assert	2	3	10	Link Pulses	
t_{72}	Receive Full Duplex Assert Delay			7	µs	Full Duplex Mode Detection

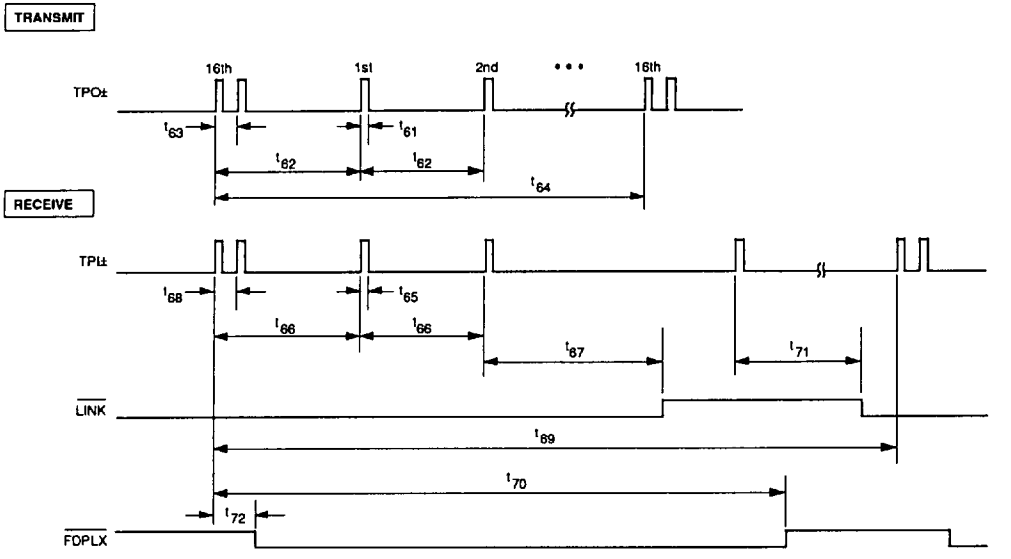

Figure 12. Link Pulse Timing

JABBER TIMING CHARACTERISTICS

Refer To Figure 13 For Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{81}	Jabber Activation Time	20		50	ms	
t_{82}	Jabber Deactivation Time	250		750	ms	

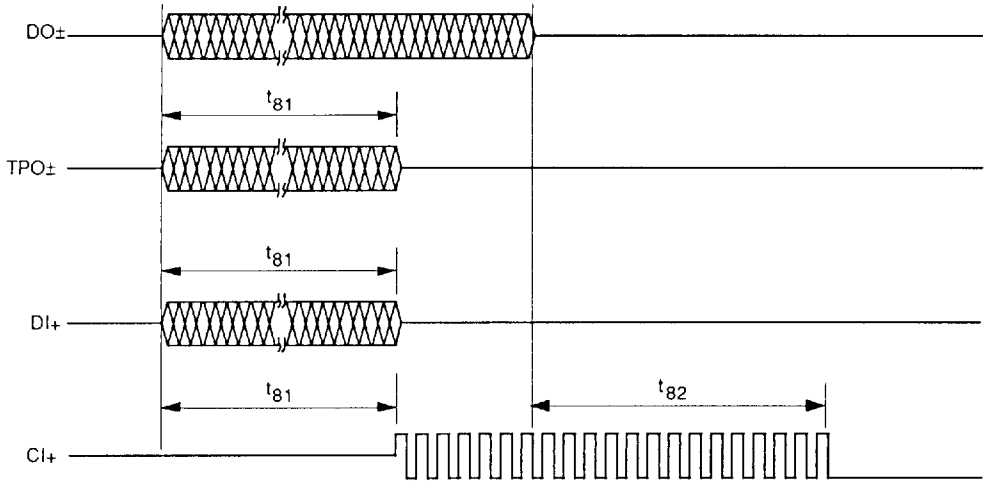

Figure 13. Jabber Timing

SERIAL TIMING CHARACTERISTICS

Refer To Figure 14 For Timing Diagram

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{91}	SCLK Low Time	50			ns	
t_{92}	SCLK High Time	50			ns	
t_{93}	$\overline{CS}$ to SCLK Setup	50			ns	
t_{94}	$\overline{CS}$ to SCLK Hold	50			ns	
t_{95}	$\overline{CS}$ High Time	50			ns	
t_{96}	SIO Setup Time	50			ns	
t_{97}	SIO Hold Time	0			ns	
t_{98}	SCLK to SIO Delay			50	ns	
t_{99}	$\overline{CS}$ Deassert to SIO Tristate			50	ns	
t_{100}	$\overline{CS}$ Deassert to $\overline{INT}$ Transition			100	ns	

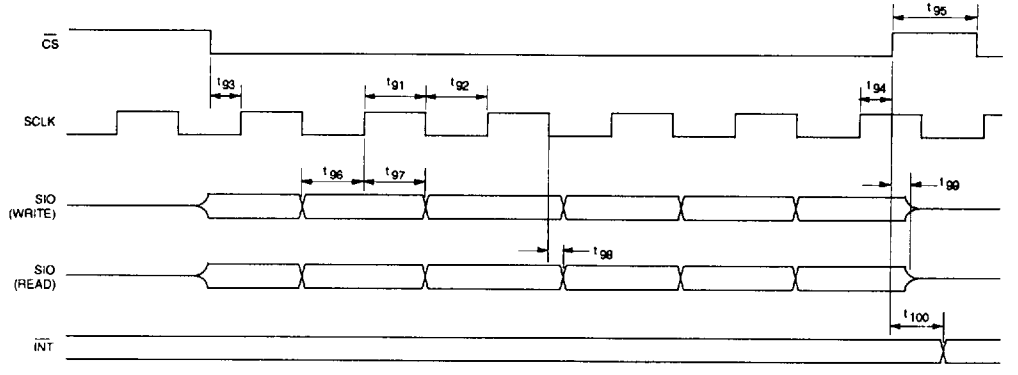

Figure 14. Serial Status Port Timing

Ordering Information

PART NUMBER

N	Q	83C97

- 83C97: PRODUCT: 83C97 10BASE-T Ethernet Transceiver
- Q: TEMPERATURE RANGE: = 0° to 70° C
- N: PACKAGE TYPE : N = 20 PIN PLCC

SEEQ AutoDUPLEX Designation

Symbol indentifies product as AutoDUPLEX device