

1 MEG DRAM

(Micron 1 MEG DRAM Family)

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We're building our reputation on innovation.

917588 997590 1M
 MT1001, MT1002 1M (1,048,576 x 1) BIT DYNAMIC RAM
 997589
 MT4256, MT4257 262,144 x 4 BIT DYNAMIC RAM

PIN ASSIGNMENT (TOP VIEW)

FEATURES

- Industry standard x1 and x4 pin-out, timing, function and package
- High performance CMOS silicon gate process
- Single +5V ±10% power supply
- Low power, 3mw standby, 175 mw active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms (every 16μ sec)
- Refresh modes: $\overline{\text{RAS}}$ only, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ and hidden
- Slow edge rates allowed on all inputs
- Optional Page Mode or nibble mode cycle
- On-chip single bit Error Correction using Hamming Code

OPTIONS

- Timing
 - 80ns access
 - 100ns access
 - 120ns access
 - 150ns access

- Packages
 - Plastic DIP
 - Ceramic DIP
 - Plastic ZIP
 - Plastic SOJ

Additional Access Modes

Page Mode MT1001, MT4256
 Nibble Mode MT1002, MT4257

Order Examples:

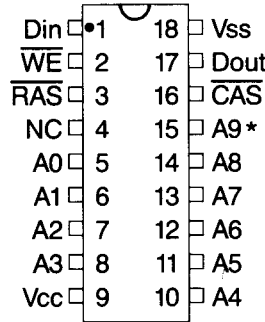
1 MEG x 1, 100ns access, nibble mode in Plastic DIP = MT1002-10
 256K x 4, 120ns access, page mode in Plastic ZIP = MT4256Z-12

005981

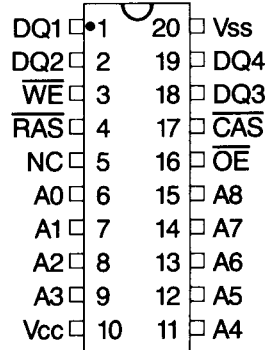
* Address not used for RAS only refresh.

* CMOS memory, 1M (1mx1) DRAM
 * CMOS memory, 1M (256Kx4)

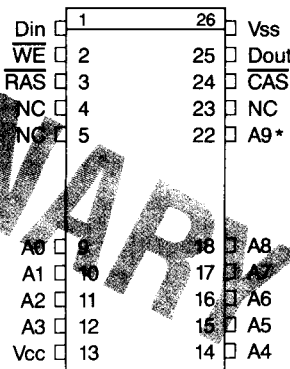
MT1001, MT1002 18 Pin DIP



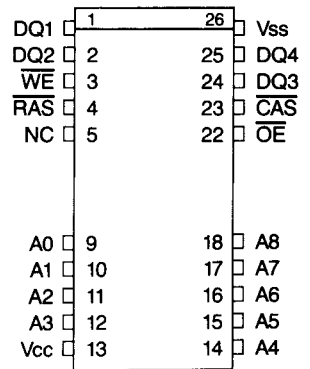
MT4256, MT4257 20 Pin DIP



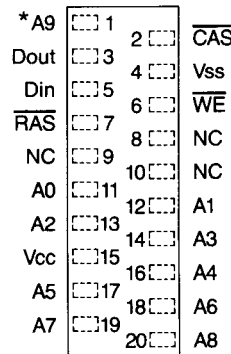
26 Pin SOJ



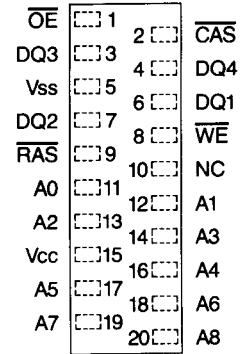
26 Pin SOJ



20 Pin ZIP



20 Pin ZIP



The Micron 1 MEG DRAM family is manufactured and quality controlled in Micron's modern Boise, Idaho USA facility using its low power, high performance CMOS silicon gate process. They are functionally equivalent to other manufacturer's products meeting JEDEC standards. Several parameters are sampled; however, functionality is consistently assured over a wider power supply, temperature and refresh range than specified. Each unit receives accelerated burn-in and several hours of AMBYX™ system level testing prior to final test and shipment.

Please contact the factory for technical, test and application assistance. Micron can also furnish the representative and distributor nearest you. Micron's QUALITY ASSURED policy is to offer prompt, accurate and courteous service while assuring quality and reliability. The success of our memory business depends on the success of your application.

GENERAL DESCRIPTION

The Micron 1 MEG DRAM family are randomly accessed solid-state memories containing 1,048,576 bits organized in a $\times 1$ or $\times 4$ configuration. In addition to the 1,048,576 bits available to the user, the memory contains 327,680 additional bits used for "real-time" internal error correction using a (16,21) Hamming Code. This error correction process, while offering significant advantages, is transparent to the user. Each bit is uniquely addressed through the 20 address bits which are entered 10 bits at a time (4 data bits are uniquely addressed with 18 address bits in the $\times 4$ configuration). \overline{RAS} is used to latch the first 10 bits and \overline{CAS} the latter 10 bits (9 address bits each time in the $\times 4$ version). In the $\times 4$ configuration 4 DATA inputs and 4 DATA outputs are routed through 4 pins using common I/O. Pin direction is controlled by \overline{OE} . Schmitt triggers have been added to all input control lines, a feature which allows slow edge rates on all inputs to assure microprocessor compatibility. Memory cell data is retained in its correct state by maintaining power and executing a refresh cycle (\overline{RAS} only, \overline{CAS} -before- \overline{RAS} or hidden) at least every 16 μ sec so that all 512 combinations of \overline{RAS} addresses are executed at least every 8msec (regardless of sequence).

Error Correction Coding

The Micron 1 MEG DRAM family incorporates an innovative feature called error correction coding (ECC). ECC utilizes a technique based on the Hamming Code that includes an additional 5 check bits for each 16 information bits resulting in a base die of 1,376,256 total bits. With each data access the chip's circuitry automatically accesses a 21-bit word composed of 16 data bits and 5 check bits. Upon the occurrence of a single bit error in any one of the 65,536 (21 bit) words, the 5 check bits are sufficient to identify the error location and correct the bit by complimenting it. The correction occurs whenever a word is user selected for READ or WRITE operations so that errors are corrected before being presented to the output pin(s) or written to memory. The result is enhanced data integrity (noise and soft errors are minimized). This enhancement is achieved while retaining complete JEDEC compatibility so that Micron's DRAM may be interchanged with those of other vendors.

OPTIONAL ACCESS CYCLES

Page Mode

Page mode operation allows faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a \overline{RAS} address (A0-A9) defined Page boundary. The page cycle is always initiated with a row address strobed in by \overline{RAS} followed by a column address strobed in by \overline{CAS} . By holding \overline{RAS} low, \overline{CAS} may strobe in different column addresses executing faster memory cycles. Returning \overline{RAS} high terminates the memory cycle.

Nibble Mode

Nibble mode operation allows faster sequential serial data operation (READ, WRITE or READ-MODIFY-WRITE) on up to 4 bits. The first of 4 bits is accessed in the usual manner with \overline{CAS} address A9 (nibble MSB) and \overline{RAS} address A9 (nibble LSB) selecting one of 4 bits within a nibble for initial access. By holding \overline{RAS} low, \overline{CAS} can be toggled incrementing the nibble address field in modulo 4 fashion with wrap around.



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