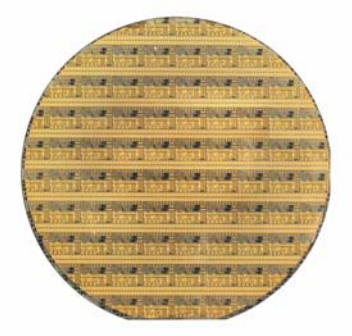
1340TL-S05D
TIA / LIA with RSSI
Data Sheet



Applications

- SONET OC-192 and SDH STM-64 transponders
- Short, intermediate, long reach, and long haul optical receiver modules
- 10 Gbps Ethernet
- Broadband instrumentation

Features

- Supports data rates up to 12.5 Gbps
- 12 kΩ differential electrical gain
- Input-referred noise density 10 pA/rt Hz
- Input overload current 4 mApp
- Output voltage 440 mVpp
- Adjustable DC offset control
- Typical input sensitivity: –19 dBm (ρ = 0.85 A/W, ER = 9 dB)
- Squelch/output enable
- Fast rise and fall times: 17 ps
- Low power consumption: 165 mW
- Receive signal strength indicator (RSSI)
- Single +3.3 V power supply
- Available in die form (980 µm x 980 µm)
- Simplified assembly with through-wafer vias on ground pads

Description

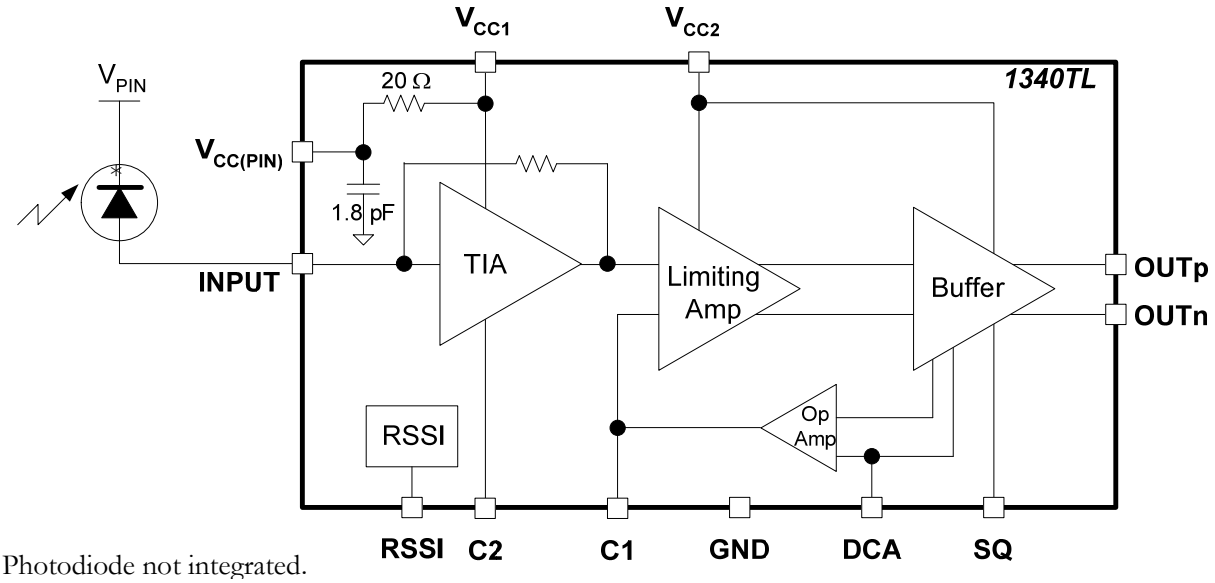
The 1340TL transimpedance amplifier / limiting amplifier (TIA/LIA) is designed to support data rates up to 12.5 Gbps. This device is intended for use with PIN photodetectors and is capable of amplifying input currents from 20 µA to 5 mA with low duty cycle distortion. The 1340TL exhibits a typical input sensitivity of –19 dBm while maintaining a BER of 10^{-12}.

With 12 kΩ of differential gain, the 1340TL eliminates the need for a stand-alone LIA to amplify signals from a TIA. The output level of the TIA/LIA ranges from 200 mV (minimum input) to 440 mV peak-to-peak. This part has RSSI to help align fiber and monitor the input power level, an output enable to allow system debugging, and an adjustable DC offset to allow for adjustment of the decision threshold of the limiting amplifier. The DC offset level is automatically adjusted to 50% of eye crossing if no adjustments are made to the DCA pin.

The 1340TL has fast rise and fall times and low power consumption. The TIA/LIA uses a single +3.3 V power supply and is available in die form.

Through-wafer vias provide very low inductance ground connections to the 1340TL for maximally flat frequency response and high output return loss. This allows for the elimination of the ground bond wires.

Block Diagram



* Photodiode not integrated.

Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min	Max	Unit
Power Supply Voltage	V_{CC}		---	4	V
Continuous Input Current	---		---	10	mA
DCA Voltage[1]	V_{DCA}		-10	10	V
Junction Temperature	T_J		---	+175	°C
Shipping/Storage Temperature	T_{STORE}		–40	+125	°C

Notes:
[1] DCA is self-adjusting. Only apply V_{DCA} if different eye crossing is required.

Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	± 5% Tolerance	+3.135	+3.300	+3.465	V
Power Supply Current	I_{CC}		---	50	65	mA
On-Chip Power Dissipation	P_D		---	165	225	mW
Operating Temperature (Ambient)	T_A		-10	---	+85	°C

Electrical Specifications

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.
Electrical specifications based on *Photodiode Specification Assumptions* on Page 5.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Data Rate		10^{-12} BER (NRZ format)	10.7	---	---	Gbps
Small Signal Transimpedance	Z_T	Differential peak-to-peak, f = 100 MHz	8	12	16	kΩ
Input Current[1]	I_{IN}	peak-to-peak	0.02	---	4	mApp
Differential Output Amplitude (Limited)[1]	$V_{OUTp} - V_{OUTn}$	Differential peak-to-peak, For I_{IN} > 0.05 mApp	360	440	550	mVpp
Differential Output Voltage (Squelched)	$V_{OUTn} - V_{OUTp}$	SQ = GND	---	220	275	mV
Small Signal Z_T BW (3 dB)	BW		8.0	10	12.5	GHz
Low Frequency Cutoff[2]	f_{Low}	With 0.47 µF capacitor from C1 pad to GND and with 0.1 µF capacitor from C2 pad to GND	---	25	---	kHz
Rise/Fall Time	t_r/t_f	20–80% for I_{IN} > 0.1 mApp	---	17	20	ps
Input-Referred RMS Noise	IN_{rms}	10 GHz BW	---	0.9	1.3	µA
Input-Referred Noise Density	I_{ND}	RMS noise per 10 GHz noise bandwidth	---	9	13	pA/rt Hz
Input Sensitivity		@ 10.7 Gbps (ρ = 0.85 A/W, ER = 9 dB)	---	–19	---	dBm
Added Deterministic Jitter	J_T	200 µA < I_{IN} < 3 mApp	---	5	10	ps
Random Jitter	J_R		---	---	0.8	ps RMS
Output Return Loss[3]	RL_{OUT}	< 8.5 GHz	10	---	---	dB
Output Ripple	r_{OUT}	Measured with a probe card in a 50 Ω environment.	–0.5	---	0.5	dB
Peaking[4]		Measured with a probe card in a 50 Ω environment.	---	---	1	dB
Group Delay Variation		50 MHz – 10 GHz	---	---	± 10	ps
Input DC Level	V_{INPUT}	Generated on chip	---	1.35	1.5	V

Electrical Specifications (cont'd)

Electrical specifications guaranteed when the part is operated within the specified operating conditions. **Electrical specifications based on *Photodiode Specification Assumptions* on Page 5.**						
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
RSSI Gain[5]	G_{RSSI}	Small signal AC (<100 µA)	---	30	---	kΩ
		DC & large signal AC	---	500	---	Ω
Squelch V_{IL}	V_{SIL}	Output is disabled	---	0	0.8	V
Squelch V_{IH}	V_{SIH}	Output is enabled	1.5	(open)	---	V
DCA Current Draw[6]	I_{DCA}		-100	---	100	µA

Notes:

[1] Output fully limited for inputs greater than 50 µApp. Refer to Figure 2.

[2] Can be increased or decreased by adjusting external capacitor.

[3] Output return loss is sensitive to V_{CC} and GND bonding wires length. Keep below 250 µm for best performance.

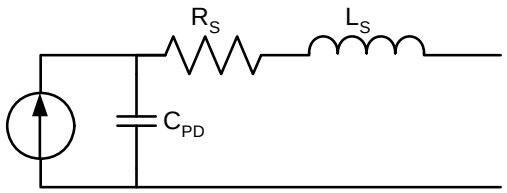
[4] Depends on input bond wire length and photodiode characteristics.

[5] Refer to Figures 3 and 4. RSSI gain is defined as $\Delta V_{RSSI} / \Delta I_{INaverage}$. Small signal gain, as defined, depends on extinction ratio of the input signal.

[6] DCA is self-adjusting. Only apply V_{DCA} if different eye crossing is required.

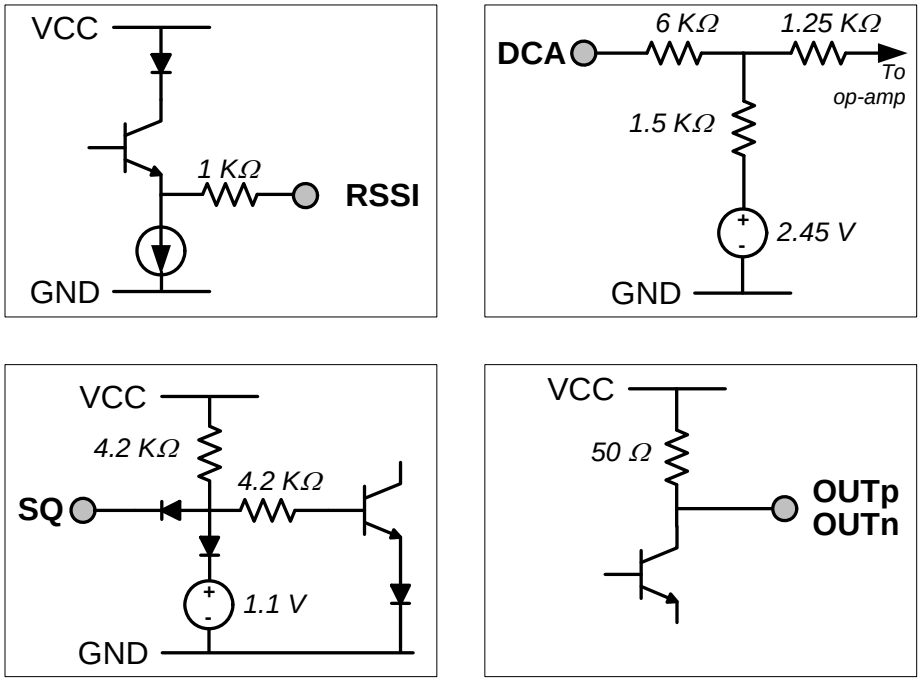
Photodiode Specification Assumptions

Parameter	Symbol	Typ
Photodiode Capacitance	C_{PD}	0.20 pF
Photodiode Resistance	R_S	20 Ω
Photodiode and Bondwire Inductance	L_S	1 nH
Photodiode Responsivity	ρ	0.85
Modulation Extinction Ratio	ER	9 dB



Photodiode electrical model

I/O Equivalent Circuits



Equivalent circuits for 1340TL inputs and outputs

Typical Operating Characteristics

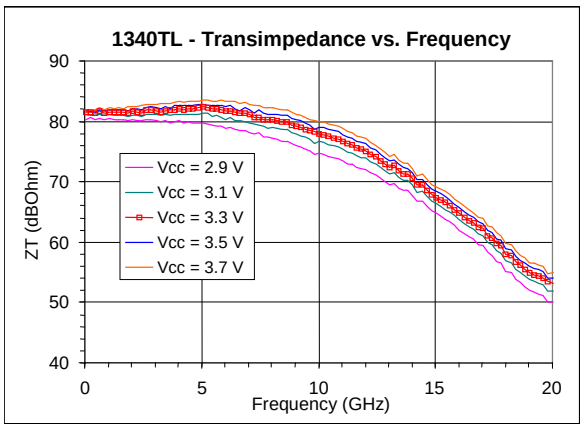


Figure 1. Differential transimpedance vs. frequency and V_{CC}. Z_T computed from measured S parameters with photodiode model defined under "Photodiode Specification Assumptions".

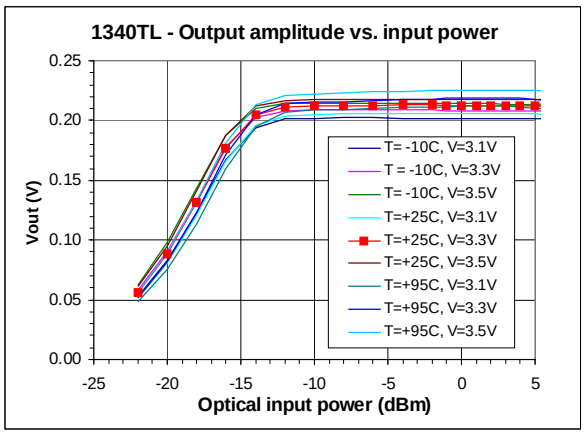


Figure 2. Output amplitude vs. input power. Photodiode responsivity R = 0.66 A/W, extinction ratio ER = 13.2 dB

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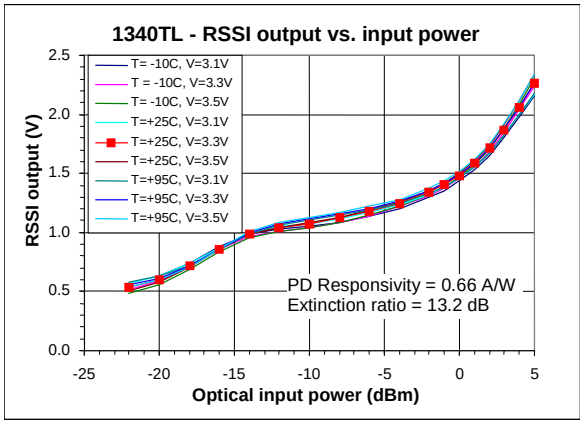


Figure 3. RSSI output vs. input power.

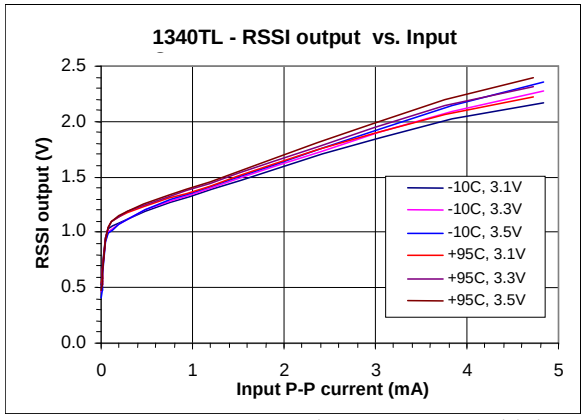


Figure 4. RSSI output vs. input current at high input signal level.

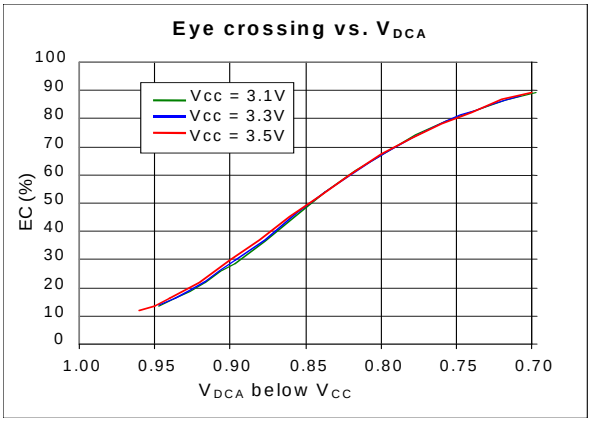


Figure 5. Eye crossing vs. voltage at DCA pin.

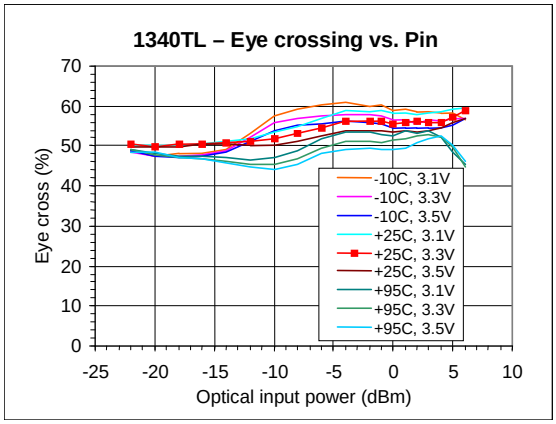


Figure 6. Eye crossing vs. input power. Measured with optical probe.

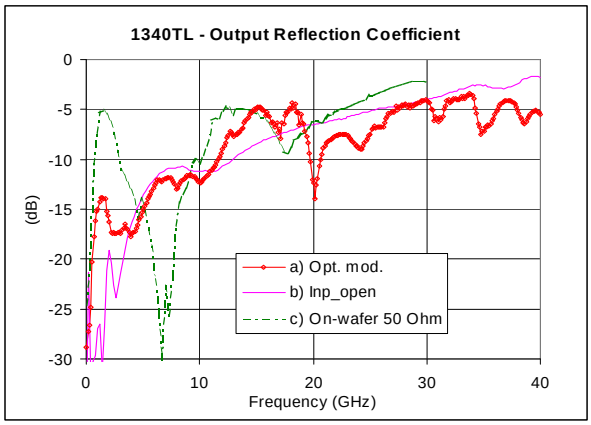


Figure 7. Output reflection coefficient measured under various conditions:
a) die and photodiode mounted in a metal package;
b) on-wafer with input open;
c) on-wafer with input terminated into 50 Ω.

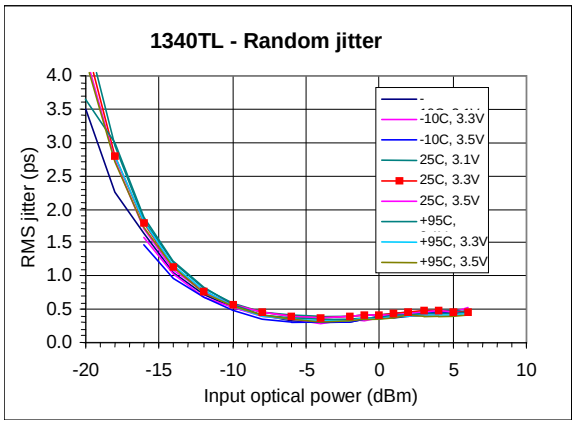


Figure 8. Random jitter vs. input power. Measured with optical probe.

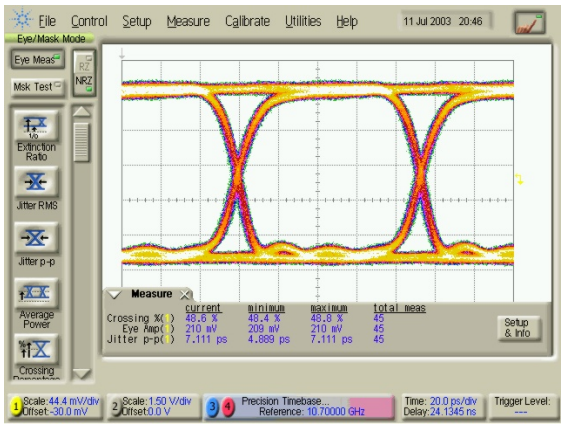


Figure 9. Eye diagram for eye cross (EC) set at 50% (or DCA pin open).

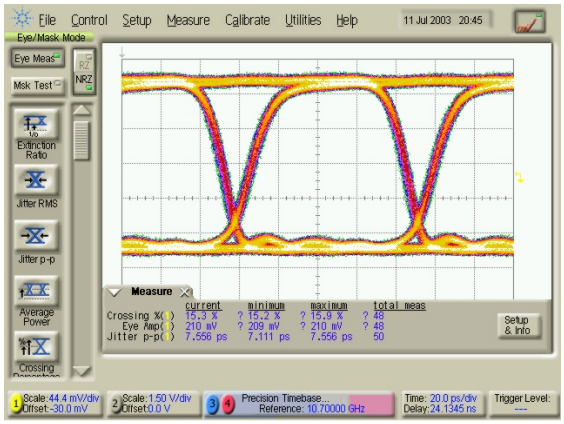


Figure 10. Eye diagram with EC set at 15%.

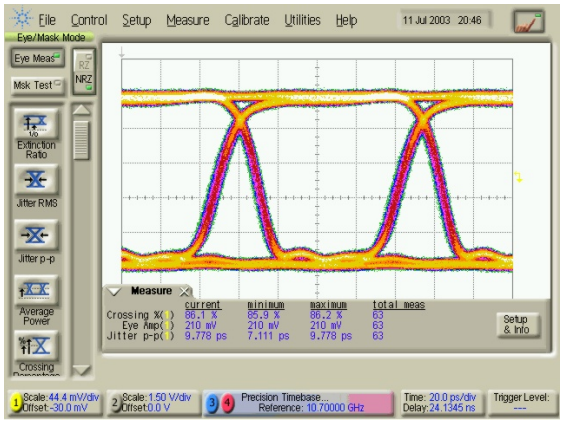


Figure 11. Eye diagram with EC set at 86%.

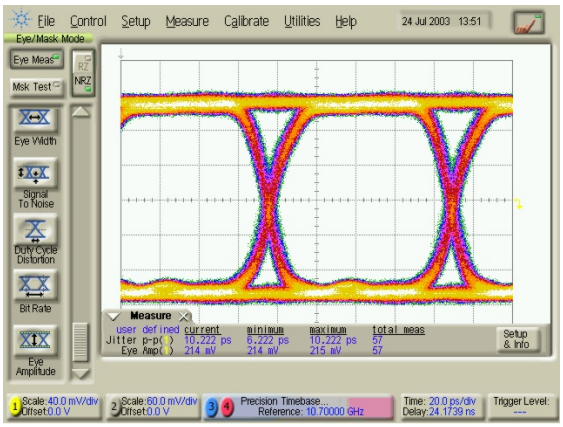


Figure 12. Eye diagram at 3 mApp input current. Source peak-to-peak total jitter is 8.8 ps.

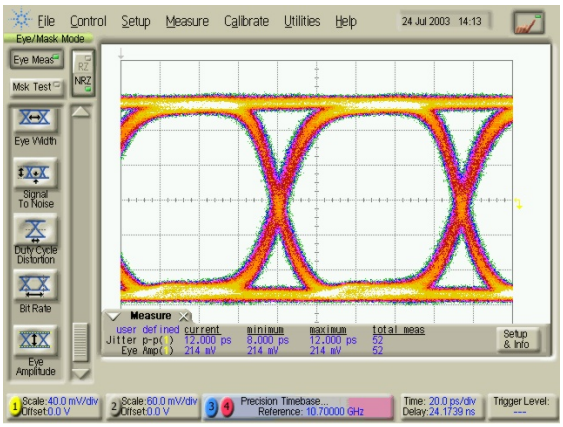


Figure 13. Eye diagram at 100 µApp input current with DCA pin floating. Measured Eye source jitter: 8.9 ps peak-to-peak total jitter.

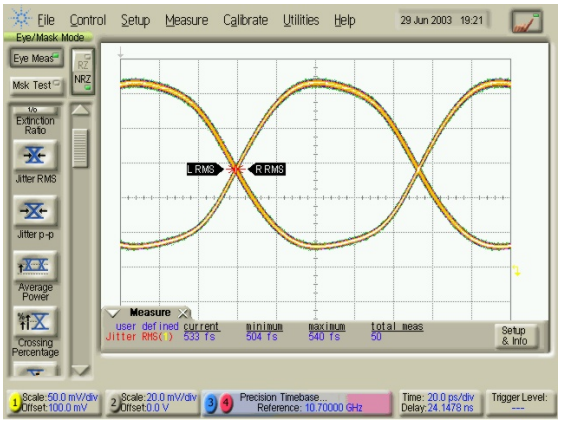


Figure 14. Eye diagram for 0101.. pattern – random jitter measurement.

NOTE: Eye diagrams shown in Figures 9 through 13 were obtained at wafer probe in a 50 Ω environment. Eye diagram in Figure 14 was obtained on-wafer with optical input probe consisting of a photodiode mounted in a GSSG coplanar probe. Total probe capacitance = 0.35 pF.

RSSI Circuit Operation

The 1340TL transimpedance amplifier contains a receive signal strength indicator (RSSI) circuit to facilitate fiber alignment as well as the monitoring of the optical input signal level and modulation.

The RSSI circuit consists of two subcircuits: Block 1 and Block 2. Block 1 corresponds to the AC component of the input signal and operates with high gain over a relatively narrow range of input signals (5–80 µA typ). The output from Block 1 depends on the peak-to-peak amplitude of the input current and thus on the modulation (extinction ratio) of the incoming light. The output of Block 2 is proportional to the DC component in the input signal and hence optical power on average is independent of extinction ratio. The outputs of the two blocks are added together to produce the RSSI output as shown in Figure 15.

The high gain of Block 1 enables the detection and monitoring of relatively low input signals and helps to align the fiber during optical module assembly

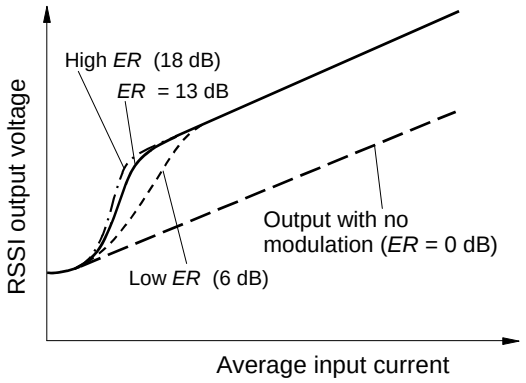


Figure 15. Simplified response at the RSSI output for various modulation conditions.

Output Squelch

The SQ pad may be used to enable or disable (squelch) the output pads. To enable the outputs (normal operation), SQ may be left floating, or connected to a LVTTL/CMOS compatible "HIGH" level (i.e. +3.3 V). To disable the outputs (squelched operation), SQ should be connected to a LVTTL/CMOS compatible "LOW" level (i.e. ground).

Eye-Cross Level Adjustment

The DCA pad may be used to adjust the crossing level in the output eye diagram. When the DCA pad is left open, the eye-cross (EC) level is typically 50 ±5 % over the entire input signal range, and the voltage at the DCA pad is approximately 0.85 V below V_{CC}, i.e. 2.45 V for V_{CC} = 3.3 V. External voltage applied to the DCA input will shift the eye crossing as shown in Figure 5 (see pg. 7). The DCA input is referenced to V_{CC}, i.e. the EC level remains constant when the voltage between V_{CC} and the DCA pad is held constant, even as V_{CC} changes. The DCA pad typically has an input resistance of 7 kΩ with an input current of zero when V_{DCA} = 0.85 V below V_{CC}. The DCA input current ranges from –15 to +15 µA over the full EC level adjustment.

Suggested connections for DCA control are shown in Figure 16 (note the V_{CC} referenced connection).

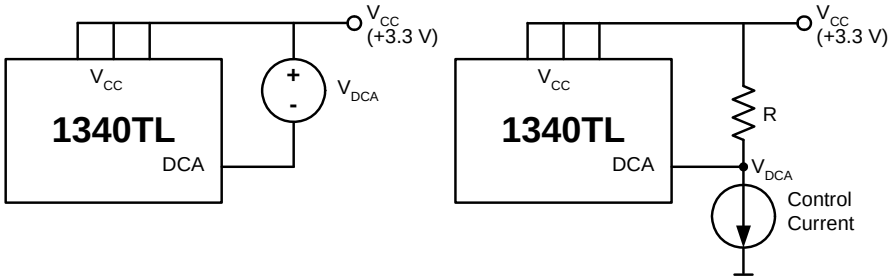
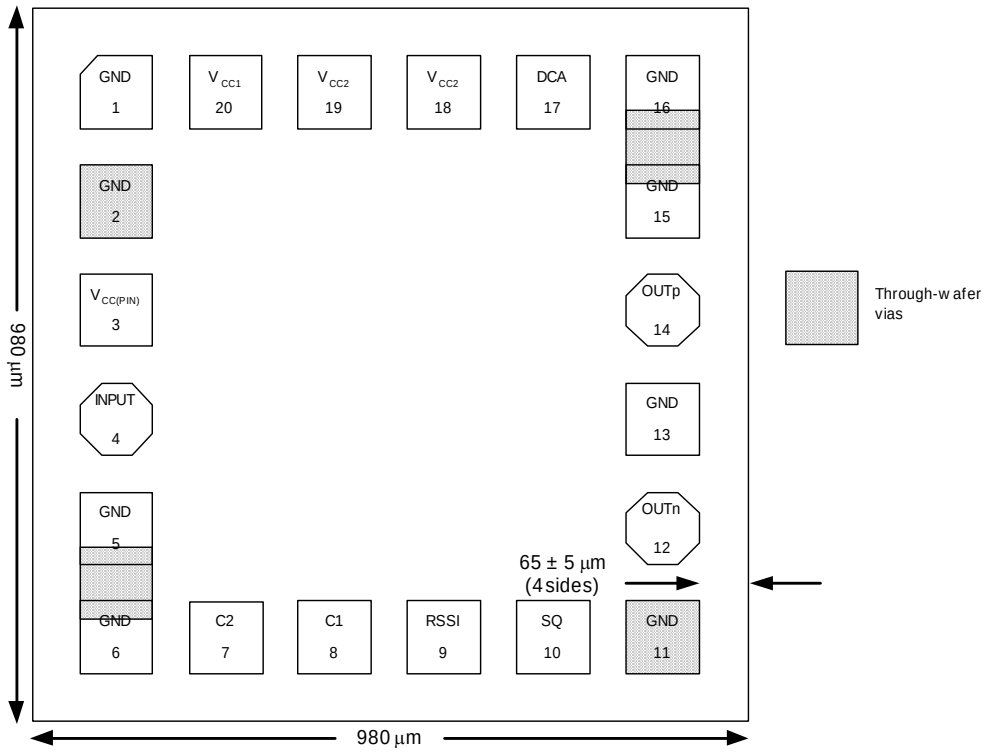


Figure 16. Suggested implementations of DCA control

Die Pad Layout



Notes:

[1] Die size: 980 µm x 980 µm nominal.

[2] 100 µm pads on 150 µm pitch.

[3] 65 ± 5 µm pad frame border.

[4] 110 ± 10 µm die thickness.

[5] Backside of die is metalized.

[6] Metalization covering through-wafer vias cannot be contacted from top-side of die.

Name	Pad	Description	Function
INPUT	4	Data input from photodiode	Input
OUTp, OUTn	14, 12	Data outputs	Output
DCA	17	Eye-cross adjust: Leave open for 50% EC.	Analog
$V_{CC(PIN)}$	3	Optional power supply for photodiode: Internally connected to V_{CC1}	Supply
C1	8	Filter capacitor pad for DCA feedback loop: Requires a 0.47 µF capacitor connected to ground for a 25 kHz cutoff frequency.	Analog
C2	7	Filter capacitor pad for input overload control loop: Requires a 0.1 µF capacitor connected to ground.	Analog
SQ	10	Squelch/output enable: Ground to squelch (output = 0). Open or connect to +3.3 V (LVTTL/CMOS compatible) for normal operation.	Input
RSSI	9	Receive signal strength indicator (RSSI) output: May be left open when not used.	Analog
V_{CC1}	20	Connect to +3.3 V	Supply
V_{CC2}	18, 19	Connect to +3.3 V	Supply
GND	1, 5, 6, 13, 15, 16	Ground. Ground wire-bond connections to the 1340TL are not required. Ground connection to the circuit is made with through wafer vias at pads 2 and 11 in the chip footprint shown above, and between pads 5 and 6, 15 and 16.	Supply
DNU	2,11	Do not use. Connected to the back of the die with through-wafer vias. Back of the die must be connected to electrical ground using conductive epoxy.	Do Not Use

Order Information

Part No.	Description
1340TL-S05D	12.5 Gbps TIA/LIA with RSSI (12 kΩ Differential Gain) – Die

For each customer application, customer's technical experts must validate all parameters. Inphi Corporation reserves the right to change product specifications contained herein without prior notice. No liability is assumed as a result of the use or application of this product. No circuit patent licenses are implied. Contact Inphi Corporation's marketing department for the latest information regarding this product.

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Qualification Notification

The 1340TL-S05 is considered qualified by similarity to the 1340TL-S04. It differs from the 1340TL-S04 only in that the 1340TL-S05 has through-wafer vias whereas the 1340TL-S04 does not. Because the 1340TL-S04 and other Inphi TIA products with through-wafer vias are fully qualified, the 1340TL-S05 is considered qualified.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Changes to the 1340TL-S05 relative to the 1340TL-S04

Through-Wafer-Vias have been added to the 1340TL-S05 under bond-pads 2 and 11, between pads 5 and 6, and between pads 15 and 16. Wirebonds may no longer be made to pads 2, 5, 6, 11, 15 and 16. Attempting to wire bond to these pads will damage the through-wafer vias and compromise the integrity of the circuit's ground connections.

Version Updates

From Version 2.2 to 2.3 (dated 11/04/05)

1. Added Through-Wafer-Vias to the Features section (pg 1).
2. Added a paragraph on Through-Wafer-Vias and reworded some of the Description section (pg 1).
3. Added Through-Wafer-Vias information to the Die-Pad Layout diagram and table (pg 10).
4. Changed product revision from –S04 to –S05 in the Order Information section (pg 11).
1. Added the statement "*Inphi Corporation reserves the right to change product specifications contained herein without prior notice.*" to the Order Information section (pg 11).
2. Qualification Notification section (pg 11) was changed to indicate that the 1340TL-S05 is considered qualified by similarity to the 1340TL-S04 and other Inphi TIA products with through-wafer vias.

Version Updates (cont'd.)

From Version 2.3 to 2.4 (dated 2007-12-13)

1. Added "Preliminary" watermark.
2. Updated Features section by changing Input overload current from 4 mA min to 4 mApp. (page 1)
3. Updated Operating Conditions (page 2):
    a. Changed Power Supply Current max specification from 60 mA to 65 mA.
    b. Changed On-Chip Power Dissipation max specification from 210 mW to 225 mW.
4. Updated Electrical Specifications (page 3-4):
    a. Changed Power Supply Current max specification from 60 mA to 65 mA.
    b. Changed On-Chip Power Dissipation max specification from 210 mW to 225mW.
    c. Updated Small Signal Transimpedance parameter:
        i. Changed min specification from 10 KΩ to 8 KΩ
        ii. Added max specification = 16 KΩ
    d. Changed Differential Output Amplitude (Limited) parameter's max specification from 500 mVpp to 550 mVpp.
    e. Changed Differential Output Amplitude (Squelched) parameter's max specification from 250 mV to 275 mV.
    f. Updated Small Signal Z_T BW parameter:
        i. Added max specification 12.5 GHz
    g. Changed Output Return Loss condition from <12 GHz to < 10 GHz
    h. Removed min specifications for both conditions of the RSSI Gain parameter
5. Removed 1340TL-S05EVB part # and description from Order Information table (page 11).

From Version 2.4 to 2.5 (dated 2009-01-06)

1. Removed "Preliminary" watermark in the datasheet
2. Updated Electrical Specifications (page 3)
    a. Changed "Differential Output Amplitude (Squelched)" to "Differential Output Voltage (Squelched)" and changed its symbol from "$V_{OUTp} – V_{OUTn}$" to "$V_{OUTn} – V_{OUTp}$".
    b. Changed Added Deterministic Jitter Conditions from "peak-to-peak total jitter" to "200 uA < I_{IN} < 3 mApp".
    c. Updated Random Jitter parameter
        i. Deleted Conditions "@ > 500 uA input current" and spec. of max 0.5 ps RMS.
        ii. Removed Conditions "@ 100 µA input current"
    d. Changed Output Return Loss Conditions from "< 10 GHz" to "< 8.5 GHz".