UHF ASK/FSK Transmitter

Description

The T5750 is a PLL transmitter IC which has been developed for the demands of RF low-cost transmission systems at data rates up to 32 kBaud. The transmitting frequency range is 868 MHz to 928 MHz.
It can be used in both FSK and ASK systems.

Features

- Integrated PLL loop filter
- ESD protection (4 kV HBM/ 200V MM) [1)]
- High output power (5.5 dBm) with low supply current (8.5 mA)
- Modulation scheme ASK/ FSK [2)]
- Easy to design in
- Single Li-cell for power supply
- Supply voltage 2.0 V to 4.0 V in the temperature range of –40°C to 85°C
- Package SO8
- Single-ended antenna output
- CLK output for clocking the µC
- One-chip solution with minimum external circuitry

System Block Diagram

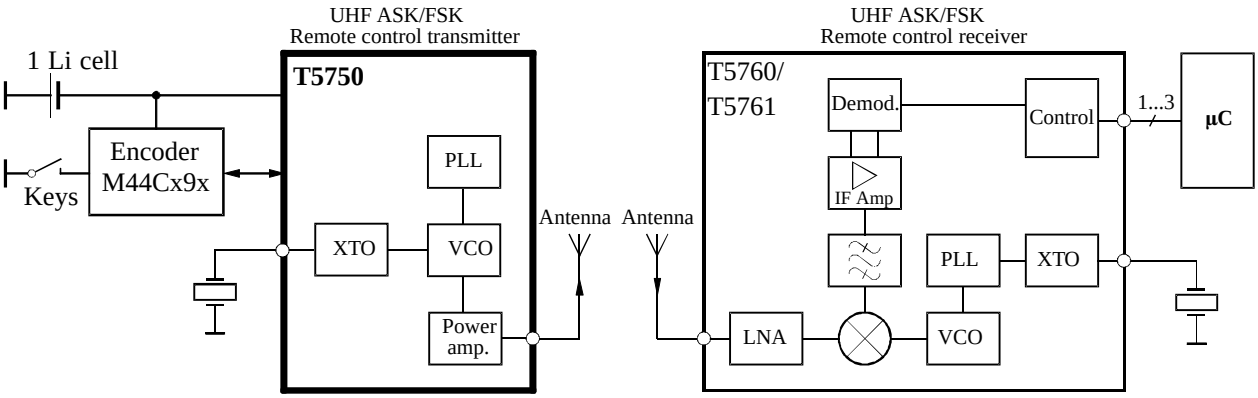


Figure 1. System block diagram

Ordering Information

Extended Type Number	Package	Remarks
T5750–TAS	SO8	Tube
T5750–TAQ	SO8	Taped and reeled

1) Except Pin 2 (4 kV HBM / 100 V MM).
2) FSK modulation is achieved by connecting an additional capacitor between the XTAL load capacitor and the open drain output of the modulating µC.

Preliminary Information

Pin Description

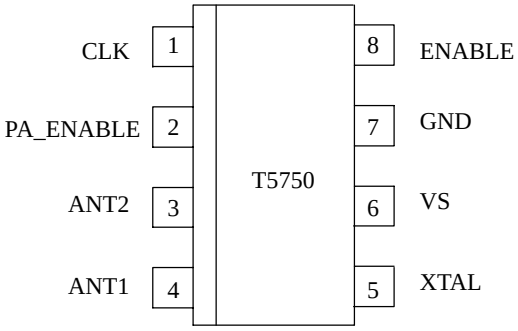
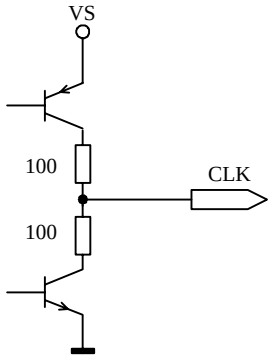
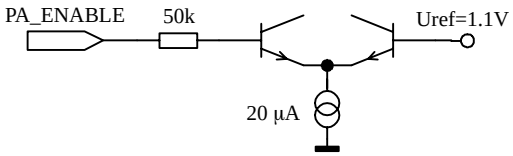
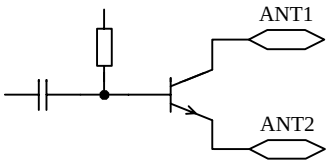
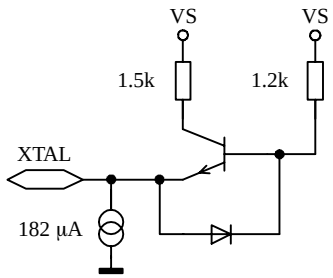
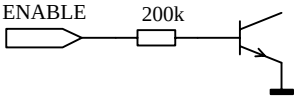


Figure 2. Pinning SO8

Pin	Symbol	Function	Configuration
1	CLK	Clock output signal for µC The clock output frequency is set by the crystal to f_{XTAL} / 4	
2	PA_ ENABLE	Switches on power amplifier, used for ASK modulation	
3	ANT2	Emitter of antenna output stage	
4	ANT1	Open collector antenna output	
5	XTAL	Connection for crystal	
6	VS	Supply voltage	See ESD protection circuitry (figure 8)
7	GND	Ground	See ESD protection circuitry (figure 8)
8	ENABLE	Enable input	

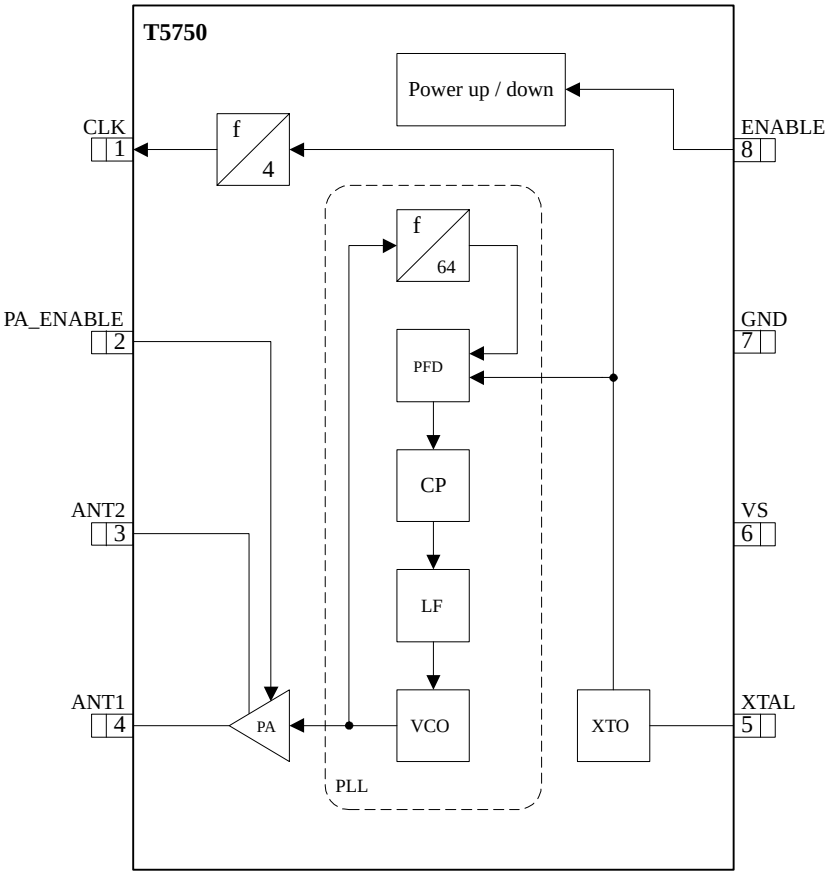


Figure 3. Block diagram

General Description

This fully integrated PLL transmitter allows particularly simple, low cost RF miniature transmitters to be assembled. The VCO is locked to $64 \times f_{XTAL}$ hence a 13.5672 MHz crystal is needed for a 868.3 MHz transmitter and a 14.2969 MHz crystal for a 915 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL needs typ.<1ms until the PLL is locked and the CLK output is stable. A wait time of ≥ 4 ms must be used until the CLK is used for the uC and the PA is switched on.

The power amplifier is an open collector output delivering a current pulse which is nearly independent to the load impedance. The delivered output power is hence controllable via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to 50 Ω. A high power efficiency of $\eta = P_{out}/(I_{S,PA} \times V_S)$ of 24% for the power amplifier @ 868.3 MHz results when an optimised load impedance of Z_{Load}= (166 + j226) Ω is used at 3 V supply voltage.

Functional Description

If ENABLE = L and the PA_ENABLE=L the circuit is in standby mode consuming only a very small amount of current, so that a lithium cell used as power supply can work for several years.

With ENABLE=H the XTO, PLL and the CLK driver are switched on. If PA_ENABLE stay L only the PLL and the XTO is running and the CLK signal is delivered to the µC. The VCO locks to 64 times the XTO frequency.

With ENABLE=H and PA_ENABLE=H the PLL, XTO, CLK driver and the power amplifier are on. With PA_ENABLE the power amplifier can be switched on an off, which is used to perform the ASK modulation.

ASK Transmission

The T5750 is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 4 ms, then the CLK signal is taken to clock the µC and output power can be modulated by

means of Pin PA_ENABLE. After transmission PA_ENABLE is switched to L and the µC switches back to internal clocking. The T5750 is switched back to standby mode with ENABLE=L.

FSK Transmission

The T5750 is activated by ENABLE = H. PA_ENABLE must remain L for t ≥ 4 ms, then the CLK signal is taken to clock the µC and the power amplifier is switched on with PA_ENABLE=H. The chip is then ready to FSK modulation. The µC starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. If the switch is closed, the output frequency is lower than if the switch is open. After transmission PA_ENABLE is switched to L and the µC switches back to internal clocking. The T5750 is switched back to standby mode with ENABLE=L.

The accuracy of the frequency deviation with XTAL pulling method is about ± 25% when the following tolerances are considered.

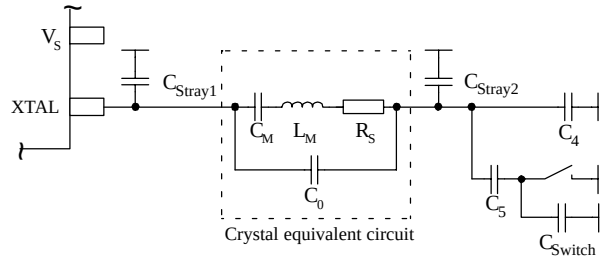


Figure 4. Tolerances of frequency modulation

Using C_4 = 9.2 pF ± 2%, C_5 = 3.9 pF ± 5%, a switch port with CS_{witch} = 3 pF ± 10%, stray capacitances on each side of the crystal of $C_{Stray1} = C_{Stray2}$ = 1 pF ± 10%, a parallel capacitance of the crystal of C_0 = 3.2 pF ± 10% and a crystal with C_M = 13 fF ± 10% an FSK deviation of ± 21.5 kHz typical with worst case tolerances of ± 16.8 kHz to ± 28.0 kHz results.

CLK Output

An output CLK signal is provided for a connected µC, the delivered signal is CMOS compatible if the load capacitance is lower than 10 pF.

Take-over of the Clock Pulse

The clock of the crystal oscillator can be used for clocking the µC. The M4xCx9x has the special feature of starting with an integrated RC-oscillator to switch on the T5750 with ENABLE = H, and after 4 ms to assume the clock signal of the transmission IC, so that the message can be sent with crystal accuracy.

Output Matching and Power Setting

Output power is set by load impedance of the antenna. The maximum output power is archieved with a load impedance of $Z_{Load,opt}$ = (166 + j226) Ω @868.3 MHz. There must be a low resistive path to V_S to deliver the DC current.

The delivered curent pulse of the power amplifier is 7.7 mA and the maximum output power is delivered to a resistive load of 475 Ω if the 0.53 pF output capacitance of the power amplifier is compensated by the load impedance. An optimum load impedance of $Z_{Load} = 475\ \Omega \parallel j/(2 \times \pi \times f \times 0.53\ pF) = (166 + j226)\ \Omega$ thus results for the maximum output power of 5.5 dBm.

The load impedance is defined as the impedance seen from the T5750's ANT1, ANT2 into the matching network. Do not confuse this large signal load impedance with a small signal input impedance delivered as input characteristic of RF amplifiers and measured from the application into the IC instead of from the IC into the application for an power amplifier.

Less output power is achieved by lowering the real parallel part of 475 Ω where the parallel imaginary part should be kept constant.

Output power measurement can be done with the circuit of figure 5, note that the component values must be changed to compensate the individual board parasitics until the T5750 see the right load impedance $Z_{Load,opt}$ = (166 + j226) Ω @868.3 MHz. Also the damping of the cable used to measure the output power must be calibrated out.

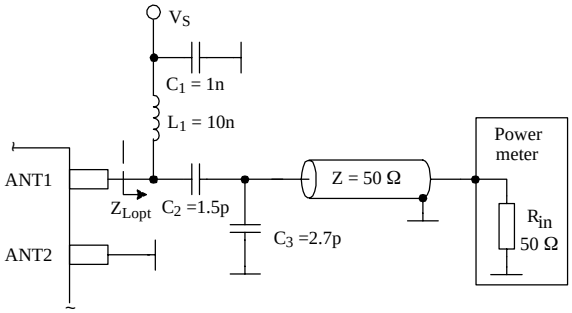


Figure 5. Output power measurement

Application Circuit

For the supply-voltage blocking capacitor C_3 a value of 68 nF/ X7R is recommended. C_1 and C_2 are used to match the loop antenna to the power amplifier where C_1 typically is 3.9 pF/ NP0 and C_2 is 1 pF/ NP0 (for C_2 two capacitors in series should be used to achieve a better tolerance value and to have the possibility to realize the $Z_{Load,opt}$ by using standard valued capacitors).

C_1 forms together with the Pins of T5750 and the PCB board wires a series resonance loop that suppresses the 1st

harmonic, hence the position of C_1 on the PCB is important. Normally the best supression is achieved when C_1 is placed as close as possible to the Pins ANT1 and ANT2. The loop antenna should not exceed a width of 1.5 mm, otherwise the Q-factor of the loop antenna is too high.

L_1 ($\approx$50 nH to 100 nH) can be printed on PCB. C_4 should be selected that the XTO runs on the load resonance frequency of the crystal. Normally for a 15 pF load-capacitance crystal a value of 12 pF results.

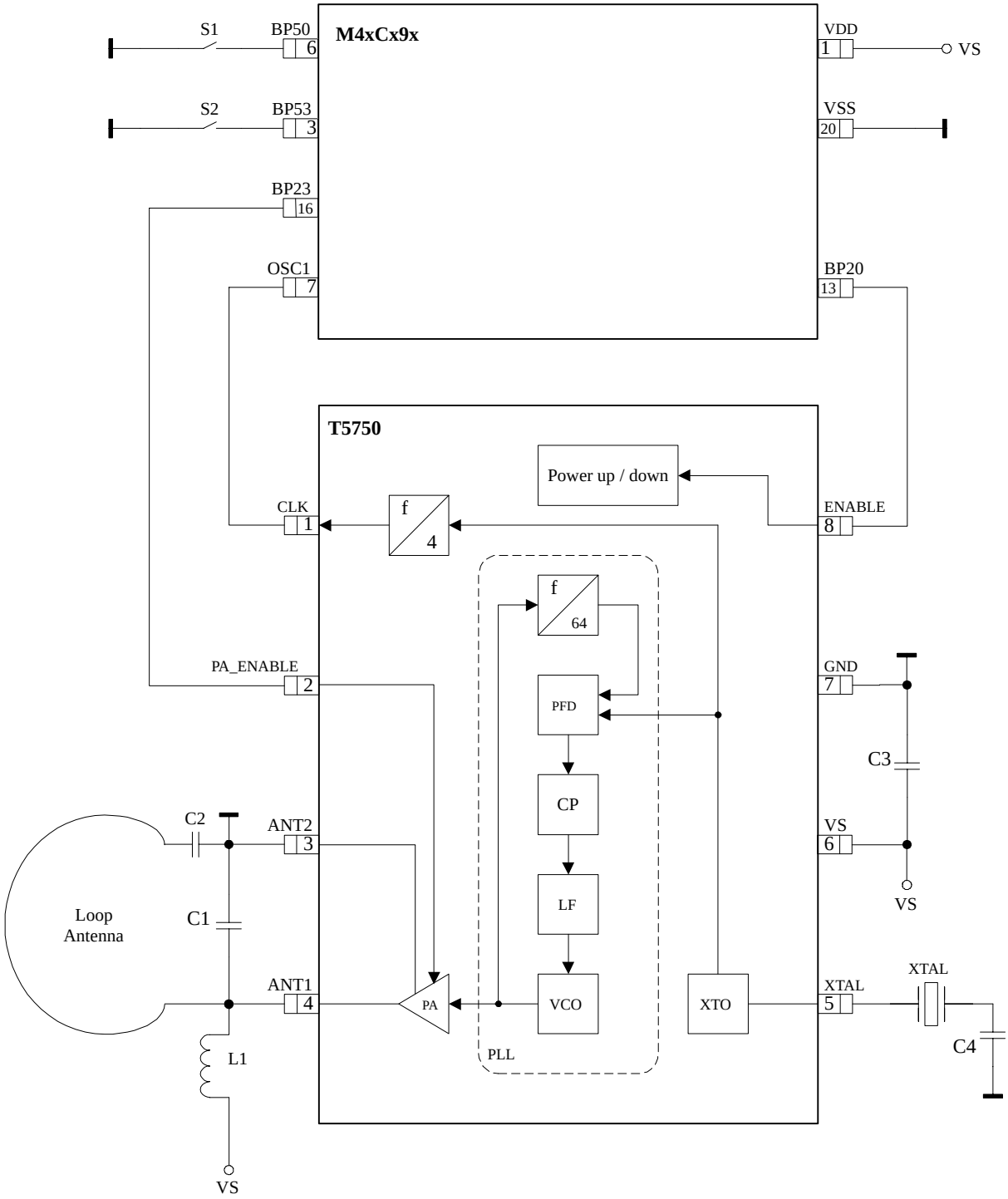


Figure 6. ASK application circuit

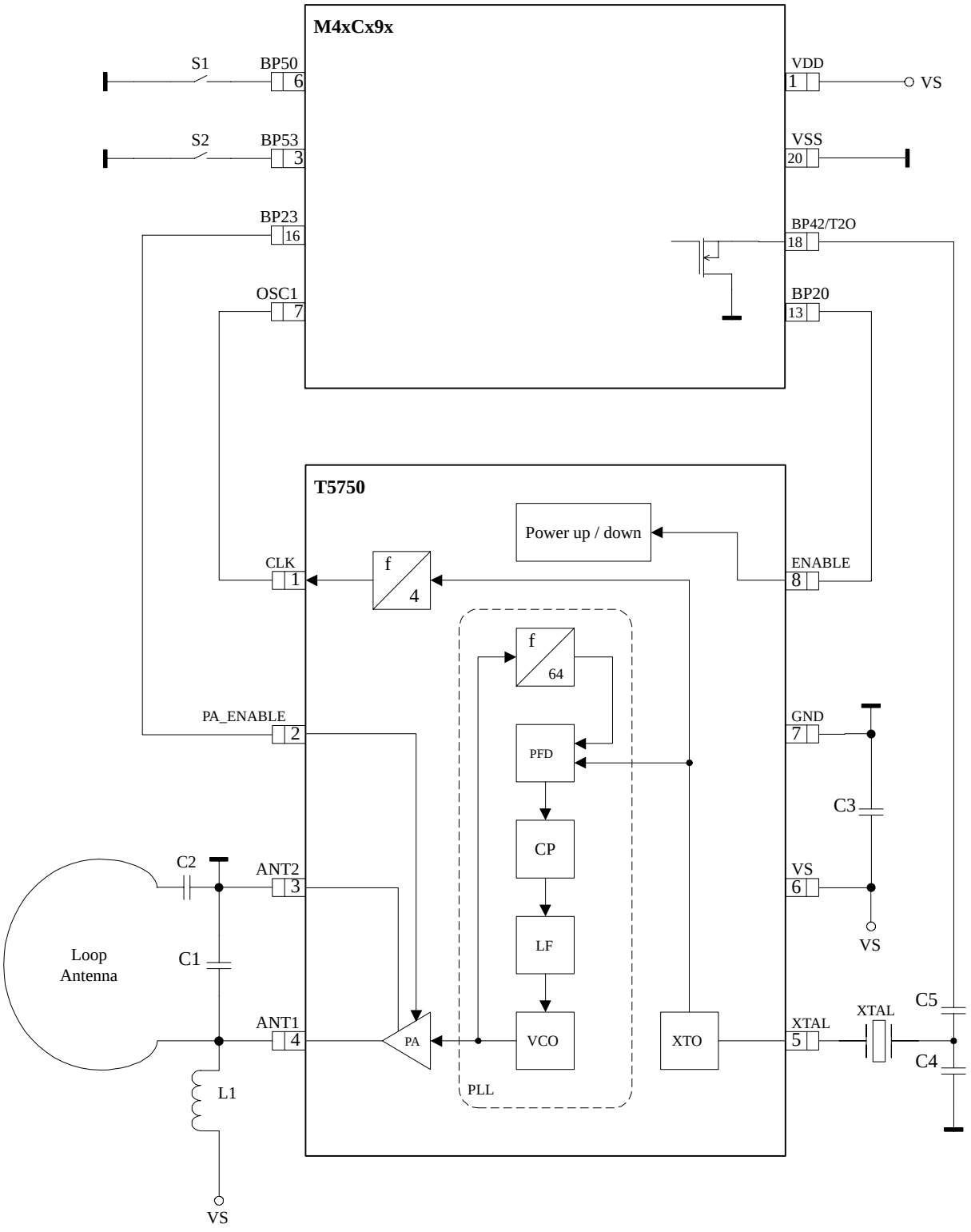


Figure 7. FSK application circuit

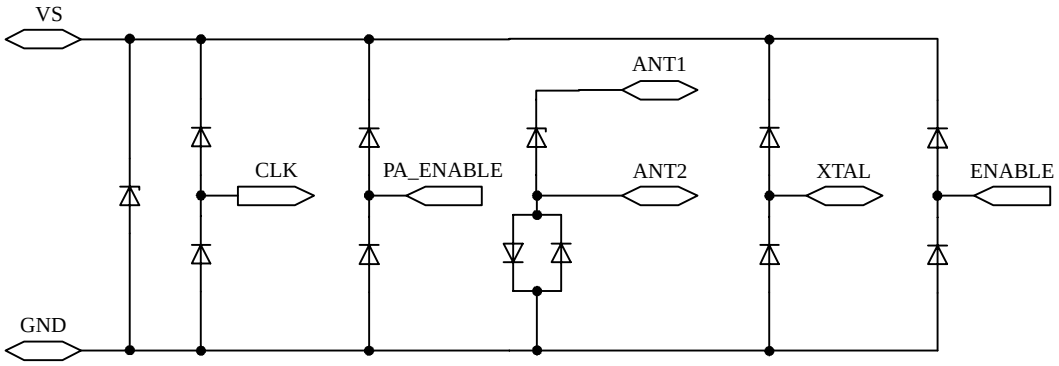


Figure 8. ESD protection circuit

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	V_S		5	V
Power dissipation	P_{tot}		100	mW
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	–55	125	°C
Ambient temperature	T_{amb}	–55	105	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal resistance junction ambient	RthJA	160	K/W

Electrical Characteristics

V_S = 2.0 V to 4.0 V, T_{amb} = –40°C to 85°C unless otherwise specified. Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are refered to GND (Pin 7)

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply current	Power down, V_{ENABLE} < 0.3 V, VPA_{ENABLE} < 0.3 V	I_{S_Off}			350	nA
Supply current	Power up, PA off, V_S = 3 V, V_{ENABLE} > 1.7 V, VPA_{ENABLE} < 0.3 V	I_S		3.6	4.6	mA
Supply current	Power up, V_S = 3.0 V, V_{ENABLE} > 1.7 V, VPA_{ENABLE} >1.7 V	$I_{S\_Transmit}$		8.5	11	mA
Output power	V_S = 3.0 V, T_{amb} = 25°C, f = 868.3 MHz, Z_{Load} = (166 + j226) Ω	P_{Ref}	3.5	5.5	8.0	dBm
Output power variation for the full temperature range	T_{amb} = –40°C to +85°C, V_S = 3.0 V V_S = 2.0 V $P_{Out} = P_{Ref} + \Delta P_{Ref}$	ΔP_{Ref} ΔP_{Ref}			–1.5 –4.0	dB dB
Achievable output-power range	Selectable by load impedance	P_{Out_typ}	–3.0		5.5	dBm

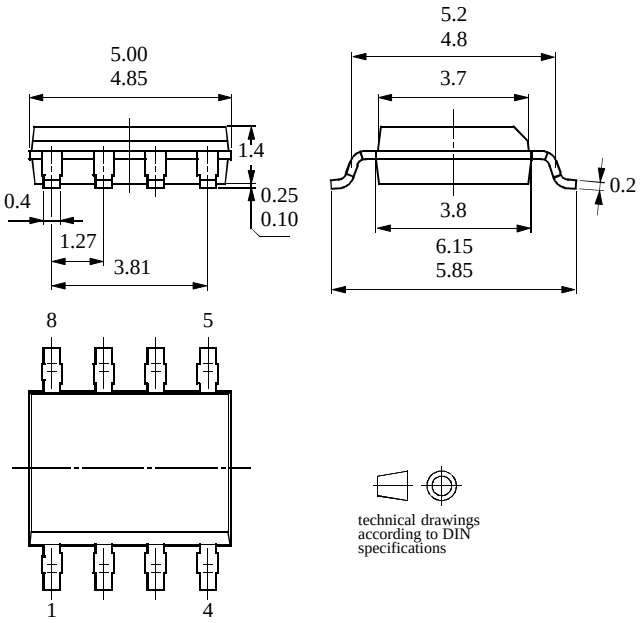
Electrical Characteristics (continued)

V_S = 2.0 V to 4.0 V, T_{amb} = –40°C to 85°C unless otherwise specified. Typical values are given at V_S = 3.0 V and T_{amb} = 25°C. All parameters are refered to GND (Pin 7)

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Spurious emission	$f_{CLK} = f_0/256$ Load capacitance at Pin CLK = 10 pF $f_O \pm 1 \times f_{CLK}$ $f_O \pm 4 \times f_{CLK}$ other spurious are lower			 –52 –52		 dBc dBc
Oscillator frequency XTO (=phase comparator frequency)	$f_{XTO} = f_0/64$ f_{XTAL} = resonant frequency of the XTAL, C_M = 10 fF, load capacitance selected accordingly	f_{XTO}	–30ppm	f_{XTAL}	+30ppm	
PLL loop bandwidth				250		kHz
Phase noise of phase comparator	Refered to $f_{PC} = f_{XT0,}$ 10 kHz distance to carrier			–116	–110	dBc/Hz
In loop phase noise PLL	10 kHz distance to carrier			–80	–74	dBc/Hz
Phase noise VCO	@ 1 MHz @ 36 MHz			–89 –120	–86 –117	dBc/Hz dBc/Hz
Frequency range of VCO		f_{VCO}	868		928	MHz
Clock output frequency (CMOS µC compatible)				$f_0/256$		MHz
Voltage swing at Pin CLK	$C_{Load} \leq 10$ pF	V_{0h} V_{0l}	$V_S \times 0.8$		 $V_S \times 0.2$	V V
Series resonance R of the crystal		Rs			80	Ω
Capaictive load @ Pin XT0					7	pF
FSK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ASK modulation frequency rate	Duty cycle of the modulation signal = 50%		0		32	kHz
ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	 1.7		0.3 20	V V µA
PA_ENABLE input	Low level input voltage High level input voltage Input current high	V_{Il} V_{Ih} I_{In}	 1.7		0.3 5	V V µA

Package Information

Package SO8
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Data sheets can also be retrieved from the Internet: http://www.atmel–wm.com

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