

KMCJ5322000

2M x 32 / 4M x 16 Fast Page Mode

GENERAL DESCRIPTION

The KMCJ5322000 is the industry standard high capacity DRAM memory card and consists of SAMSUNG's advanced TSOP 1Mx4 DRAM devices.

The SAMSUNG memory card family is designed to protect the internal circuitry from electrostatic discharge by using metal plates on the top and bottom side of the card. And the memory card supports the JEIDA standard to provide system upgradability and exchangeability.

The memory card allows the user to switch x32/x16 for the ease of system interface. The memory card is designed to suit for memory capacity expansion and applications which handles large data.

FEATURES

- Performance range :

	1RAC	1CAC	1RC
KMCJ5322000 - 6	60 ns	15 ns	110 ns
KMCJ5322000 - 7	70 ns	20 ns	130 ns
KMCJ5322000 - 8	80 ns	20 ns	150 ns
- Organization : 2Mx32 / 4Mx16
- Power Supply : 5V±5%
- Fast Page Mode Operation
- TTL compatible inputs and outputs
- All inputs buffered except RAS inputs
- Extended refresh : 1024 cycles/128 ms
 - RAS only and Hidden refresh
 - CAS before RAS refresh
- Supported Industry Standard (JEIDA / JEDEC)
 - Connector type : 88 pin two piece (Two Row)
 - Card Dimensions : 85.6 x 54.0 x 3.3 (mm)



PIN CONFIGURATION

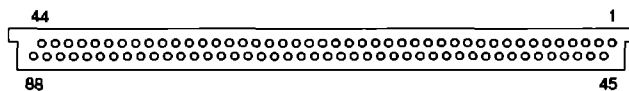
1	Vss	16	A4	31	NC	46	DQ16	61	A9	76	PD8
2	DQ0	17	NC	32	NC	47	DQ17	62	NC	77	NC
3	DQ1	18	A6	33	NC	48	DQ18	63	Vss	78	NC
4	DQ2	19	A8	34	DQ8	49	DQ19	64	NC	79	NC
5	DQ3	20	NC	35	NC	50	DQ20	65	RAS1	80	DQ24
6	DQ4	21	NC	36	DQ9	51	DQ21	66	CAS2	81	DQ25
7	DQ5	22	RAS0	37	Vcc	52	DQ22	67	Vss	82	DQ26
8	DQ6	23	CAS0	38	DQ10	53	DQ23	68	CAS3	83	DQ37
9	Vcc	24	CAS1	39	DQ11	54	NC	69	RAS2	84	DQ28
10	DQ7	25	NC	40	DQ12	55	NC	70	WE	85	DQ29
11	NC	26	RAS2	41	DQ13	56	Vss	71	PD1	86	DQ30
12	NC	27	Vcc	42	DQ14	57	A1	72	PD3	87	DQ31
13	A0	28	PD2	43	DQ15	58	A3	73	Vss	88	Vss
14	A2	29	PD4	44	Vss	59	A5	74	PD5		
15	Vcc	30	PD6	45	Vss	60	A7	75	PD7		

PIN DESCRIPTION

A0 - A9	Address Inputs
DQ0 - DQ31	Data Input / Outputs
RAS0 - RAS3	Row Address Strobe
CAS0 - CAS3	Column Address Strobe
WE	Read / Write Input
Vcc	Power (4-5V)
Vss	Ground
NC	No Connection

	60 ns	70 ns	80 ns
PD1	GND	GND	GND
PD2	NC	NC	NC
PD3	GND	GND	GND
PD4	GND	GND	GND
PD5	GND	GND	GND
PD6	NC	GND	NC
PD7	NC	NC	GND
PD8	NC	NC	NC

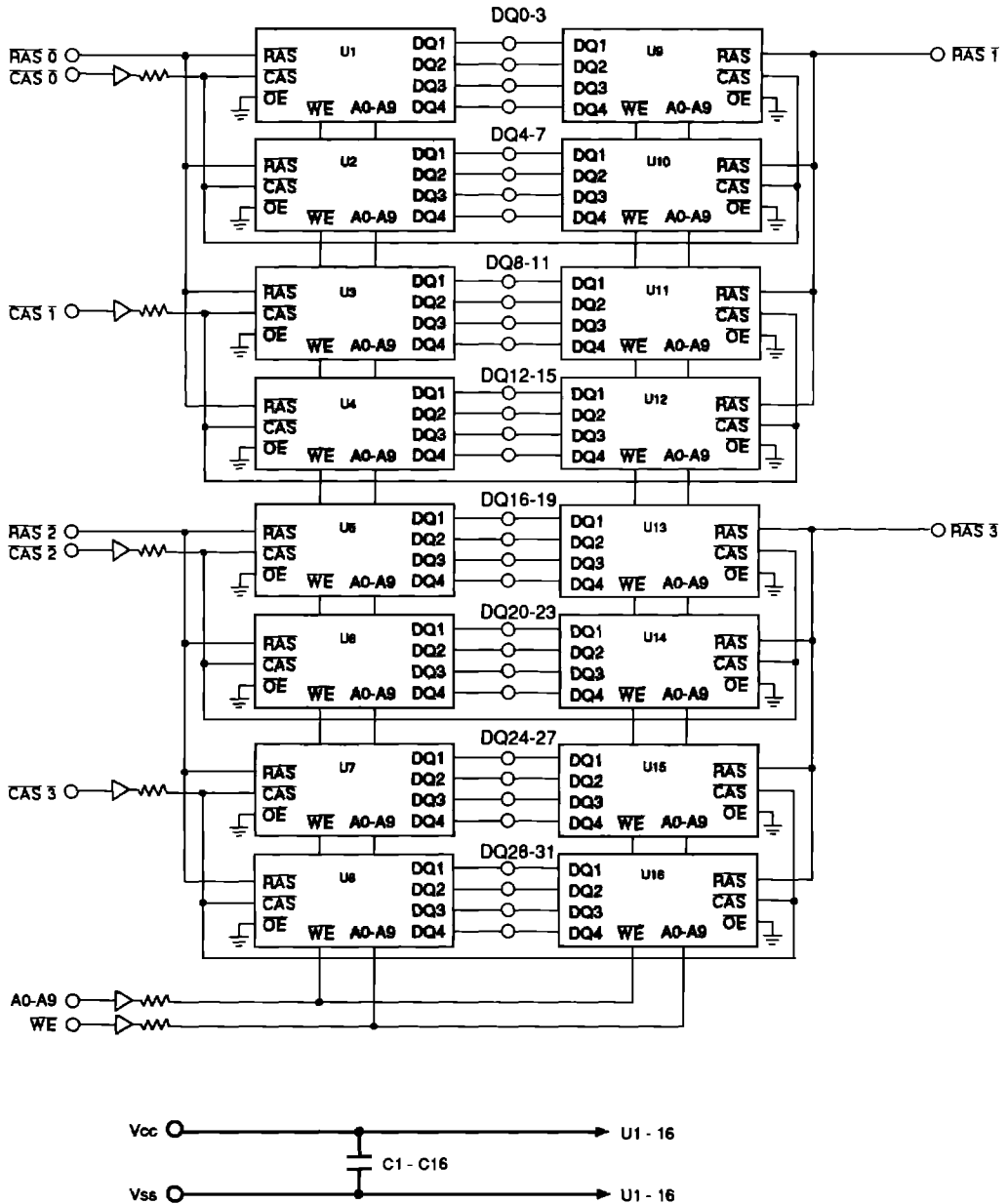
PIN CONNECTOR



DRAM CARD

8 Mega Byte

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Units
Input Voltage on any pin relative to Vss : \overline{RAS} pin	V _{IN1}	-1.0 to +7.0	V
Input Voltage on any pin relative to Vss : except \overline{RAS} pin	V _{IN2}	-0.5 to V _{CC} +0.5	V
Output Voltage on any pin relative to Vss	V _{OUT}	-1.0 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to +7.0	V
Storage Temperature	T _{stg}	-20 to +70	°C
Power Dissipation	P _D	9.6	W
Short Circuit Output Current	I _{OS}	50	mA

*Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T = 0 to 70 °C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.75	5.0	5.25	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1	V
Input Low Voltage	V _{IL}	-1.0	-	0.8	V
Operating Temperature	T _A	0	-	55	°C

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Part No	Symbol	Min	Max	Units
OPERATING CURRENT* (RAS, CAS, Address cycling @tRC=min.)	KMCJ5322000 - 6 KMCJ5322000 - 7 KMCJ5322000 - 8	Icc1	-	736 656 576	mA mA mA
STANDBY CURRENT (RAS=CAS=V _{IH})		Icc2	-	32	mA
RAS-ONLY REFRESH CURRENT* (CAS= V _{IH} , RAS cycling@tRC =min.)	KMCJ5322000 - 6 KMCJ5322000 - 7 KMCJ5322000 - 8	Icc3	-	736 656 576	mA mA mA
FAST PAGE MODE CURRENT* (RAS=V _{IL} , CAS cycling: tPC= min.)	KMCJ5322000 - 6 KMCJ5322000 - 7 KMCJ5322000 - 8	Icc4	-	576 496 416	mA mA mA
STAND BY CURRENT (RAS=CAS=V _{CC} -0.2V)		Icc5	-	3.2	mA
CAS-BEFORE-RAS REFRESH CURRENT* (RAS and CAS cycling @tRC=min.)	KMCJ5322000 - 6 KMCJ5322000 - 7 KMCJ5322000 - 8	Icc6	-	736 656 576	mA mA mA
BATTERY BACK UP CURRENT - only Low Power ver. (CAS=CAS before RAS cycling or 0.2V, WE,/A0-A9=V _{CC} -0.2V or 0.2V, DIN=V _{CC} -0.2V or open, tRC=125us, tRAS=min. ~ 1us)		Icc7	-	4.8	mA
INPUT LEAKAGE CURRENT (Any Input 0 ≤ V _{IN} ≤ 6.5V, all other pins not under test = 0 volts.)	RAS pin	I _{IL}	-40	40	μA
	else RAS pin		-1	1	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V _{OUT} ≤ 5.5V)		I _{OL}	-20	20	μA
OUTPUT HIGH VOLTAGE LEVEL(I _{OH} = -5mA)		V _{OH}	2.4	-	V
OUTPUT LOW VOLTAGE LEVEL(I _{OL} = 4.2mA)		V _{OL}	-	0.4	V

* NOTE : Icc1, Icc3, Icc4 and Icc5 are dependent on output loading and cycle rates. Specified values are obtained with the output open. Icc is specified as an average current.

CAPACITANCE (T = 25 °C)

Item	Symbol	Min	Max	Unit
Input capacitance : A0-A9	C _{IN1}	-	15	pF
Input capacitance : WE	C _{IN2}	-	15	pF
Input capacitance : RAS0-RAS3	C _{IN3}	-	50	pF
Input capacitance : CAS0-CAS3	C _{IN4}	-	15	pF
Input/Output capacitance : DQ0-31	C _{DQ1}	-	10	pF

AC CHARACTERISTICS (0°C ≤ Ta ≤ 55°C, Vcc = 5.0V ± 5%. See notes 1,2.)

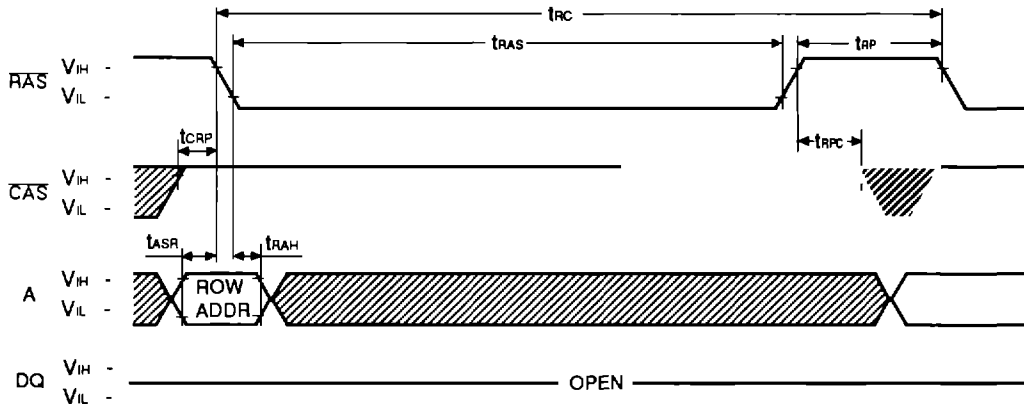
STANDARD OPERATION	Symbol	KMCJ5322000-6		KMCJ5322000-7		KMCJ5322000-8		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	IRC	120		140		160		ns	
Access time from RAS	IRAC		60		70		80	ns	3,4
Access time from CAS	ICAC		22		27		27	ns	3,4,5
Access time from column address	IAA		37		42		47	ns	3,11
CAS to output in Low-Z	tCLZ	0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	22	0	27	0	27	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	ns	2
RAS precharge time	tRP	40		50		60		ns	
RAS pulse width	tRAS	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	tRSH	22		27		27		ns	
CAS hold time	tCSH	60		70		80		ns	
CAS pulse width	tCAS	22	10,000	27	10,000	27	10,000	ns	
RAS to CAS delay time	IRCD	18	38	18	43	20	53	ns	4
RAS to column address delay time	IRAD	13	23	13	28	13	33	ns	11
CAS to RAS precharge time	ICRP	17		17		17		ns	
Row address set-up time	IASR	7		7		7		ns	
Row address hold time	IRAH	8		8		13		ns	
Column address set-up time	IASC	2		2		2		ns	
Column address hold time	ICAH	22		22		22		ns	
Column address hold referenced to RAS	IAR	50		55		60		ns	6
Column Address to RAS lead time	IRAL	37		42		47		ns	
Read command set-up time	IRCS	2		2		2		ns	
Read command hold referenced to CAS	IRCH	2		2		2		ns	9
Read command hold referenced to RAS	IRRH	2		2		2		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold referenced to RAS	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to RAS lead time	IRWL	22		27		27		ns	
Write command to CAS lead time	ICWL	15		20		20		ns	
Data-in set-up time	IDS	2		2		2		ns	10
Data-in hold time	IDH	22		22		22		ns	10
Data-in hold referenced to RAS	IDHR	50		55		60		ns	6
Refresh period	tREF		120		120		120	ns	
Write command set-up time	tWCS	2		2		2		ns	8
CAS setup time (C-B-R refresh)	ICSR	17		17		17		ns	
CAS hold time (C-B-R refresh)	tCHR	17		17		17		ns	
RAS precharge to CAS hold time	IRPC	22		22		22		ns	
Access time from CAS precharge	ICPA		42		47		52	ns	3
Fast Page mode cycle time	IPC	47		52		57		ns	
CAS precharge time (Fast page)	ICP	10		10		10		ns	
RAS pulse width (Fast page)	IRASP	60	100K	70	100K	80	100K	ns	
W to RAS precharge time (C-B-R refresh)	tWRP	10		10		10		ns	
W to RAS hold time (C-B-R refresh)	tWRH	10		10		10		ns	
CAS precharge (C-B-R counter test)	ICPT	20		25		30		ns	

2

NOTES

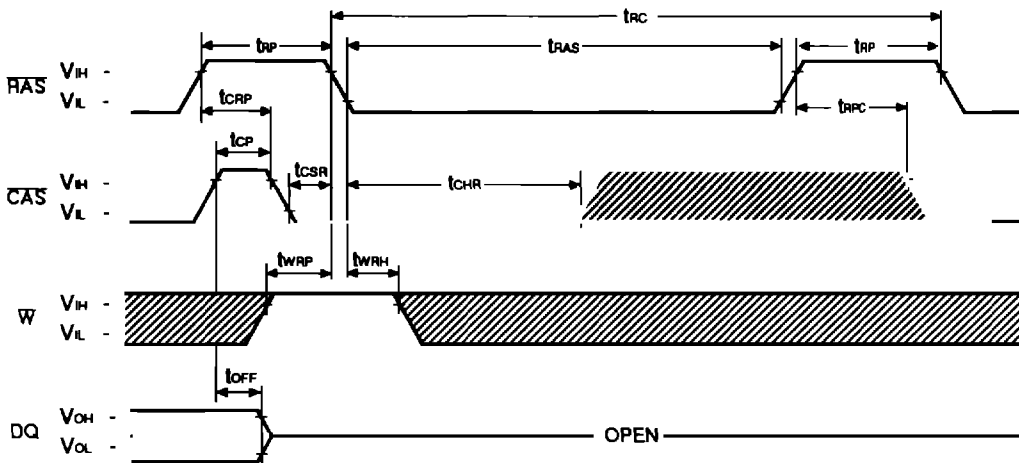
1. An initial pause of $200\mu\text{s}$ is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
2. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF .
4. Operation within the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$.
6. t_{AR} , t_{WCR} , t_{DHR} are referenced to $t_{\text{RAD}}(\text{MAX})$
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
8. t_{WCS} is non restrictive operating parameter. It included in the data sheet as electrical characteristic only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles.
11. Operation within the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled by t_{AA} .

RAS-ONLY REFRESH CYCLE



NOTE : W = Don't care

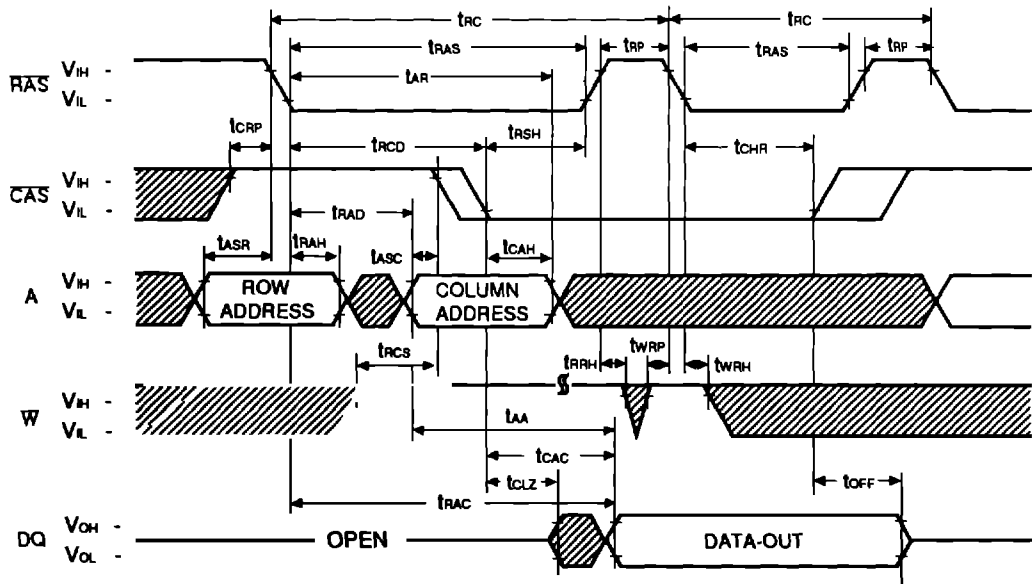
CAS-BEFORE-RAS REFRESH CYCLE



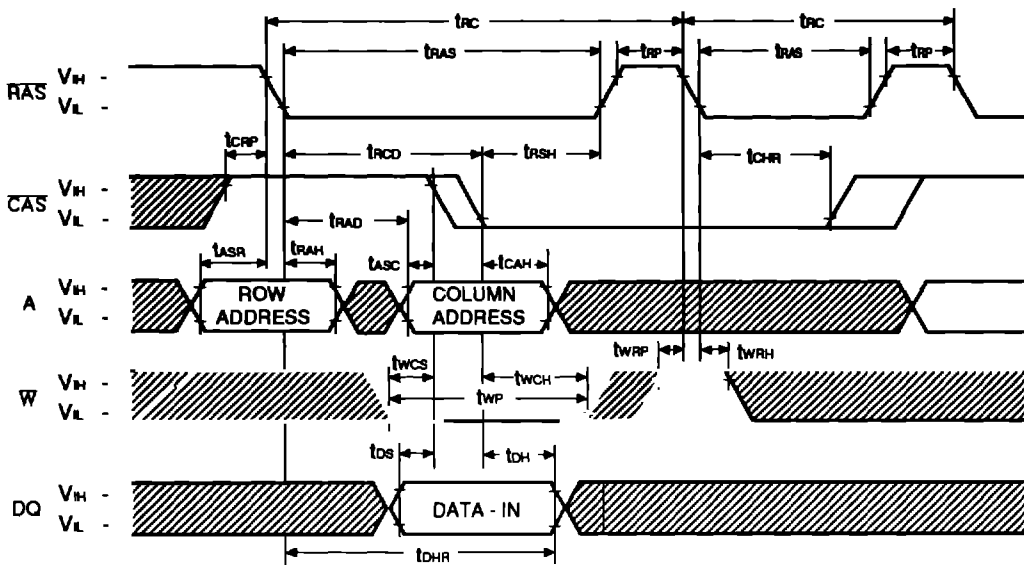
NOTE : A = Don't Care

 Don't Care

HIDDEN REFRESH CYCLE (READ)

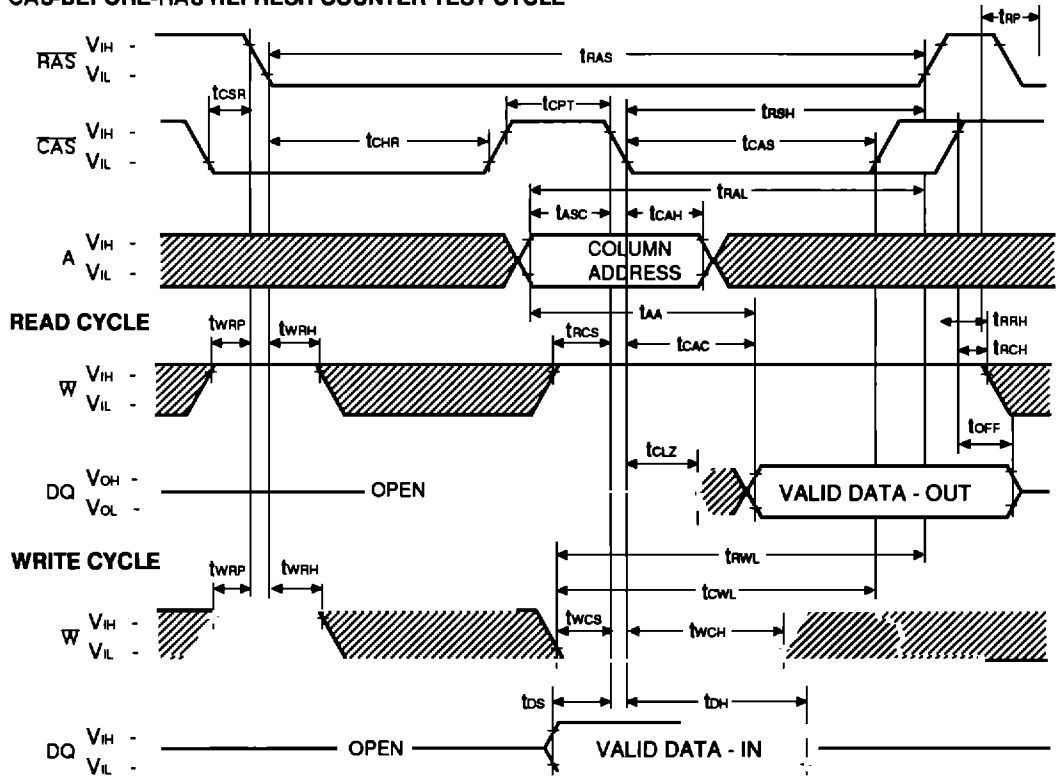


HIDDEN REFRESH CYCLE (WRITE)



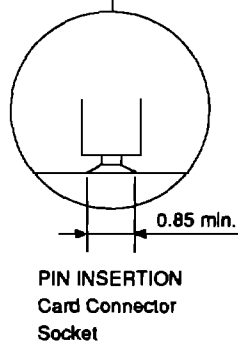
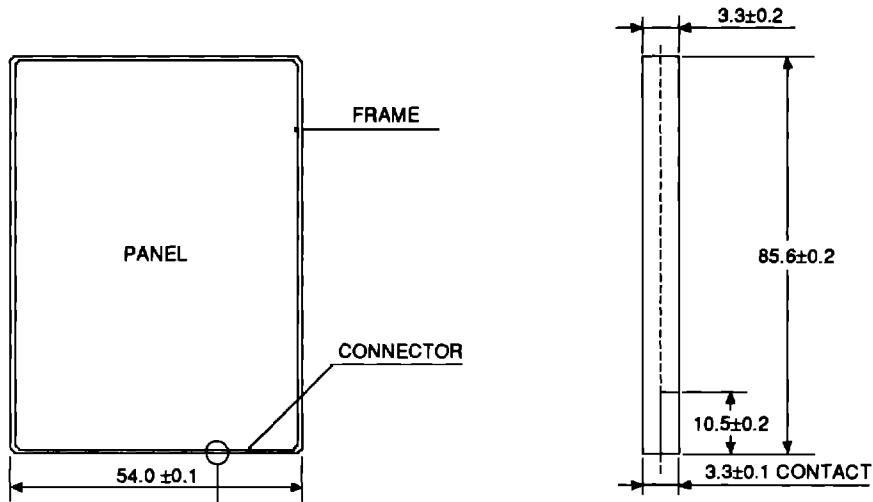
 Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

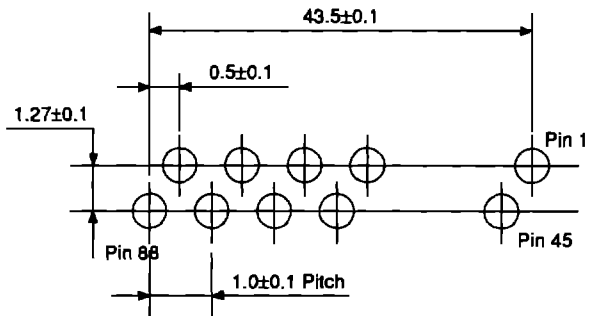


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PACKAGE DIMENSIONS



PIN LAYOUT 2 Row - 88 Pins



CONNECTOR

