

HN62331AP/F

131,072 × 8-Bit CMOS MASK Programmable Read Only Memory

DESCRIPTION

The HN62331A is a 1-Mbit CMOS mask-programmable ROM organized as 131,072-words × 8-bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62331A, which provides large capacity of 1M bits, is ideally suited for kanji character generators.

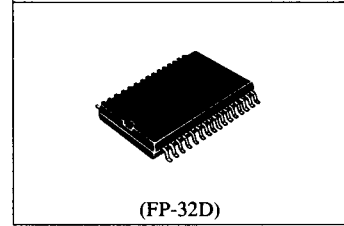
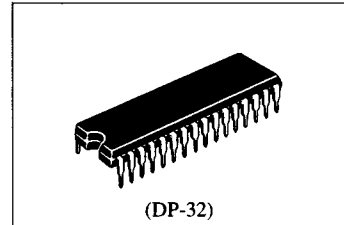
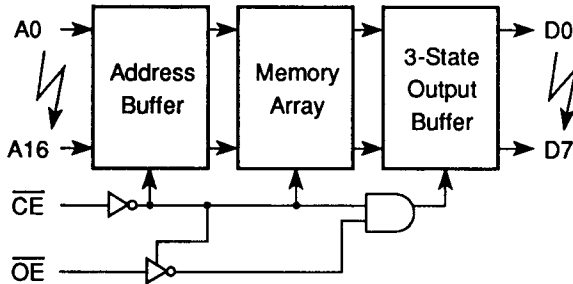
FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time120ns (max.)
- Low Power Consumption100mW (typ.) Active
5μW (typ.) Standby
- Byte-wide Data Organization
- Pin Compatible with JEDEC

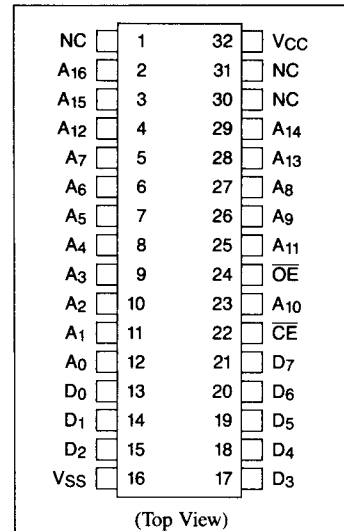
ORDERING INFORMATION

Type No.	Access Time	Package
HN62331AP	120ns	600 mil 32 pin Plastic DIP
HN62331AF	120ns	32 pin Plastic SOP

BLOCK DIAGRAM



PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	-0.3 ~ +7.0	V	1
All Input and Output Voltage	V_T	-3.0 ~ $V_{CC} + 0.3$	V	1
Operating Temperature Range	T_{opr}	0 ~ +70	°C	
Storage Temperature Range	T_{stg}	-55 ~ +125	°C	
Temperature Under Bias	T_{bias}	-20 ~ +85	°C	

NOTE: 1. With respect to V_{SS} .

■ RECOMMENDED OPERATING CONDITIONS ($V_{SS} = 0V$, $T_a = 0 \sim 70^\circ C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.4	—	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	—	0.45	V

■ DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0 \sim 70^\circ C$)

Item	Symbol	Test Condition	Min.	Max.	Unit	
Supply Current	Active	I_{CC}	$V_{CC} = 5.5V$, $ID_{OUT} = 0mA$, $t_{RC} = \text{Min.}$	—	50	mA
	Standby	I_{SB}	$V_{CC} = 5.5V$, $\overline{CE} \geq V_{CC} - 0.2V$	—	30	μA
Input Leakage Current	$ I_{IL} $	$V_{IN} = 0 \sim V_{CC}$	—	10	μA	
Output Leakage Current	$ I_{OL} $	$\overline{CE} = 2.4V$, $V_{OUT} = 0 \sim V_{CC}$	—	10	μA	
Output Voltage	V_{OH}	$I_{OH} = -205\mu A$	2.4	—	V	
	V_{OL}	$I_{OL} = 1.6mA$	—	0.4	V	

■ **CAPACITANCE** ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 25^\circ C$, $V_{IN} = 0V$, $f = 1MHz$)

Item	Symbol	Min.	Max.	Unit
Input Capacitance	C_{IN}	—	10	pF
Output Capacitance	C_{OUT}	—	15	pF

NOTE: * This parameter is sampled and not 100% tested.

■ **AC ELECTRICAL CHARACTERISTICS** ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0 \sim 70^\circ C$)

Item	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{RC}	120	—	ns
Address Access Time	t_{AA}	—	120	ns
\overline{CE} Access Time	t_{ACE}	—	120	ns
\overline{OE} Access Time	t_{OE}	—	60	ns
Output Hold Time From Address Change	t_{DHA}	0	—	ns
Output Hold Time From \overline{CE}	t_{DHC}	0	—	ns
Output Hold Time From \overline{OE}	t_{DHO}	0	—	ns
\overline{CE} to Output in High Z	t_{CHZ}^*	—	60	ns
\overline{OE} to Output in High Z	t_{OHZ}^*	—	60	ns
\overline{CE} to Output in Low Z	t_{CLZ}	5	—	ns
\overline{OE} to Output in Low Z	t_{OLZ}	5	—	ns

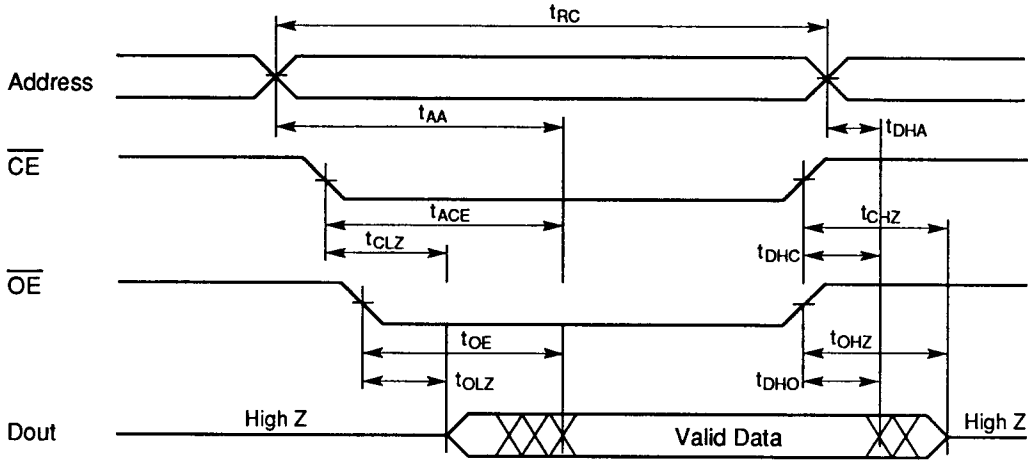
NOTE: * t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

• **Test Conditions**

- Input Pulse Level: 0.45 ~ 2.4V
- Input and Output Timing Reference Level: 1.5V

- Input Rise and Fall Time: 10ns
- Output Load: 1 TTL gate + CL = 100pF
(including scope and jig capacitance)

■ **TIMING WAVEFORM**



NOTES:

1. t_{DHA} , t_{DHC} , t_{DHO} ; determined by faster.
2. t_{AA} , t_{ACE} , t_{OE} ; determined by slower.
3. t_{CLZ} , t_{OLZ} ; determined by slower.