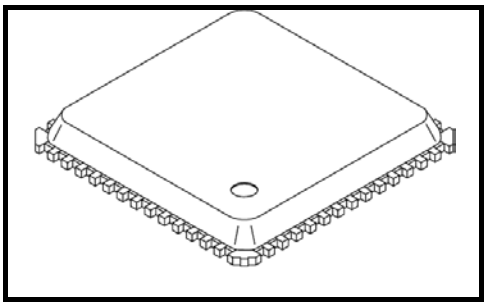
Toshiba bipolar type linear integrated circuit Bi-CMOS silicon Monolithic

TB9042FTG

DCDC converter &LDO series power supply



P-HVQFN52-0808-0.50-001

1. Outline

The TB9042FTG is a system power supply for the vehicle applications. It is a multi-output power supply incorporating two DCDC convertors and three series power supplies. High efficient drive is realized by DCDC power supply and reduced noise is also realized by series power supply.

Abundant monitoring functions for detecting abnormal power supply and MCU are incorporated. It is possible to transmit a monitoring state to an external system by SPI communication.

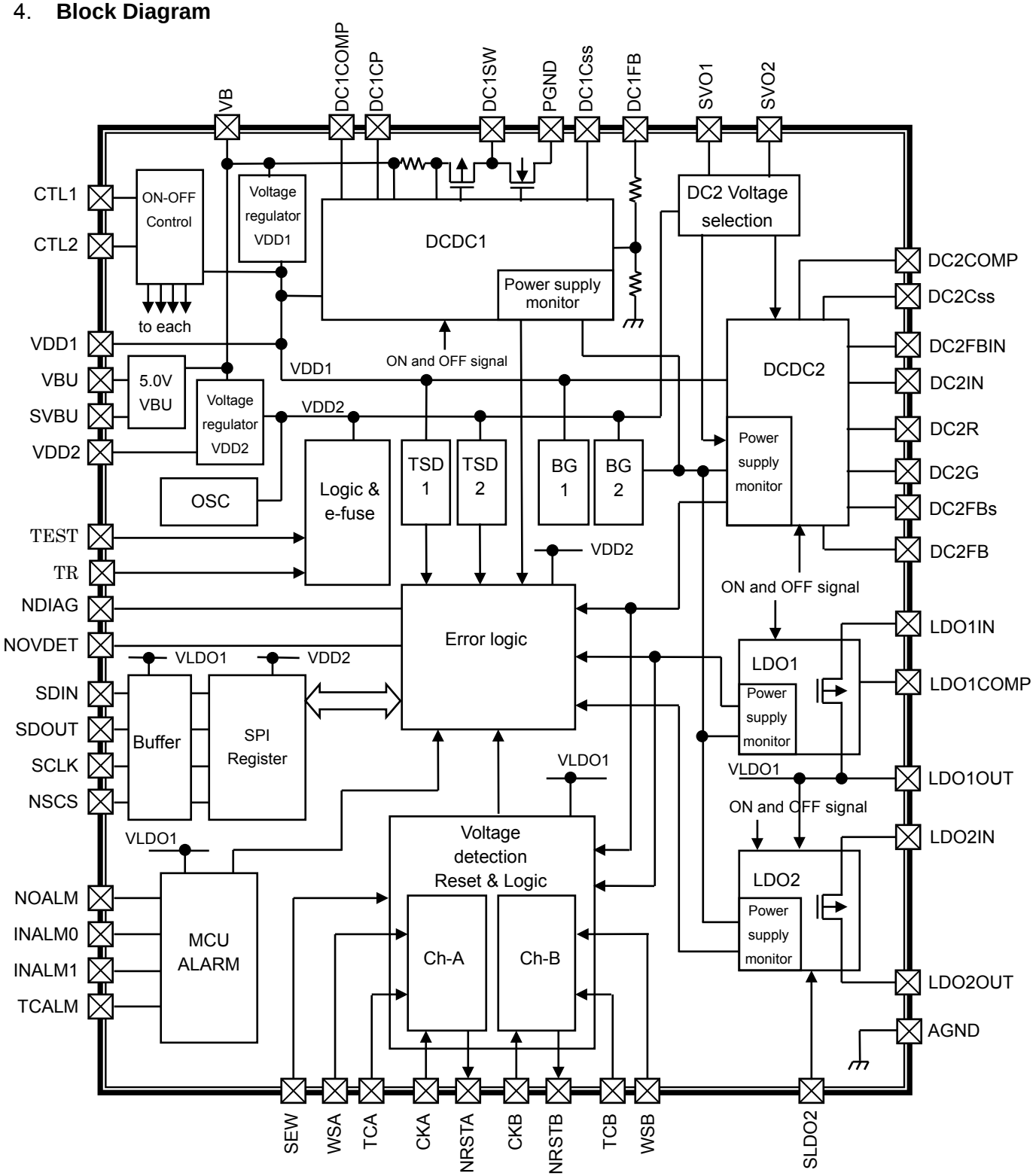
2. Application

Engine control / brakes control /EPS control systems

3. Features

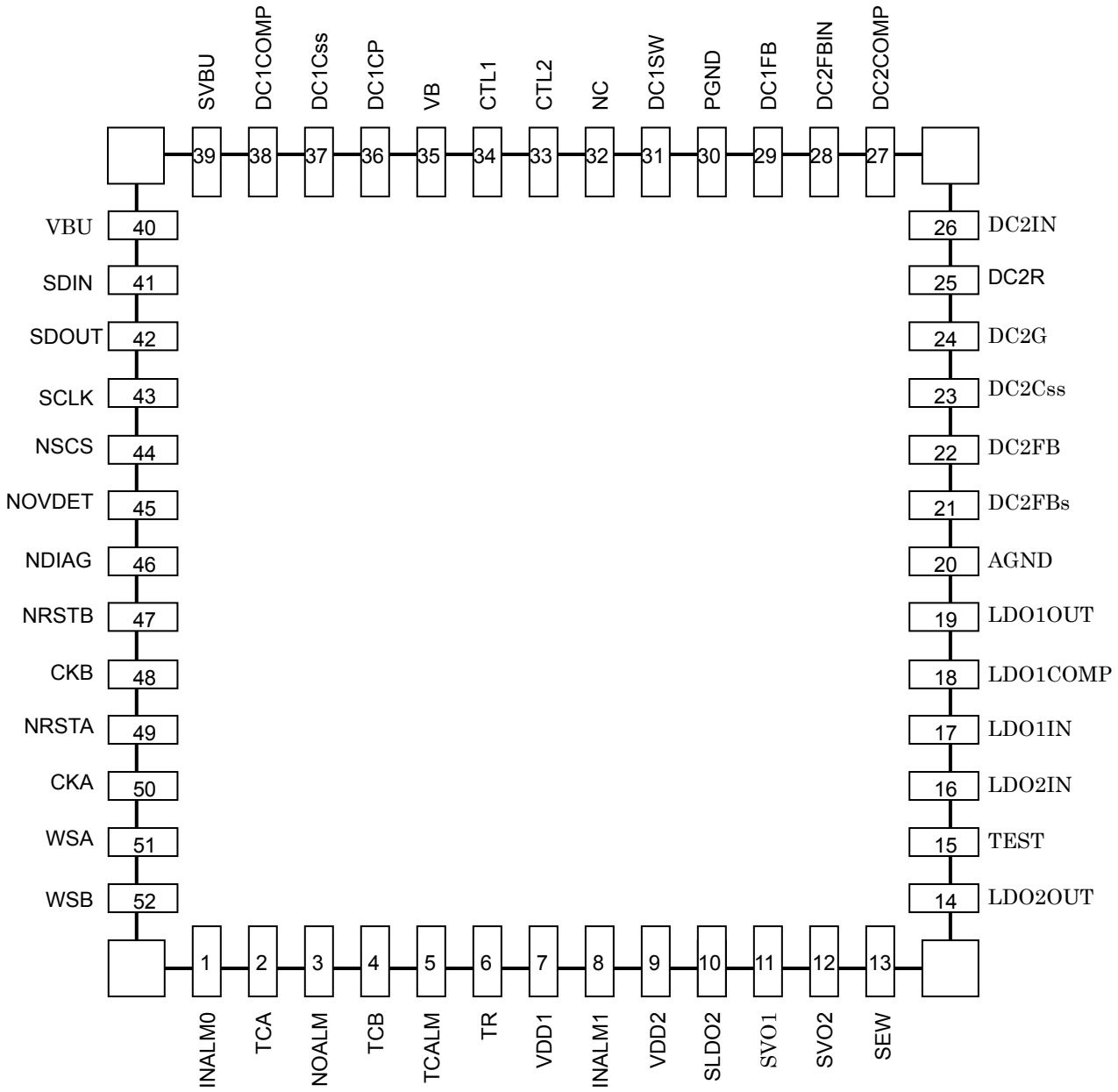
- DCDC converters (two circuits)
  - DCDC1: Synchronous rectification step-down converter with built-in output MOS Tr.: 6V output.
  - DCDC2: Step-down converter to drive external MOS Tr.: 1.2V / 1.5V output selectable.
- Series power supplies with a built-in output MOS Tr.(three circuits)
  - LDO1: Output voltage 5.0V
  - LDO2: Output voltage 5.0V (Independent mode or tracking mode is selectable.)
  - VBU: Backup power supply 5.0V / 3.3V (selection by terminal setup)
- Monitoring output voltage & Outputting reset
  - Monitoring high-voltage and low-voltage
  - Power-on reset
  - Watchdog timer (clock input and reset output: two independent systems)
  - MCU alarm signal monitor
- Built-in SPI communication
  - The notice signal output of each abnormality of a power supply function. MCU diagnosis
- Operational temperature range: -40 to 125 °C
- Small leadless and power flat package: P-HVQFN52-0808-0.50-001

4. Block Diagram



Notes: Since a function is explained, it may have omitted in part and may have simplified the functional block / circuit / constant in a block diagram.

5. **Pin description**



6. Terminal Function

6.1. Terminal Function explanation

Terminal numbers	Sign	Explanation of a terminal
1	INALM0	The input terminal of a MCU alarm signal
2	TCA	The timer time setting capacitor terminal of reset timer Ch-A
3	NOALM	The terminal which outputs the filter judged result of MCU alarm
4	TCB	The timer time setting capacitor terminal of reset timer Ch-B
5	TCALM	The judgment filter time setting capacitor terminal of MCU alarm
6	TR	Test terminal. It is an open setup at the time of user use.
7	VDD1	The output terminal of power supply VDD1 for internal circuits
8	INALM1	The input terminal of a MCU alarm signal
9	VDD2	The output terminal of power supply VDD2 for internal circuits
10	SLDO2	The output voltage control selection terminal of series power supply LDO2 It is H and is 5V constant voltage outputting operation. It becomes 1 time amplifier control of LDO1 output by L, and outputs LDO1 voltage.
11	SVO1	The output voltage setting terminal of DCDC2 A setup of the output voltage of DCDC2 is possible by the combination of H of SVO1 and SVO2, and L. 1.2V, 1.5V. Please refer to 6.2 Terminal setting truth table for the details. The detection voltage of the high-voltage and low-voltage is also interlocked with this setup.
12	SVO2	
13	SEW	The ON/OFF selection terminal of the clock high-speed abnormality detecting of a watchdog timer. SEW ="H" : High-speed detection disable. SEW ="L" : High-speed detection enable. Please fix this selection at the time of application circuit determination, and do not perform the change under IC operation.
14	LDO2OUT	The output terminal of series power supply LDO2
15	TEST	Test mode setting terminal
16	LDO2IN	The input terminal of series power supply LDO2
17	LDO1IN	The input terminal of series power supply LDO1
18	LDO1COMP	It is a phase compensation terminal of series power supply LDO1. A capacitor and resistance are connected to series between output terminals.
19	LDO1OUT	It is an output terminal of series power supply LDO1.
20	AGND	GND terminal
21	DC2FBs	The sense terminal for surveillance of the feedback loop of DCDC2. It is used, short-circuit with DC2FB.
22	DC2FB	It is output voltage feedback detection terminals of DCDC2.
23	DC2Css	It is a time setting terminal of the soft start of DCDC2. If capacitor 0.1micro F is connected between GND, the soft start time for 5 ms will be generated.
24	DC2G	It is a gate drive terminal of external MOS of the switching output of DCDC2.
25	DC2R	It is a sense terminal of the resistance for current detection of DCDC2. Resistance is connected with DC2IN between DC2R.
26	DC2IN	It is an input terminal of DCDC2.
27	DC2COMP	It is a terminal for phase compensation of DCDC2. A capacitor and resistance are connected to series between DC2FBIN terminals.
28	DC2FBIN	It is a switching regulator error AMP inversion input terminal. Please connect 220pF between DC2FB and DC2FBIN.
29	DC1FB	It is output voltage feedback detection terminals of DCDC1.
30	PGND	It is a GND terminal of DCDC1.

Terminal numbers	Sign	Explanation of a terminal
31	DC1SW	It is a switching output terminal of DCDC1.
32	NC	A non-connecting terminal
33	CTL2	The terminal which controls DCDC1, DCDC2, LDO1, LDO2 and VBU operation. The combination of set-up ON/OFF is decided by combination of H and L of CTL1 and CTL2. Please refer to 6.2 Terminal setting truth table for the details.
34	CTL1	
35	VB	It is a supply voltage input terminal.
36	DC1CP	It is a reference voltage terminal of a switching output drive circuit. Please connect 0.1 micro F with VB between DC1CP.
37	DC1Css	It is a time setting terminal of the soft start of DCDC1. If capacitor 0.1uF is connected between GND, the soft start time for 5 ms will be generated.
38	DC1COMP	It is a terminal for phase compensation of DCDC1. A capacitor and resistance are connected to series to opposite GND.
39	SVBU	The selection terminal of 5V and 3.3V of VBU voltage. VBU=5V at SVBU=H,VBU=3.3V at SVBU=L.
40	VBU	The backup voltage output for RAM retention. The voltage change of 5V and 3.3V is possible with a SVBU terminal.
41	SDIN	The serial-data input terminal of SPI
42	SDOUT	The serial-data output terminal of SPI. It is a tri state buffer output.
43	SCLK	The clock input terminal of SPI
44	NSCS	The chip-select terminal of SPI
45	NOVDET	The output terminal for detection signals at the time of the output high voltage of DCDC2 and LDO1. The notice of a self-diagnostics judged result is also outputted from this terminal. N-ch open drain output. With no pull-up resistor.
46	NDIAG	The terminal which writes error information, such as abnormalities of each power supply output, a reset timer, and MCU surveillance, in a register, and outputs the flag signal of error information generating.
47	NRSTB	The reset signal output terminal of Ch-B
48	CKB	The watch dog clock input terminal of Ch-B
49	NRSTA	The reset signal output terminal of Ch-A
50	CKA	The watch dog clock input terminal of Ch-A
51	WSA	Ch-A watch dog function ON/OFF change terminal
52	WSB	Ch-B watch dog function ON/OFF change terminal

6.2. Terminal setting truth table

CTL1, CTL2 terminal: Power supply output ON/OFF change. Setting voltage of the input H: V_B

CTL1	CTL2	DCDC1	DCDC2	LDO1	LDO2	VBU	MODE
L	L	OFF	OFF	OFF	OFF	OFF	Stop
L	H	OFF	OFF	OFF	OFF	ON	Standby
H	L	ON	ON	ON	ON	ON	Active
H	H	ON	ON	ON	ON	ON	Active

SVO1, SVO2 terminal: DCDC2 output voltage. Setting voltage of the input H: V_{DD2}

SVO1	SVO2	DCDC2 output voltage (Typ.)
L	H	1.2V
H	L	1.5V
H	H	ALL 5 power-supply output OFF
L	L	

SLDO2 terminal: LDO Operation mode
Setting voltage of the input H: V_{DD2}

SLDO2	Operation mode of LDO1 and LDO2
L	Tracking
H	Independent

SVBU terminal: VBU output voltage
Setting voltage of the input H: V_{BU}

SVBU	VBU output voltage
L	3.3V
H	5V

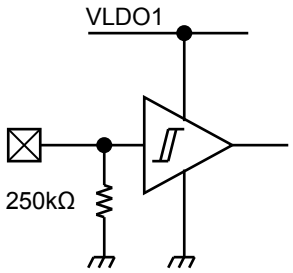
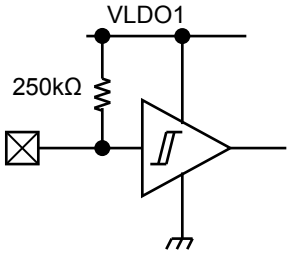
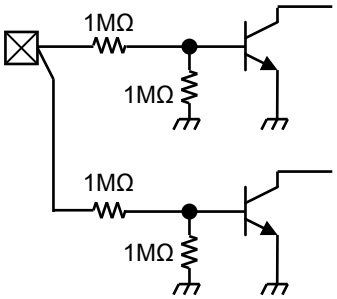
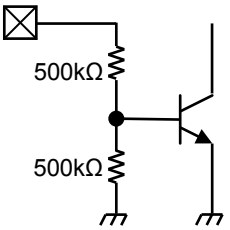
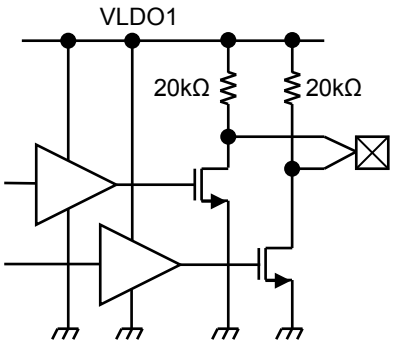
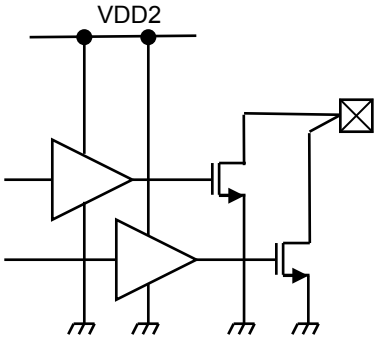
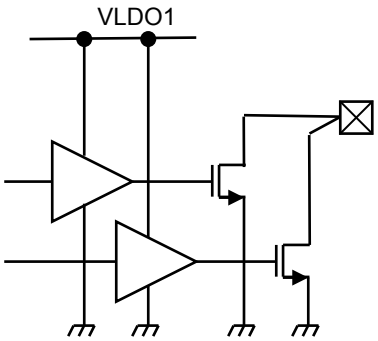
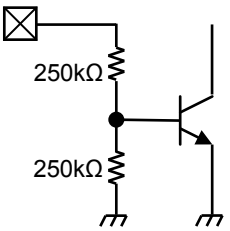
WSA, WSB terminal: WDT ON/OFF change
Setting voltage of the input H: V_{LDO1}

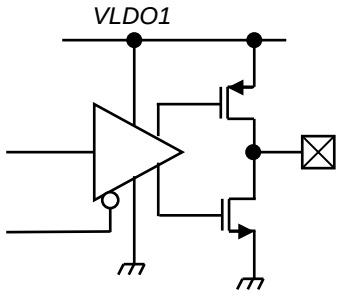
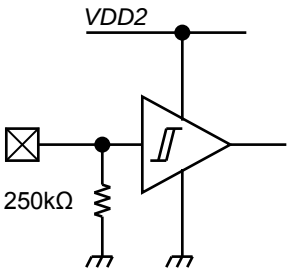
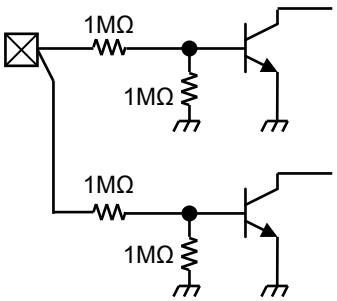
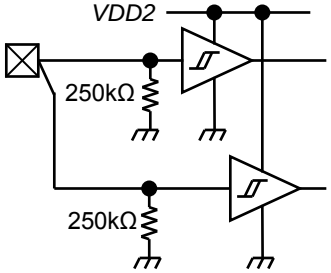
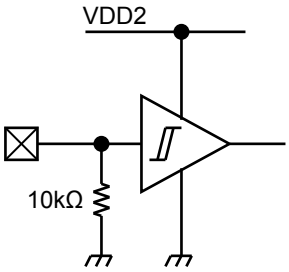
WSA, WSB	Reset timer function
L	WDT&POR
H	Only POR

SEW terminal: WDT window change
Setting voltage of the input H: V_{DD2}

SEW	Window
L	a window (high-speed detection -- effective)
H	Only low-speed detection (high-speed detection invalidity)

7. **Signal input-output-terminals equivalent circuit**

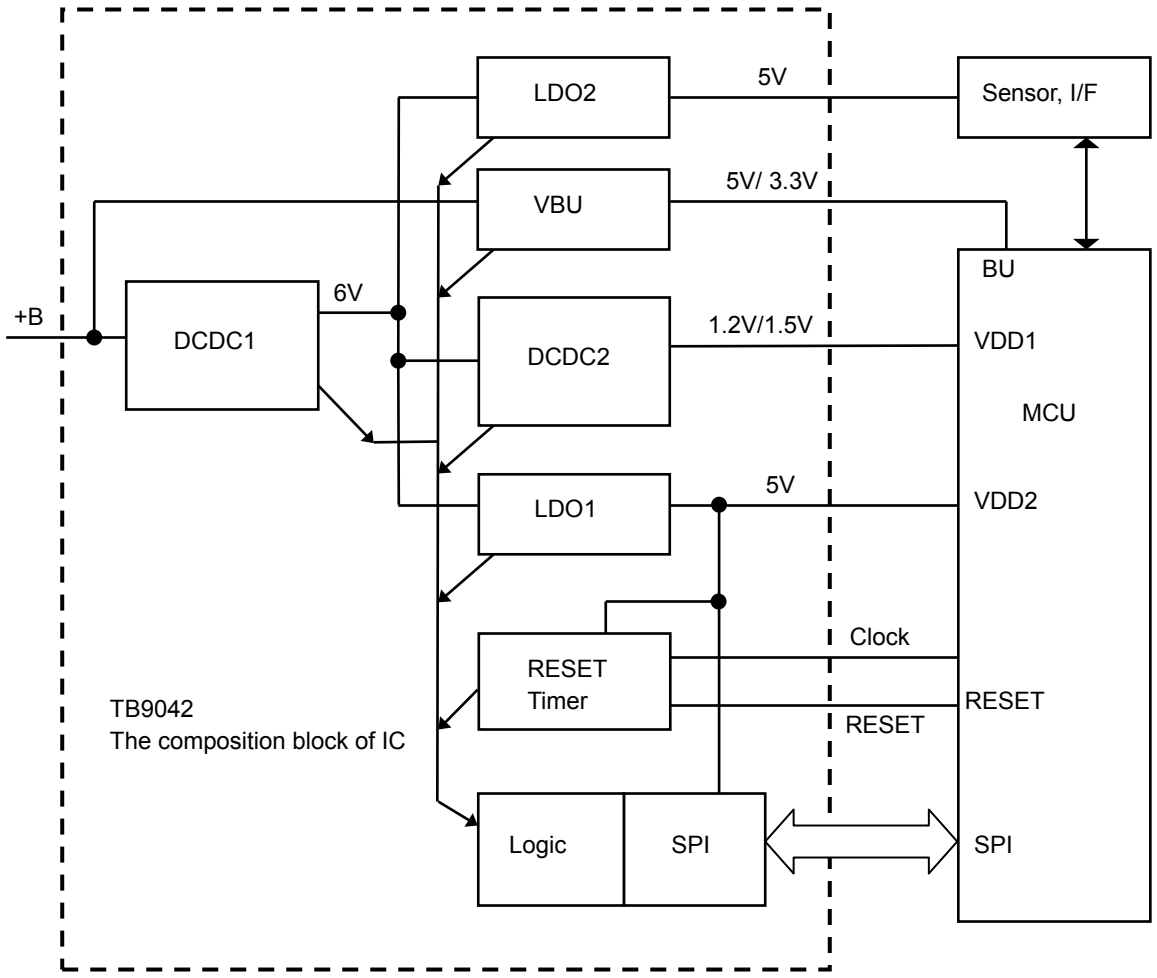
Terminal	Input/output circuit diagram	Terminal	Input/output circuit diagram
CKA, CKB, WSA, WSB, SDIN, SCLK, INALM0		NSCS, INALM1	
CTL1		CTL2	
NRSTA, NRSTB, NDIAG		NOVDET	
NOALM		SEW	

Terminal	Input/output circuit diagram	Terminal	Input/output circuit diagram
SDOUT		SLDO2	
SVBU		SVO1, SVO2	
TEST			

8. Functional explanation

8.1. Whole operation

- The voltage of 6V is generated by DCDC converter (DCDC1) from vehicle +B power supply. And this voltage of 6V generates the voltage for core of microcomputer by DCDC2 and the voltage of 5V of microcomputer by LDO1. DCDC2 is a regulator of selection-type constant voltage, and it can set up 1.2V/1.5V on terminal conditions.
- 5V-constant voltage output (LDO2) is incorporated for the sensor and other interfaces which is independent of a microcomputer-power supply.
- Backup power supply output is provided for retaining RAM data. In the standby mode, only this VBU becomes active and low dark current flows.
- By SPI communication, status of each power supply is informed to MCU and MCU diagnosis are possible.
- Two watchdog timers are built in as a MCU monitor.
- ON and OFF function of each power supply (DCDC1, DCDC2, LDO1, LDO2, and VBU) can be controlled by setting CTL1 and CTL2. Truth table is shown below.



CTL1, CTL2 terminal: Power supply output ON/OFF change. Setting voltage of the input H: VB

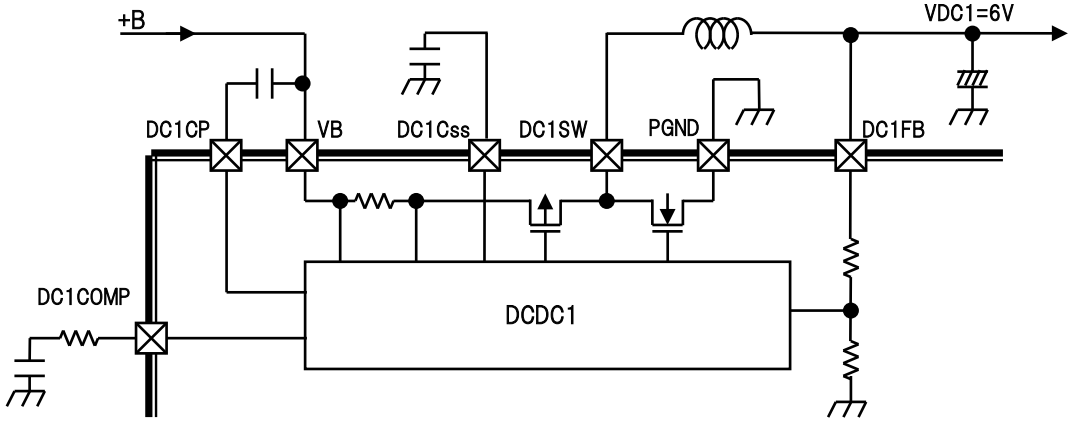
CTL1	CTL2	DCDC1	DCDC2	LDO1	LDO2	VBU	MODE
L	L	OFF	OFF	OFF	OFF	OFF	Stop
L	H	OFF	OFF	OFF	OFF	ON	Standby
H	L	ON	ON	ON	ON	ON	Active
H	H	ON	ON	ON	ON	ON	Active

8.2. DCDC converter

8.2.1. DCDC1

It is a step-down DCDC convertor (input voltage: +B, output voltage: 6 V). And it is the synchronous rectification system which built in output MOS.

- ✧ Output-current-capability: 1 A or more
- ✧ Switching frequency: 370 kHz (typ.)
- ✧ Built-in overcurrent detection (2.5A (typ.)). Duplex system is constructed by incorporating the independent control circuit of short to ground detection.
- ✧ Soft start adjustment at the voltage standup is possible by the capacitor connected with terminal DC1Css. C = 0.1 μF for 5 ms.

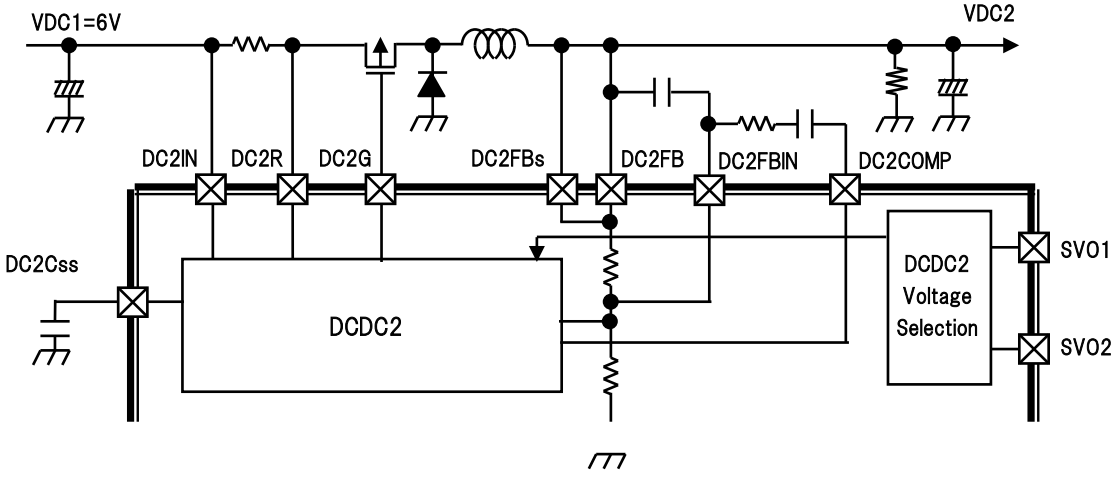


8.2.2. DCDC2

It is a step-down DCDC convertor (input voltage: 6V (VDC1), output voltage: 1.2V/1.5V). It drives the external P-ch MOS. Output voltage of 6 V of the DCDC converter 1 is used as an input voltage.

- ✧ Output-current-capability: 1.2 A or more
- ✧ Switching frequency: 370 kHz (typ.)
- ✧ The overcurrent detection by the external resistance is built in. (0.15V (typ.)). It is a voltage feedback control.
- ✧ Soft start adjustment at the voltage standup is possible by the capacitor connected with terminal DC2Css. C = 0.1 μF for 5 ms.

- Output voltage can be selected between SVO1 and SVO2. Truth table is shown below.



SVO1, SVO2 terminal: DCDC2 output voltage. Setting voltage of the input H: VDD2

SVO1	SVO2	DCDC2 output voltage (Typ.)
L	H	1.2V
H	L	1.5V
H	H	All 5 power-supply output OFF
L	L	

8.3. Series power supply

8.3.1. LDO1

- It is a series power supply with a built-in P-ch DMOS output.
- Output voltage of 6V of the DCDC converter1 should be used as the input voltage.
- Output voltage is 5V ± 0.1V. Output current is 400 mA (max). (Please set the consumption current by considering the power dissipation and the heat.)
- Please connect the phase compensation capacitor and the resistance between LDO1COMP and LDO1OUT.
- Duplex current limiter is incorporated.

8.3.2. LDO2

- It is a series power supply with a built-in P-ch DMOS output.
- Output voltage of 6V of the DCDC converter1 should be used as the input voltage.
- Output voltage is 5V ± 0.1V. Output current is 100 mA (max). (Please set the consumption current by considering the power dissipation and the heat.)
- Output of LDO2 can chose between independent mode or tracking mode to LDO1 by the SLDO2 terminal.
- Duplex current limiter is incorporated.

SLDO2 terminal: LDO2 mode. Setting voltage of the input H: VDD2

SLDO2	Operation mode of LDO1 and LDO2
L	Tracking
H	Independent

8.3.3. VBU

- It is a series power supply for retaining RAM data backup.
- Input: power supply with a built-in P-ch DMOS output connecting directly to VB.
- Output voltage is a binary change type of 5V and 3.3V. It can be chosen by the SVBU terminal. Output current is 10 mA (max).
- Only VBU power supply drives by setup of CTL1 ="L" and CTL2 ="H" (standby mode).
- It is a dark current of 250 μA (max) including VB input current, the current of CTL2 = VB (13.5V), and SVBU = VBU.
- VBU constant voltage, switching function between 5V and 3.3V, and current limiter operate in the standby mode relating to VBU. The voltage monitoring, the error logic, the SPI communication, and the thermal shutdown detection do not operate.
- Duplex current limiter is incorporated.

SVBU terminal: VBU output voltage, setting voltage of the input H: VBU

SVBU	VBU output voltage
L	3.3V
H	5V

8.4. Abnormality detection

8.4.1. The voltage abnormality detection of a power supply output

High-voltage detection is incorporated in outputs of all 5 power supplies and low-voltage detection is incorporated in four power supplies except DCDC1. Each detection result is inputted into error logic, and if any of high-voltage or low-voltage is detected, NDIAG will be outputted from error logic. Normal state: NDIAG ="H", high-voltage or low-voltage: NDIAG ="L".

If the high-voltage is detected by either DCDC2 or LDO1, NOVDET terminal other than NDIAG terminal output the abnormal flag. Normal state: NOVDET ="H", high-voltage: NOVDET ="L".

If the low-voltage is detected by either DCDC2 or LDO1, NRSTA and NRSTB terminals other than NDIAG terminal output the reset signal. As for the reset signal operation, please refer to "8.8 Reset timer".

The output to NOVDET and NRSTA&B corresponds only to DCDC2 and LDO1 of a microcomputer power supply.

The list of operation of high-voltage detection values and the list of low-operation detection values are shown below.

The list of operation of high-voltage detection values

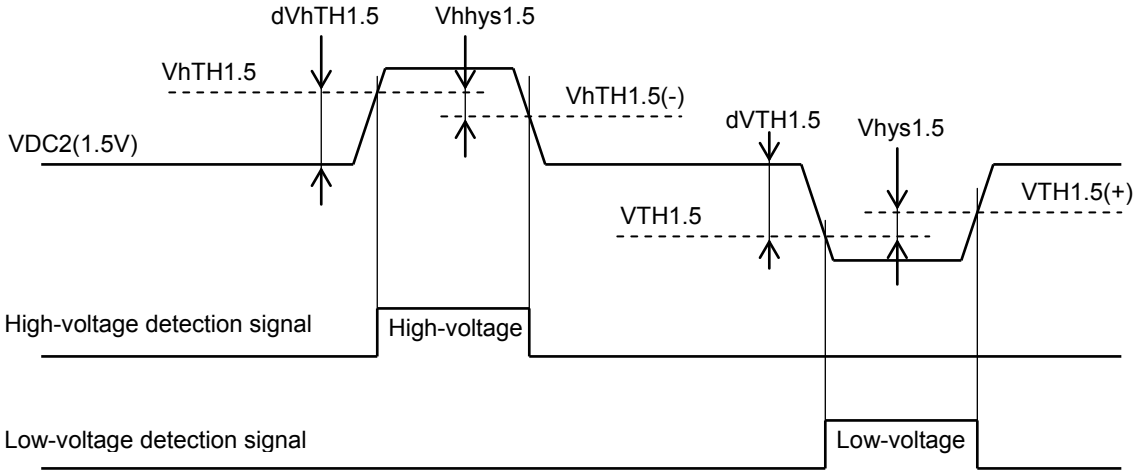
Monitor power supply	Output voltage DC1,2, LDO1,2,VBU	Detection voltage VhTH	Release voltage VhTH (-)	The signal output in detection		
				NDIAG	NOVDET	NRSTA&B
DCDC1	6.0V	6.6V	6.5V	L	H	H
DCDC2	1.20V	1.27V	1.24V	L	L	H
	1.50V	1.61V	1.58V			
LDO1	5.0V	5.3V	5.2V	L	L	H
LDO2	5.0V	5.3V	5.2V	L	H	H
VBU	5.0V	5.3V	5.2V	L	H	H
	3.3V	3.5V	3.45V			

The list of operation of low-voltage detection values

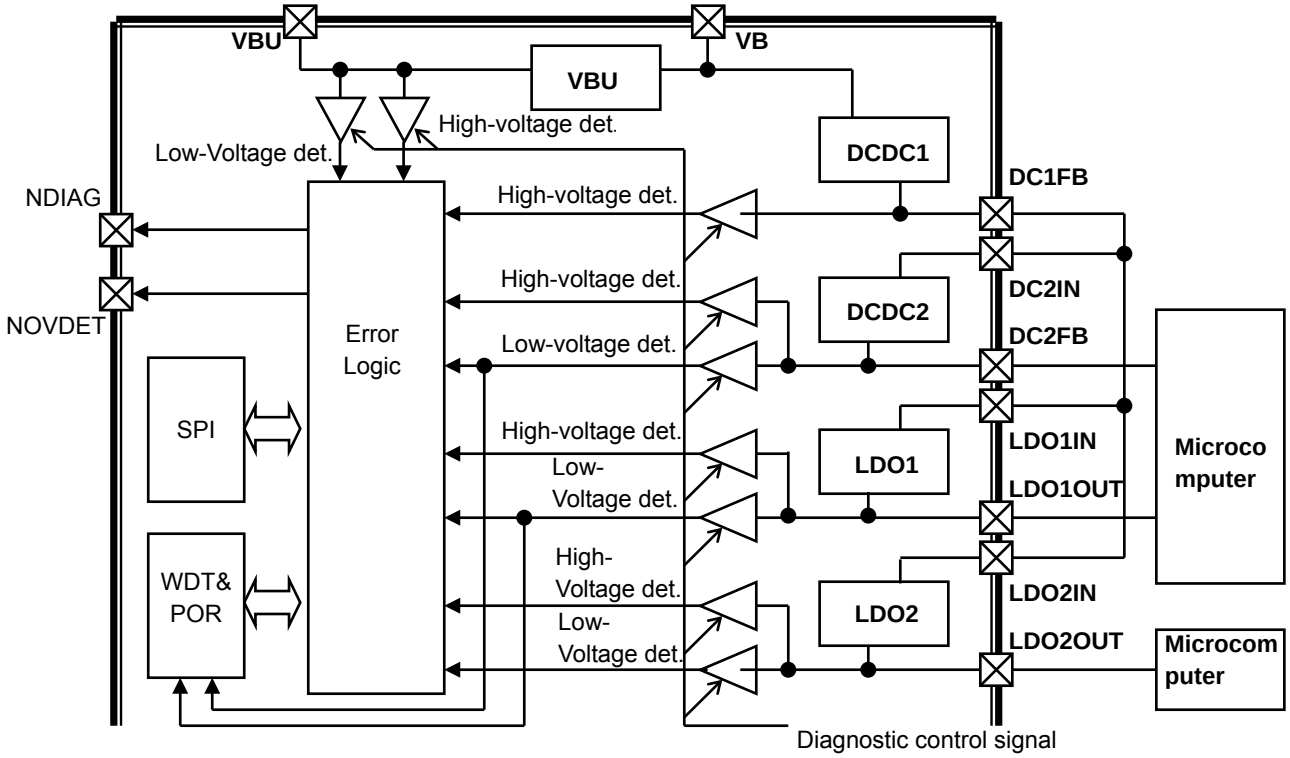
Monitor power supply	Output voltage DC1,2, LDO1,2,VBU	Detection voltage VTH	Release voltage VTH(+)	The signal output in detection		
				NDIAG	NOVDET	NRSTA&B
DCDC1	6.0V	-	-	H	H	H
DCDC2	1.20V	1.13V	1.16V	L	H	L
	1.50V	1.39V	1.42V			
LDO1	5.0V	4.7V	4.8V	L	H	L
LDO2	5.0V	4.7V	4.8V	L	H	H
VBU	5.0V	4.7V	4.8V	L	H	H
	3.3V	3.1V	3.15V			

8.4.2. Timing chart: High-voltage & Low-voltage detection operation

The sign has written 1.5V setup of DCDC2 on the example. Please confirm it in conjunction with "15.Electrical Characteristics".



8.4.3. Block diagram of High-voltage & Low-voltage detection function



8.5. Self-diagnostics control of a detection mechanism

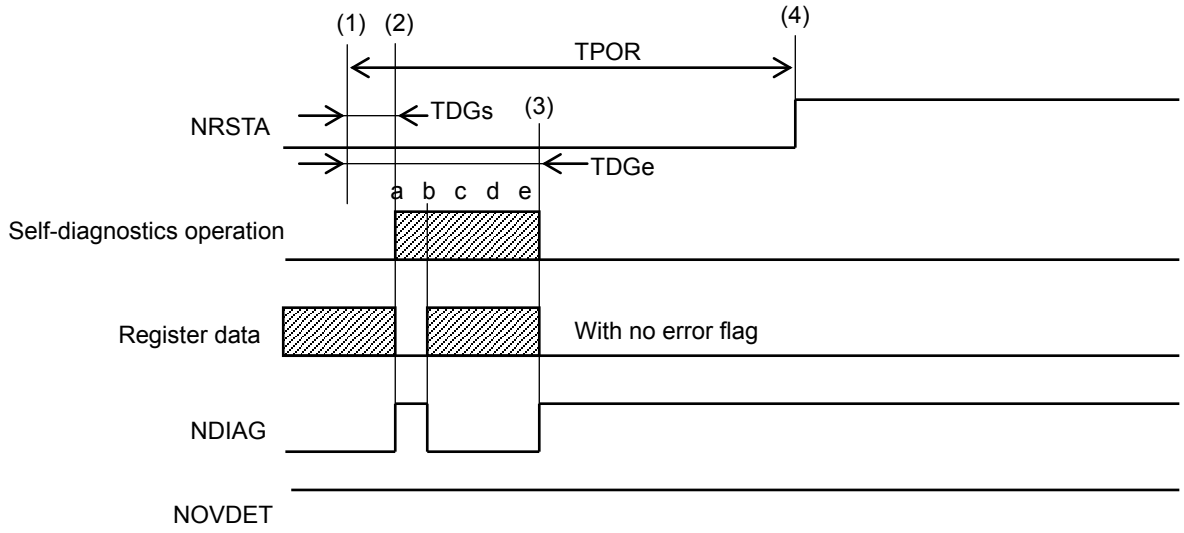
During power-on reset, self-diagnostics control of the voltage monitoring function of each power supply, a reset output, and an alarm output is performed. Self-diagnostics control is performed only at the time of the power-on reset just after powering on. It does not perform at the time of the power-on reset when the output voltage decreases and the operation returns.

The operation sequence of self-diagnostics is described in “Timing chart of the diagnostic result OK” and “Timing chart of the diagnostic result NG”.

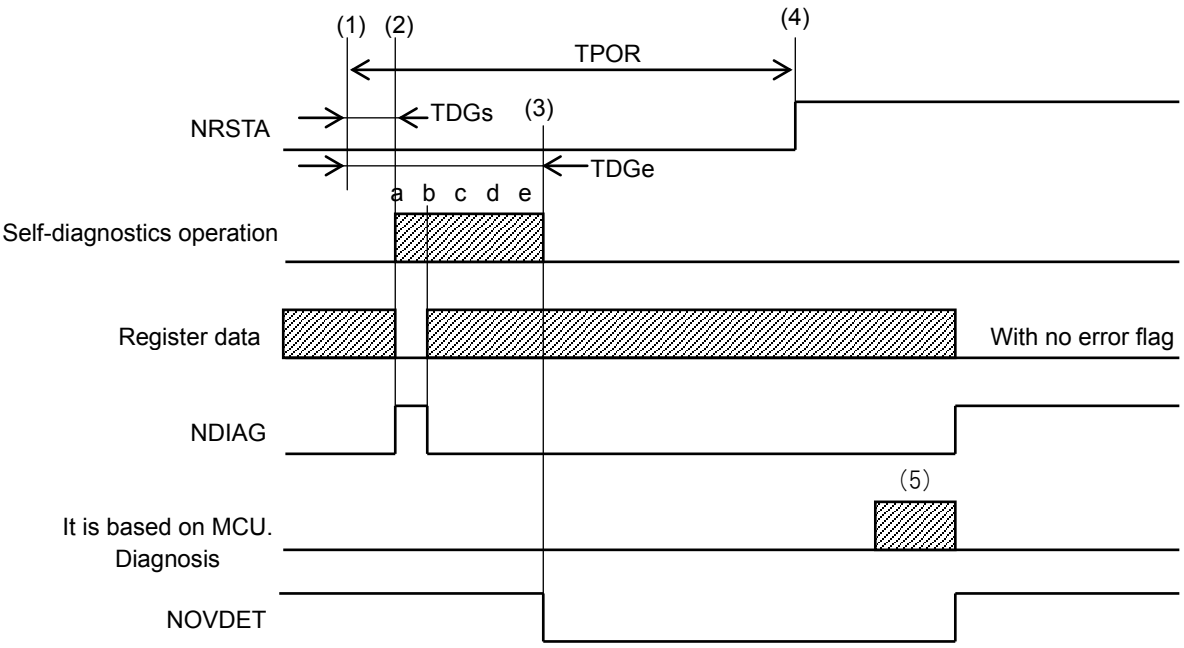
(1)	DCDC2 and LDO1 rise and the low-voltage detection is canceled. The power-on reset TPOR starts. The output of NDIAG holds “L."	
(2)	A self-diagnostics sequence is started after TDGs. a: The register data is cleared (clear monitoring the low-voltage which is generated in powering on, and the flag of current limiter) NDIAG outputs high. b: Operate the low-voltage monitoring function of each power supply output forcedly. The result is written to the register. NDIAG outputs low. c: Operate the high-voltage monitoring function of each power supply output forcedly. The result is written to the register. d: Output the MCU alarm and the reset timer forcedly. The result is written to the register. e: The data of the register is compared with an expected value and diagnose.	
(3)	When a diagnostic result is OK The data of the register is cleared. The output of NDIAG becomes "H". The output of NOVDET continues to be “H"	When a diagnostic result is NG NOVDET outputs "L". The data of the register is held. The output of NDIAG holds "L." A flag is written in the address of the diagnostic result.
(4)	POR is canceled.	
(5)	When a diagnostic result is OK MCU is not processed.	When a diagnostic result is NG The treatment on the system support NOVDET="L." MCU reads out abnormal data from this product by using SPI. (Request to MCU) The output of NDIAG becomes "H" if the data of a register is cleared.

In interlocking to self-diagnostics operation, repeated reversal operation of NDIAG output is also diagnosed.

Timing chart of the diagnostic result OK



Timing chart of diagnosis result NG



8.5.1. Diagnostic control of high-voltage and low-voltage detection

Self-diagnostics control of high and low-voltage detection of each power supply is operated forcedly by switching the threshold value of each voltage detection during diagnostics control. The result is written to the register as the error information.

While high and low-voltage is detected by the diagnostic control, the data is written to the register and DIAG signal is outputted (NDIAG="L"). NOVDET does not output and a reset output is not performed.

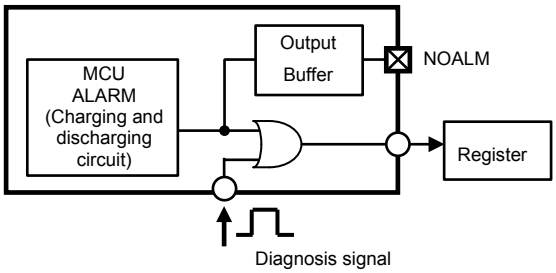
Please refer to “8.4.3 Block diagram of high-voltage and low-voltage detection function”.

8.5.2. Register diagnostic control of MCU alarm information

In diagnostic controlling, writing an abnormal signal to the register of MCU ALARM is confirmed by inputting the diagnosis signal as shown in the following block diagram.

In diagnosis, DIAG signal (NDIAG = “L”) outputs but NOALM signal does not output.

MCU ALARM

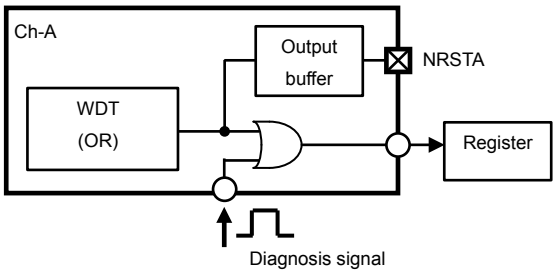


8.5.3. Register diagnostic control of WDT information

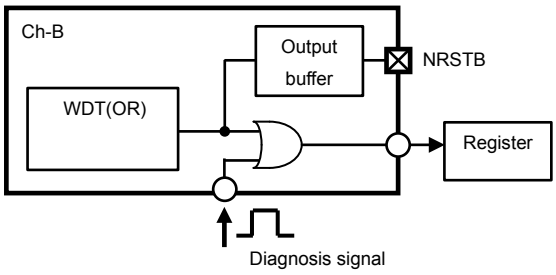
In diagnostic controlling, writing detection information of a watchdog timer operation to the register is confirmed by inputting the diagnosis signal as shown in the following block diagram.

In diagnosis, DIAG signal (NDIAG = “L”) outputs.

WDT A



WDT B



8.6. Overcurrent detection operation

The overcurrent detection is built in each power supply. This overcurrent detection consists of circuits which is independent of the power supply. It operates normally though the power supply performs abnormal operation.

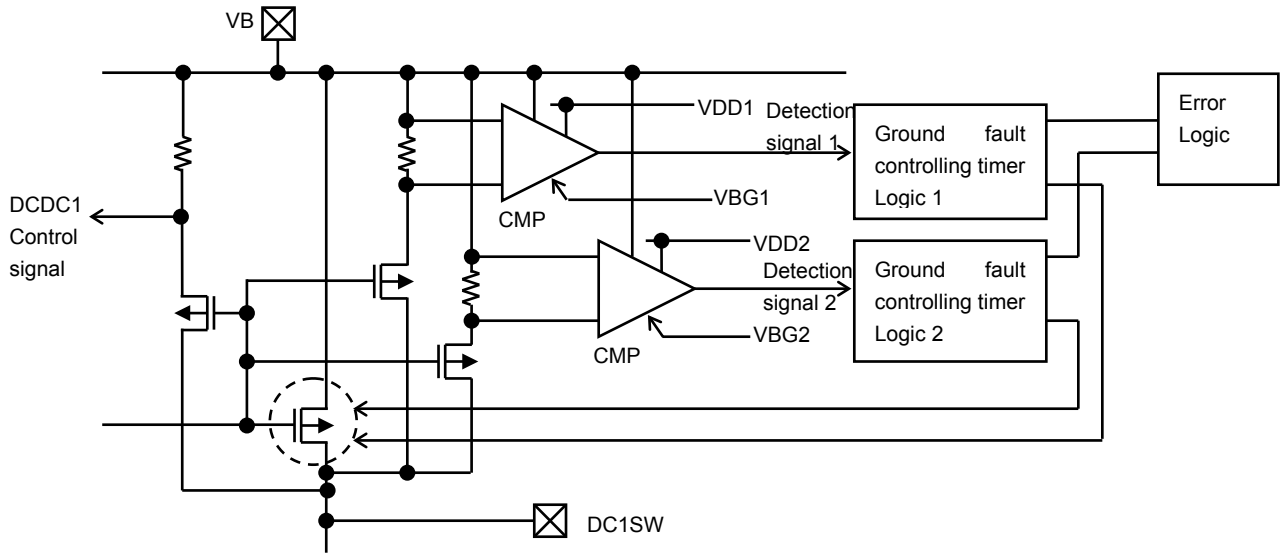
8.6.1. Overcurrent detection of DCDC1

DCDC1 detection & control system

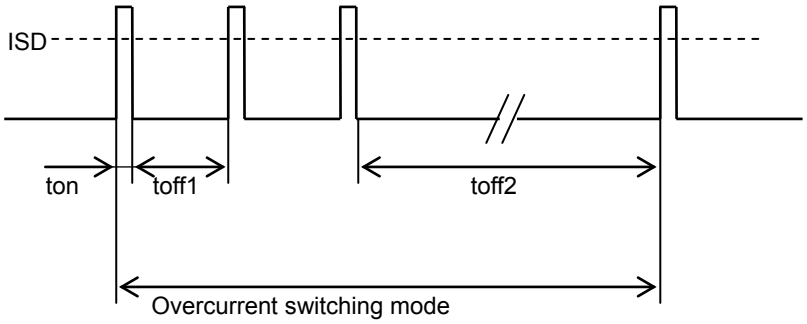
A detection value is 2.5A (typ.) and incorporated P-ch DMOS is turned off in detection. It turns on after a definite period of time, and if overcurrent is detected again, it turns off again (switching mode). When the over current state continues even if this mode repeats 8 times, an off-latch is carried out, and DCDC1 power-supply function stops (No notice to MCU). Please refer to the below timing chart "ON/OFF switching in over current detection (DCDC1)".

Current detection is performed by built-in detection resistance. The circuit configuration is as follows.

Two over current detection blocks are composed independently. Detection resistance, VDD and VBG of detection CMP are independent. Abnormal information is outputted to the error logic when over current is detected.



ON/OFF switching in over current detection (DCDC1)



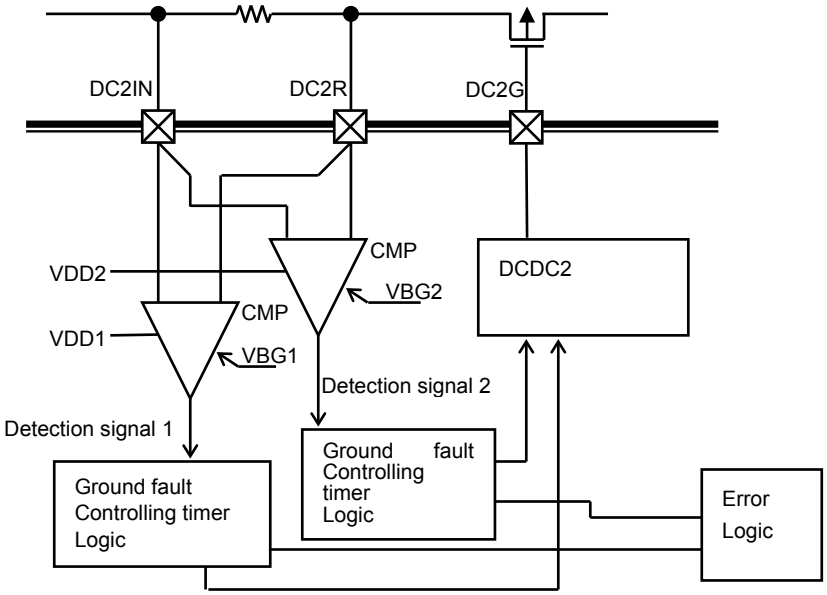
8.6.2. Overcurrent detection of DCDC2

DCDC2 detection & control system

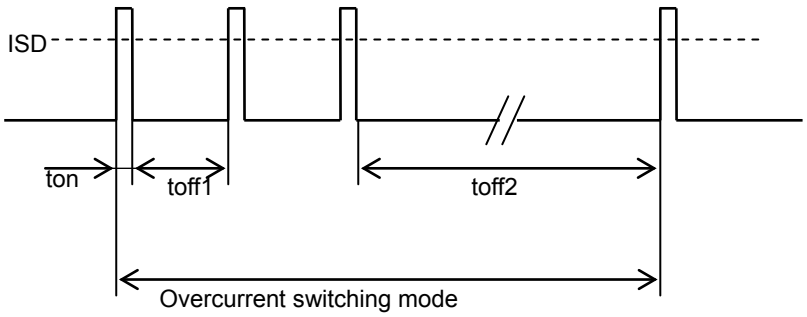
A detection value is 0.15V (typ.) and external P-ch MOS is turned off in detection. It turns on after a definite period of time, and if overcurrent is detected again, it turns off again (switching mode). When the over current state continues even if this mode repeats 8 times, an off-latch is carried out, and DCDC2 power-supply function stops (No notice to MCU). Please refer to the below timing chart "ON/OFF switching in over current detection (DCDC2)".

Current detection is performed by external detection resistance. The circuit configuration is as follows.

Two over current detection blocks are composed independently. VDD and VBG of detection CMP are independent. Abnormal information is outputted to the error logic when over current is detected.



ON/OFF switching in over current detection (DCDC2)



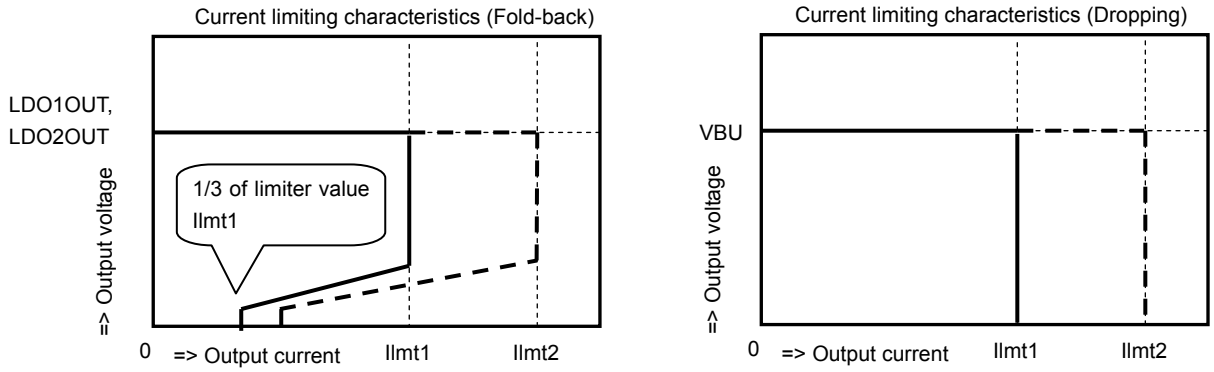
8.6.3. Overcurrent detection of LDO

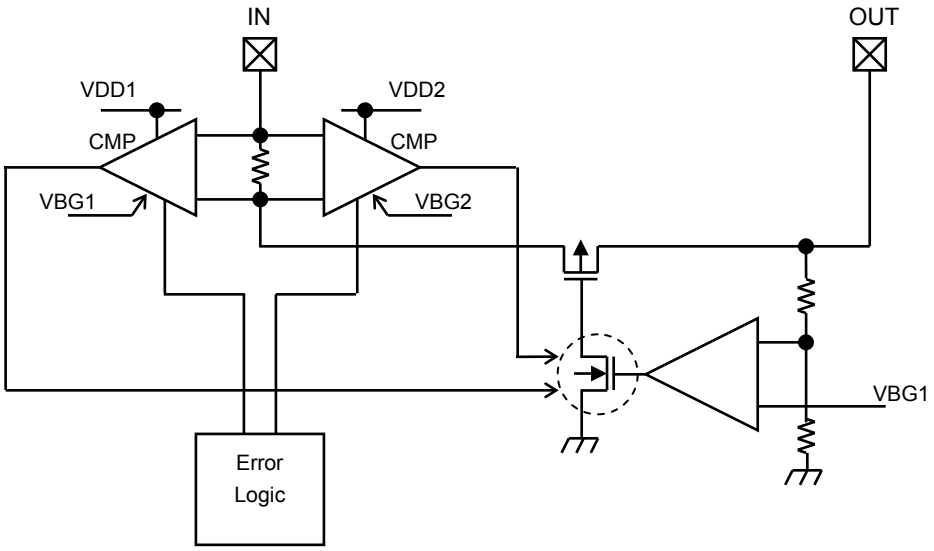
The independent current limiting function is built in LDO each power supply. This current limiting has double structure which has a difference of a detection value.

The signal of limiter operation is inputted into error logic, and an abnormal generation is notified.

Two over current limiting blocks are composed independently. VDD and VBG of detection CMP are independent.

Power supply	Current limiting detection value (typ.)	Control system
LDO1	800mA	Fold-back characteristic
	1200mA	Fold-back characteristic
LDO2	200mA	Fold-back characteristic
	300mA	Fold-back characteristic
VBU	20mA	Dropping characteristic
	40mA	Dropping characteristic

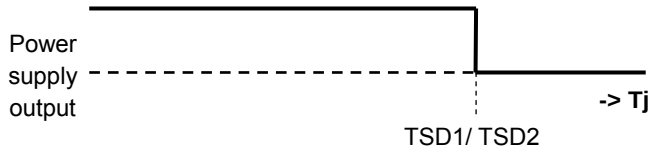


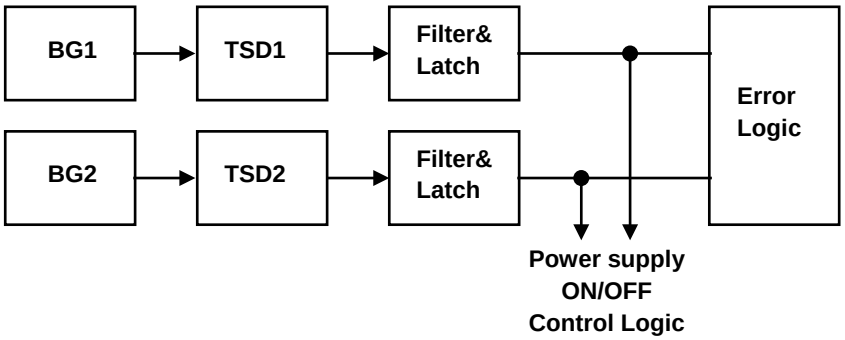


8.7. Thermal shutdown detection

This product incorporates two thermal shutdown detections. When the junction temperature Tj exceeds the thermal shutdown detection temperature (TSD1) or TSD2 (170°C (typ.)), all power supply circuits (DCDC1, DCDC2, LDO1, LDO2, and VBU) are latched OFF and stop. To release the latch, re-starting the power supply function with CTL1 and CTL2 or re-applying the power supply of VB is required.

Filter is adopted for each TSD output in order to prevent the malfunction of detection by noise. Setting time is 15μs (Typ.).





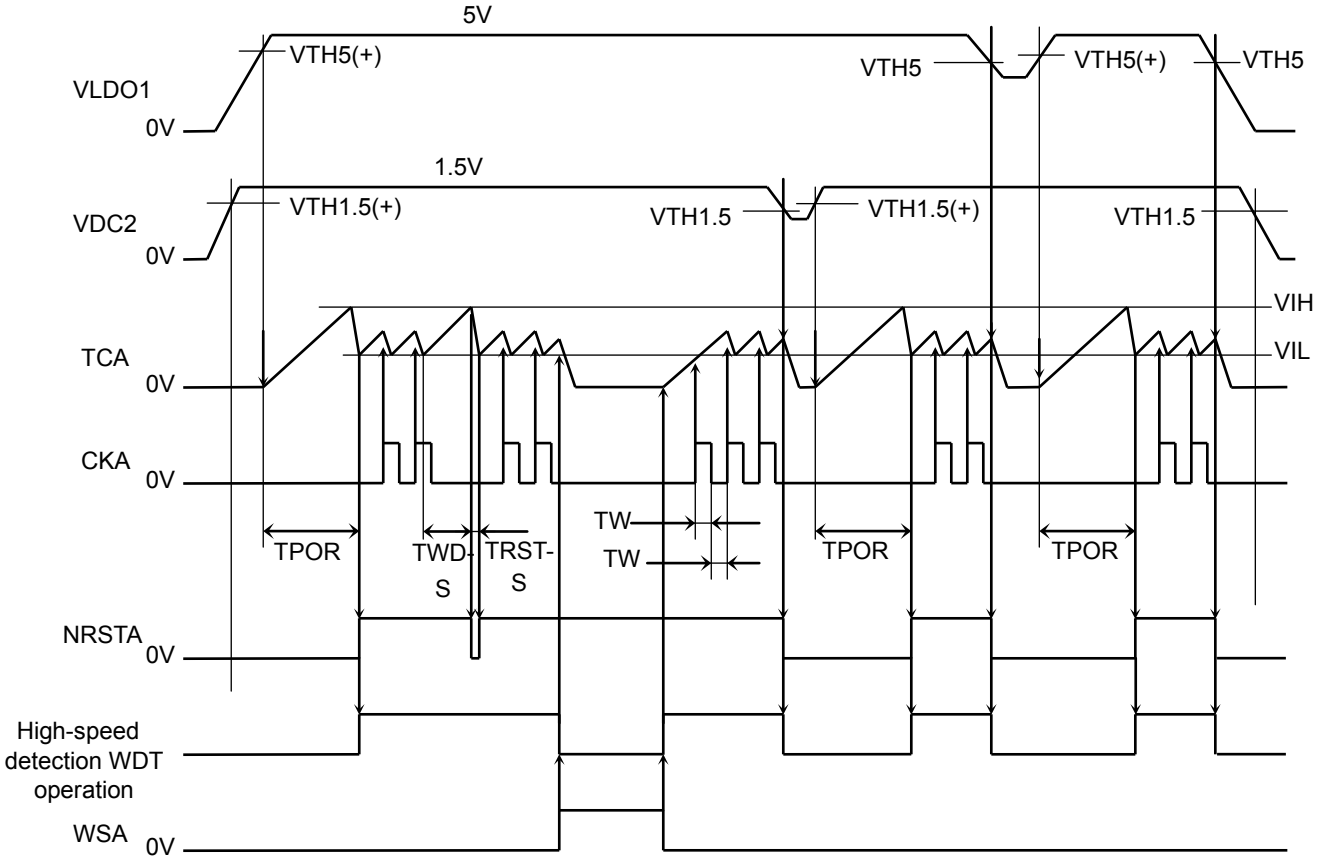
8.8. Reset timer

8.8.1. Power-on reset & watchdog timer

The TB9042FTG has two independent watchdog timers. Setting timer and inputting clock are possible for each. However, a voltage monitoring signal is common. So, if the output voltage of either DCDC2 or LDO1 falls, both Ch-A and Ch-B output the reset signals. And if both DCDC2 and LDO1 output the normal voltages (VTH or more), both of timer functions start operating.

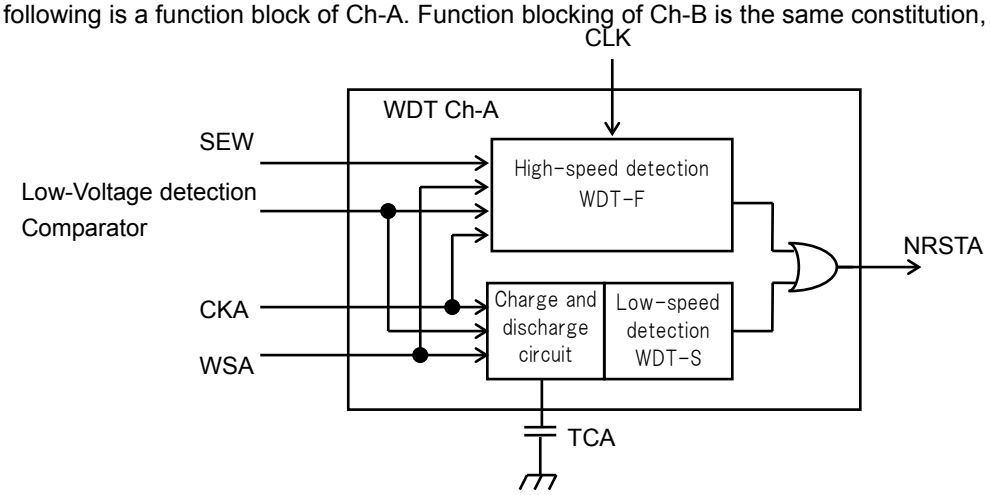
It is a window type which detects both the low-speed and high-speed abnormalities of a watch dog pulse, and if either is detected, the reset signal NRST is outputted. Please refer to “Watchdog timer functional block”.

Timing chart of the timer is indicated by describing “the single system of Ch-A and VDC2=1.5V”.



Watchdog timer functional block

The following is a function block of Ch-A. Function blocking of Ch-B is the same constitution, too.



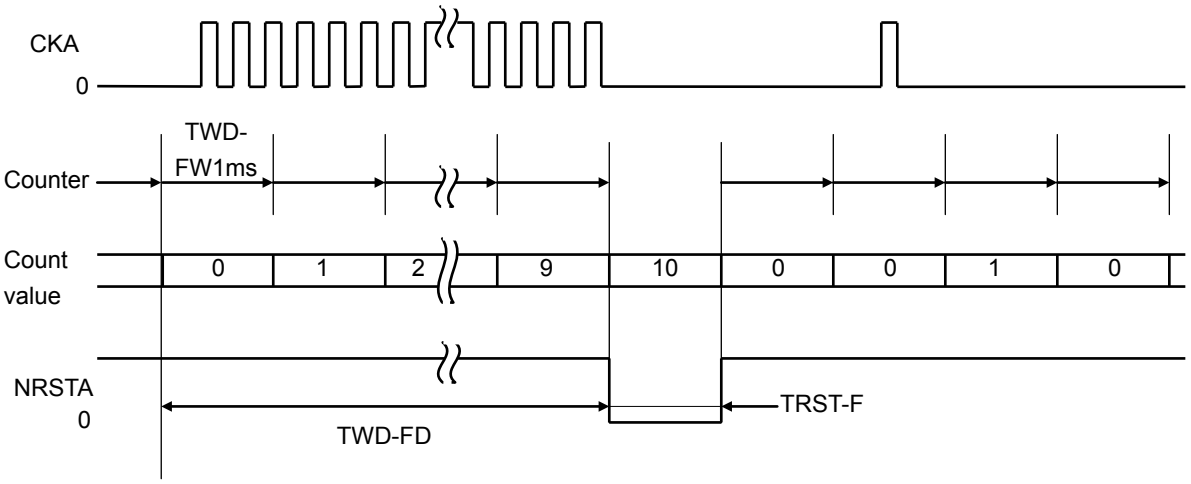
8.8.2. Detection of the high-speed abnormalities of a watch dog pulse

The detection sequence of the clock high-speed abnormalities of a window type watch dog is shown below.

Clock existence is judged at a counter for 1 ms, and reset is outputted when it detects consecutive ten times.

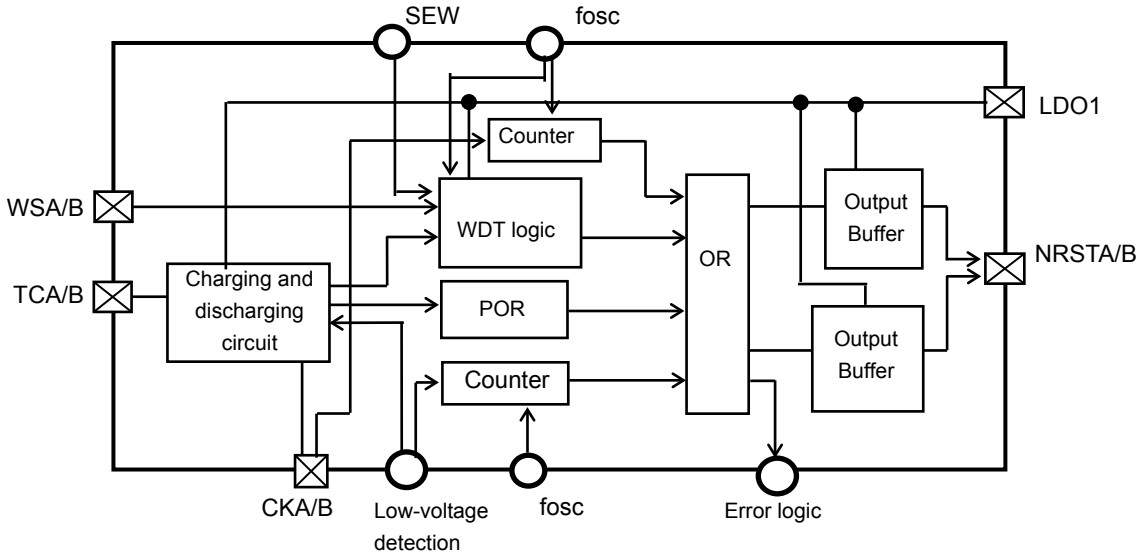
Function enable: SEW terminal = “L”, Function disable: SEW ="H"

This selection is fixed in determining application circuit. Please do not switch the selection in operating the IC.



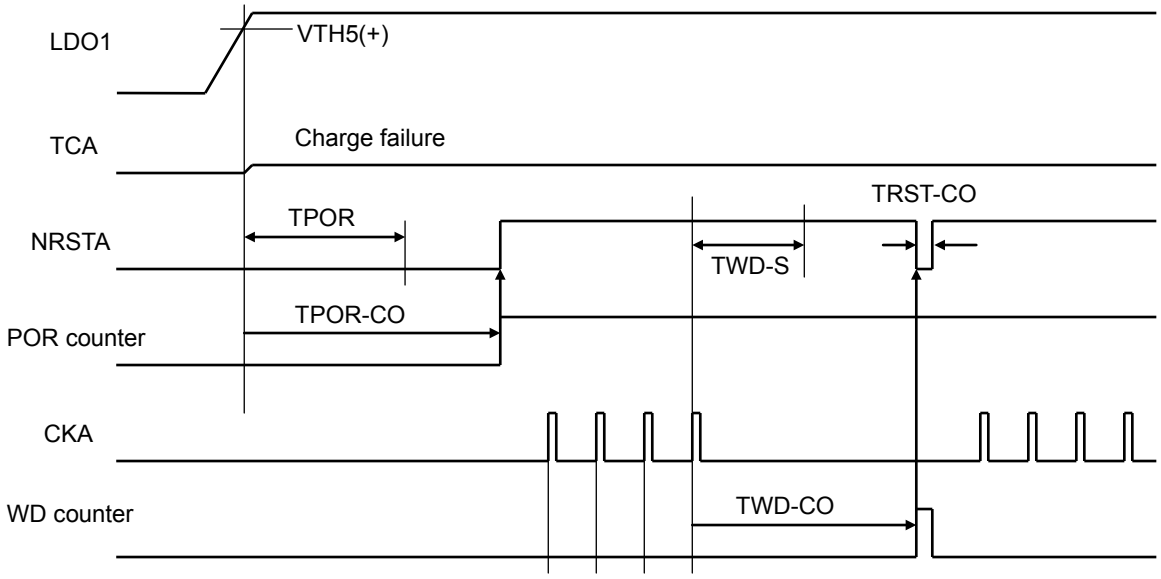
8.8.3. Details of a function

- In order to avoid fixing “H" for NRST by failure of an output buffer, the buffer of the output unit of NRST has duplex structure. Outputting “L” is possible in abnormal operation by operating either buffer in normal.
- In order to avoid being impossible to output reset by failure of a charging and discharging circuit, a counter is configured. When there are no clocks into CK terminal exceeding setup time of the counter (TPOR-CO and TWD-CO), the reset signal is outputted.
- High-speed abnormal detection is configured in WDT logic.



8.8.4. Timing chart (operation of a counter)

When charge-discharge circuit for timer set is out of order, the operation of POR&WDT-S is shown in the below chart. At failure, reset signal does not react though the voltage exceeds the configured TPOR and TWD-S. So, it operates by the counter-configured values of TPOR-CO and TWD-CO.



8.9. MCU alarm

8.9.1. Functional outline

2-bit signal is inputted into two terminals of INALM0 and INALM1 from MCU. INALM0 = 1 and INALM1 = 0 are judged OK, and others are judged NOK. The signal of NOK from MCU continues to output for TALM (Please refer to “15.Electrical characteristics”), "L" will be outputted from NOALM.

Since MCU is outputting NOK in the state where the reset signal (NRSTA="L") is applied to MCU, the timer stops by setting TCALM "L".

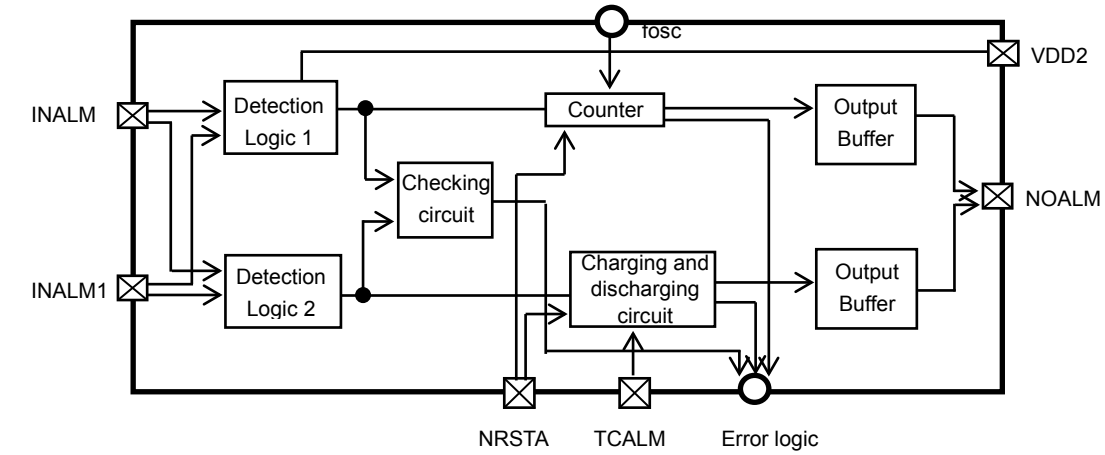
A MCU alarm function is not interlocked with NRSTB.

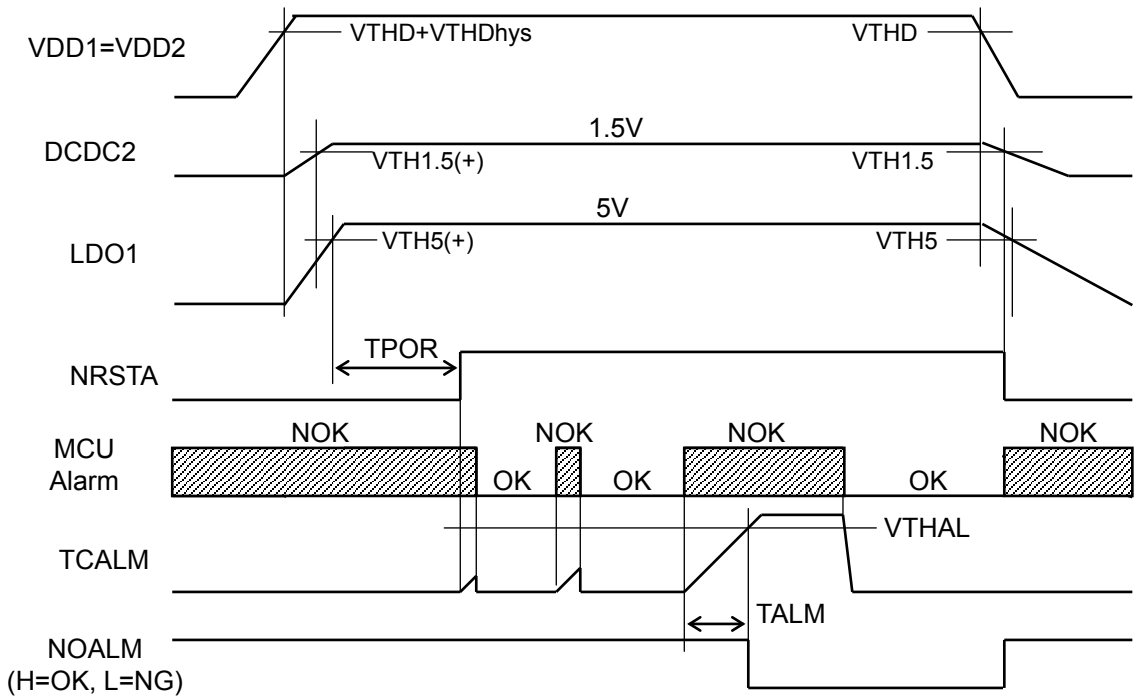
	OK	NOK	NOK	NOK
INALM0	1	0	0	1
INALM1	0	1	0	1

In order to avoid fixing “H" for NOALM by failure of an output buffer, the buffer of the output unit of NOALM has duplex structure. Outputting “L” is possible in abnormal operation by operating either buffer in normal.

In order to avoid being impossible to judge NG by failure of a charging and discharging circuit, a counter is configured. NOK continues for counter setting time (TALM-CO), NOALM outputs "L."

While it is reset by NRSTA, this counter stops.

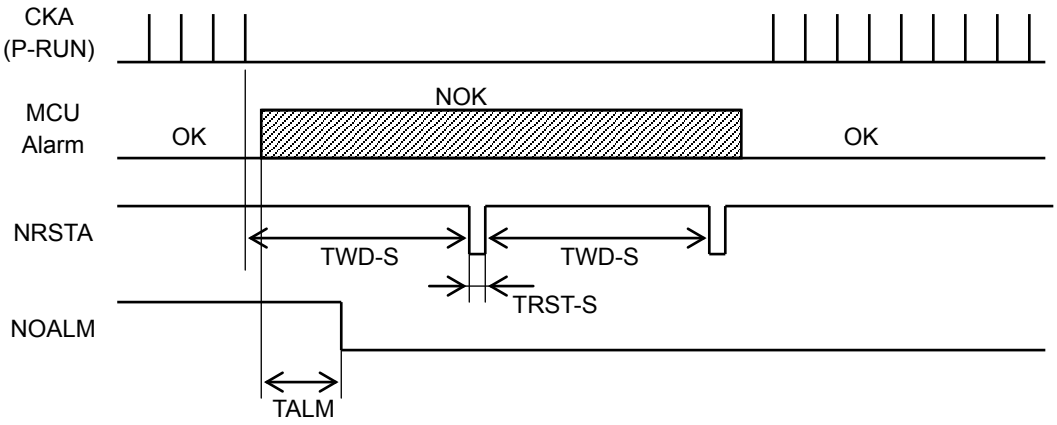




8.10. Relation between MCU alarm and a reset timer (POR, WDT)

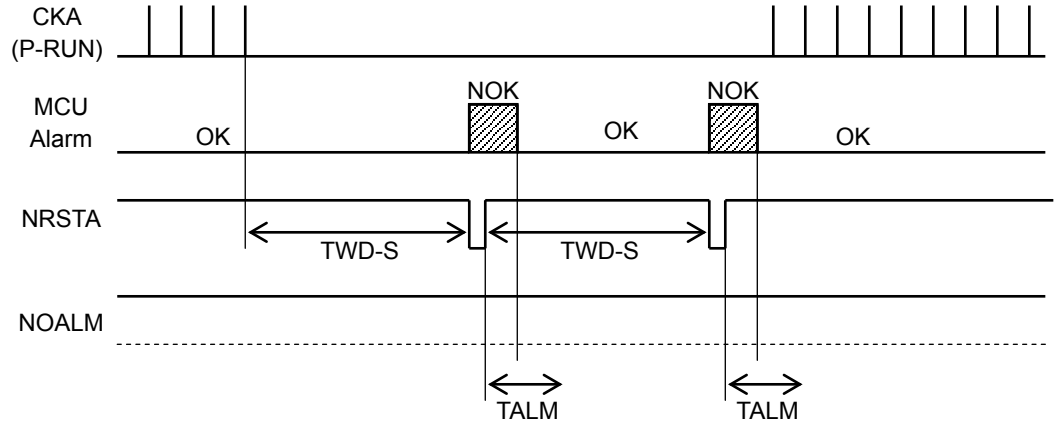
8.10.1. When MCU was set to NOK and CKA stops (INTALM1:0 ="00, 10, 11")

When MCU was set to NOK, and CKA stops, NOALM signal outputs after TALM and the reset signal outputs after TWD-S. Although the operation returns to the normal state by resetting MCU (NRSTA="L"), NOALM continues to output "L" (Latch state).



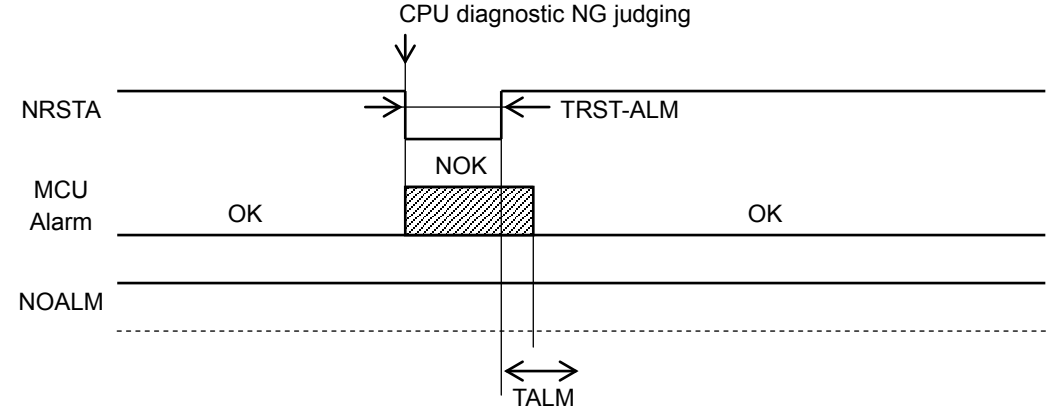
8.10.2. When CKA stops while MCU is in OK state (INTALM1:0 ="01")

When CKA stops while MCU is in OK state, MCU moves to NOK state during reset or initial set after release. NOALM does not output by setting as follows; NOK time after reset < Filter time of NOALM (TALM)



8.10.3. When the result of the MCU diagnosis using SPI is NG

When result of MCU diagnosis using SPI is NG, the reset signal TRST-ALM is outputted. MCU alarm is set NOK during reset and in initial set after release. NOALM does not output by setting as follows; NOK time after reset < Filter time of NOALM (TALM)



9. SPI communication

9.1. The functional outline by SPI communication

The SPI communication with the IC is performed by the fixed bit length of 16 bits. Please communicate by configuring as follows; the IC: a slave side, MCU: a master side.
The function which the IC can realize by SPI communication has the two modes.

- Error status communicate mode

It transmits the error, which is detected in the IC, from the IC to the MCU.

Error information: Error information which is generated in the IC, and error information judged by the following data test mode.
Please refer to “10.2 The contents of error information."

- Data test mode

The IC judges the data transmitted from the MCU.

Error status communicate mode

MCU can recognize the error detected by the IC, and can carry out control and operation depending on every error. The IC outputs NDIAG ="L" when the error is detected in the IC or NG is judged by the data test mode. MCU can recognize generating of errors by using this signal as an external trigger.

MCU transmits an applicable address, in order to acquire the status information of the error. The IC transmits the status information of the error corresponding to the address, after it receives an address. For details, please refer to 9.3 Details of a function by SPI communication. (Address 1 to 4)

Data test mode

It monitors the MCU function using SPI communication. For example, it can be used for monitoring the calculation function in MCU and ADC, etc.

The IC has three kinds of functions for checking the function of MCU, and expected value data of every function. Moreover, the address is assigned to each expected value. If the address and the data for a check corresponding to the address are transmitted from MCU, the diagnostic mechanism of the IC compares the expected value applicable to the address and the transmitted data for a check, and detects the abnormal operation of MCU. For details, please refer to “9.3 Details of a function by SPI communication”.

The outline of each function is explained below.

- Function1
  - It is a judging-data function which consists of eight frames (one frame: 16 bits). (The data bit: 64 bits)
  - Contents of a judgment: A data comparison, sequence surveillance, Timeout function
  - Sequence surveillance: The order of the address transmitted to the IC from MCU is monitored. (Order of the address: 5 to 12)
  - Timeout function: The 1st time to the 2nd communication gap time of this communication is monitored.
  - NG judging outputs: Reset signal and NDAIG signal are outputted to MCU from the IC. (NRSTA ="L", NDIAG ="L").The reset signal of NRSTB is not outputted.
- Function2
  - It is a judging-data function which consists of two frames (one frame: 16 bits). (The data bit: 16 bits)
  - Contents of a judgment: A data comparison, sequence surveillance
  - Sequence surveillance: The order of the address transmitted to the IC from MCU is monitored. (Order of the address: 13 and 14)
  - Timeout function: Nothing
  - NG judging outputs: NDIAG signal is outputted to MCU from the IC (NDIAG ="L").

- Function3
  - It is a judging-data function which consists of four frames (one frame: 16 bits). (The data bit: 32 bits)
  - Contents of a judgment: A data comparison, sequence surveillance
  - Sequence surveillance: The order of the address transmitted to the IC from MCU is monitored. (Order of the address: 15 to 18)
  - Timeout function: Nothing
  - NG judging outputs: A NDIAG signal is outputted to MCU from the IC (NDIAG ="L").

The example of application for data test mode

<> Function1

- The example of assumed application: The IC monitors the calculation function of MCU. (Monitoring critical fault)

Calculation function of the MCU calculates to gain the specific expected value and transmits it to the IC.

The expected value and the calculation value from MCU are compared, and judged match or mismatch.

The IC judges only the comparison of the expected values. The calculation method to gain the expected values can be programmed by MCU. So, configure the effective pattern for monitoring the calculation function depending on soft or hard of the MCU arbitrary.

The number of frames that the IC compares and judges is 8. The address and the expected values are configured at each frame. Therefore, as for the MCU, configure eight calculation patters.

The address and the expected values of eight frames are indicated in the following table. All expected values are set up the prime number.

Frame address	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch
Expected value data	233	229	227	211	199	197	193	181

- Processing in judgment

Since the surveillance of the calculation function of the MCU is assumed, when a judged result is NG, a serious error on a system is considered. So, the IC resets the MCU.

In OK judgment, no reaction to the MCU

<> Function2

- The example of assumed application: The IC monitors the ADC of the MCU.

The voltage divided from the voltage of VDD2 of the IC is inputted into ADC of the MCU. This voltage is read by the MCU and arbitrary expected value is calculated based on this voltage. The calculation value is transmitted to the IC. The expected value and the calculation value from MCU are compared, and judged match or mismatch.

The IC judges only the comparison of the expected values. The calculation method to gain the expected values and the read value by ADC can be configured by the MCU and the external conditions of the IC arbitrary. So, configure the effective pattern for monitoring the calculation function.

The number of frames that the IC compares and judges is two.

The address and the expected values of two frames are indicated in the following table. All expected values are set up the prime number.

Frame address	0Dh	0Eh
Expected value data	179	173

- Processing in judgment

Since the surveillance of ADC is assumed, when a judged result is NG, the result is informed by SPI communication.

Generation of abnormality is informed by NDIAG output becomes low. The abnormalities of ADC can be recognized by taking error information into MCU using the error-status communication mode of SPI.

<> Function3

- The example of assumed application: The IC monitors the calculation function of MCU. (Monitoring minor fault).

Calculation function of the MCU calculates to gain the specific expected value and transmits it to the IC

The expected value and the calculation value from MCU are compared, and judged match or mismatch.

Function1 assumes the critical fault resetting on the system when mismatch generates. And Function3 assumes the minor fault without reset.

The IC judges only the comparison of the expected values. The calculation method to gain the expected values can be programmed by MCU. So, configure the effective pattern for monitoring the calculation function depending on soft or hard of the MCU arbitrary.

The number of frames that the IC compares and judges are 4. The address and the expected values are configured at each frame. Therefore, as for the MCU, configure four calculation patters.

The address and the expected values of four frames are indicated in the following table. All expected values

are set up the prime number.

Frame address	0Fh	10h	11h	12h
Expected value data	167	163	157	151

- Processing at the time of a judgment

The surveillance of the calculation function of the MCU is assumed for minor fault. SO, when a judged result is NG, it does not reset the MCU. It informs the generation of the abnormality from NDIAG as same as Function2.

9.2. Communication outline

The IC reads receiving data in falling edge of a communication clock while NSCS is "L", and outputs transmitting data in rising edge synchronization of a communication clock. Please transmit the transmitting data at the rising edge of the communication clock.

In addition, please communicate by setting NSCS "L" for every frame.

It communicates at MSB first. It communicates by the fixed bit length of 16 bits.

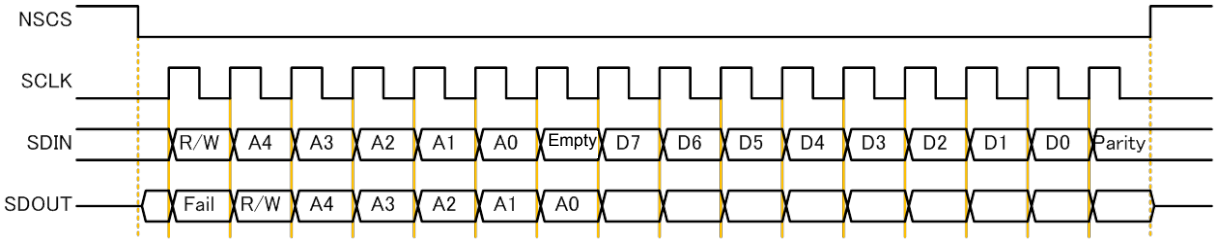
9.2.1. Terminal explanation

- NSCS: It is a chip-select input. It communicates while the input to NSCS is “L” (un-communicating: “H”)
- SCLK: It is a serial clock input. Please input a maximum of 4-MHz clock.
- SDIN: It is a serial communication input.
- SDOUT: It is a serial communication output. Output of SDOUT is High-z while input to NSCS is "H".

9.2.2. Communication format

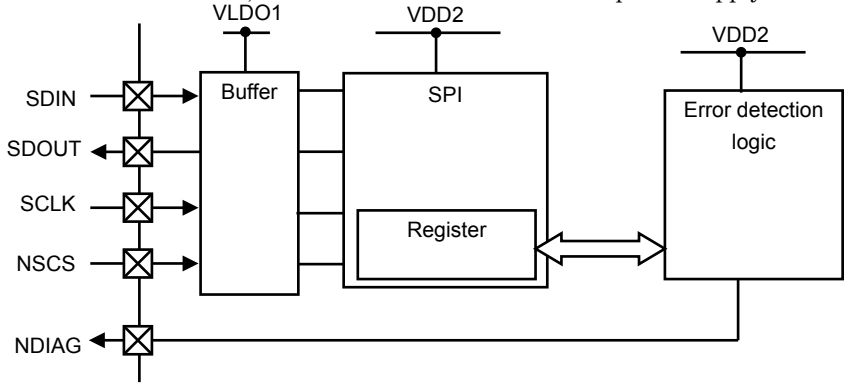
Transmission speed	Up to 4 MHz
Communication unit	Frame (one frame is the fixed bit length of 16 bits)
Frame	SDIN: Read and write + address + empty bit+ data + Parity SDOUT: Fail+ read and write + address + data + Parity
Read/Write bit	1 bit (0 : Communication mode of error status, 1 : Data test mode)
Address	5 bits
Data	8 bits
Parity bit	Odd parity for read and write + address + data An empty bit is also included in a parity account.
Fail bit	In the following case, SPI communication judges as a communication fault. Fail bit is set "1" by the next communication. - When a reception frame is except 16 bits - In the case of a parity check error

A communication format is shown below. For details, please refer to “9.4 Details of communication”.



9.2.3. Block diagram

Interface of SPI (buffer) uses VLDO1, and SPI circuit uses VDD2 as a power supply.



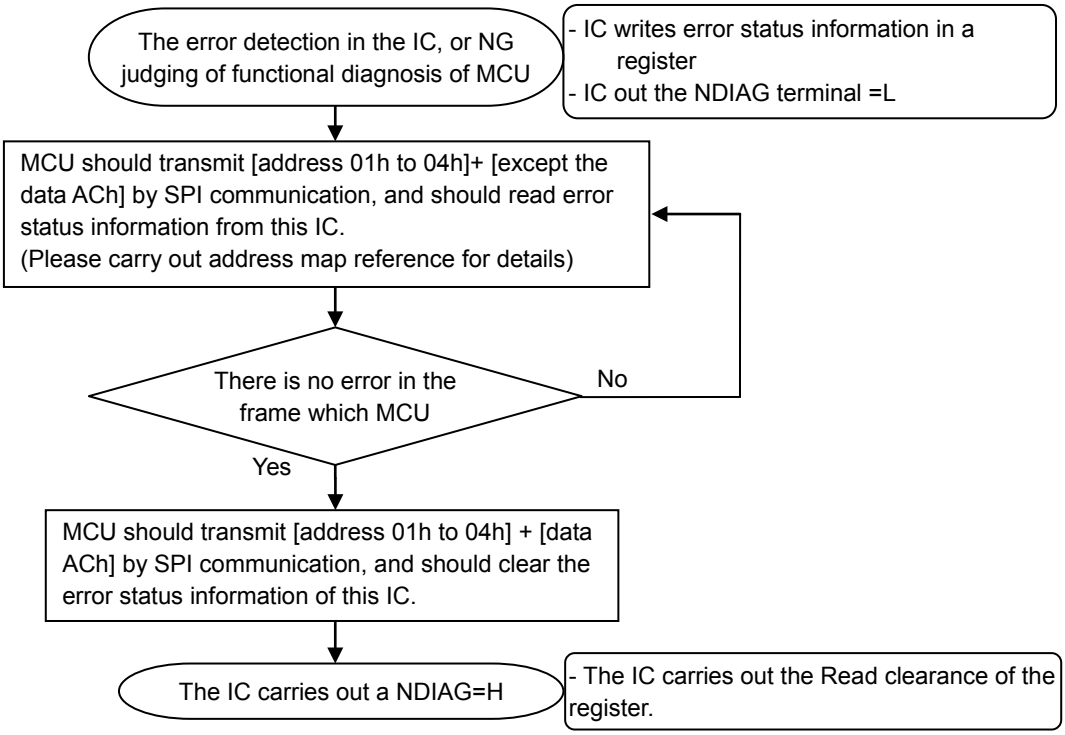
9.3. Details of a function by SPI communication

9.3.1. Error status communicate mode

NDIAG outputs "L" when the error is detected in the IC and the diagnostic result of the MCU function is NG. The status information of the error is written in the register of this IC. MCU uses the signal of NDIAG ="L" as an external triggering signal.
MCU transmits the address of 1 to 4, in order to acquire error status information. (As for error status information, please refer to “10.2 The contents of error information”.
The IC transmits the status information of the error corresponding to the address, when it receives the address. Only an address portion is required to read error information from the IC. However, using a data part, setting of the read & clearance or only a read of the error information of the register can be selected.
- If a data part reads by ACh, the error information of the corresponding address will be cleared after data transmission.
- If a data part reads except ACh, only data transmission will be performed and error information will not be cleared.

Please clear the error information in the IC after checking that MCU has received error status information.
As for the register map, please refer to “9.6 Register map”.
The corresponding address of this function is 1 to 4.
Please refer to the following flow charts for details.

Flow of data read-out



Typical normal termination of error status communicate mode

The contents of SPI communication	Comment
Initial value	-
01h read-out	Data: Don't carry out a data clearance except ACh.
02h read-out	01h Failbit is checked. Data: Don't carry out a data clearance except ACh.
03h read-out	02h Failbit is checked. Data: Don't carry out a data clearance except ACh.
04h read-out	03h Failbit is checked. Data: Don't carry out a data clearance except ACh. -
00h dummy transmission	04h Failbit is checked by dummy communication.
A 01h clearance	Data: It is a 01h data clearance at ACh.
A 02h clearance	Data: It is a 02h data clearance at ACh.
A 03h clearance	Data: It is a 03h data clearance at ACh.
A 04h clearance	Data: It is a 04h data clearance at ACh.

9.3.2. Data test mode

(1) Function1 (judging-data function for eight frames (one frame: 16bits))

This diagnostic function checks the data of 8 byte. For example, it can diagnose the calculation function of the MCU. As for the register map, please refer to “9.6 Register map”. Funcion1 uses the address of 05h to 0Ch. The IC has the previously-defined expected value, and it is assigned with the address.

Function1 test starts test when the data is written to the register address of 05h. If a data test starts, only 05h data is written and the data of 06h to 0Ch is cleared.

When a data test starts, please transmit data to the register address included in a data test at the young order of an address. If all the data of 05h to 0Ch are transmitted, please transmit a dummy frame, check the existence of a communication fault and, finally transmit a kick command. When the address of 13h is transmitted, the IC recognizes it as a kick command and compares the written data of 05h to 0Ch to the expected value. If both values are matched, the data test is completed. If both values are unmatched, NRSTA and NDIAG output low level and the data test is completed.

When the data test shows error and the reset is outputted from the IC (NRSTA="L") and MCU is reset, the state is initialized by clearing the SPI communicate mode.

In the case of data mismatch, the information of the test error of Function1 remains in the error status of the IC.

Management of an access history

The initial value of an access history is 00h. If the data is written to the register address of 05h before the test starts, the register address is set. Then, if the data is written to the one more register address, the object register address is set. If the data is written to other than one more register address, an address history does not change. An access history is initialized to 00h if the data is written to the register address of 13h.

Dummy frame

Please transmit the dummy frame of 00h after transmitting of the data of 05h to 0Ch is completed from MCU. The communication error of a prior communication frame can be confirmed by a Fail bit.

This data of 00h is outside object of the sequence surveillance.

Typical normal termination of data test Function1

The contents of SPI communication	Comment	Access history	Data test mode
Initial value	-	00h	0
It writes in to 05 h.	Sequence check start. 06h - 0Ch clearance.	05h	1
It writes in to 06 h.	-	06h	1
It writes in to 07 h.	-	07h	1
It writes in to 08 h.	-	08h	1
It writes in to 09 h.	-	09h	1
It writes in to 0Ah.	-	0Ah	1
It writes in to 0Bh.	-	0Bh	1
It writes in to 0Ch.	-	0Ch	1
It writes in to 00 h.	A Fail bit is checked by dummy communication.	0Ch	1
It writes in to 13 h.	The contents of data of 05h - 0Ch are judged. With no error output. SPI timeout surveillance start.	00h	0

Monitoring order of writing data (sequence surveillance)

When the data test starts, the order of writing data starts to be monitored. The monitoring conditions of the order of writing data are as follows.

A) Writing only to the register address included in the data test and that of 00h and 13h.
(Read-out is outside of object)

B) Writing to a register address younger than the access history+1.

Data is written without the notice of diagnosis, if the above-mentioned conditions are fulfilled. If the above-mentioned conditions are not fulfilled, the data is written to the register as error information. And NDIAG is outputted low level. It is common use in Function1, Function2, and Function3.

SPI timeout

The communication frame which starts SPI timeout and initializes count is the kick command 13h under Function1 test. In the initial state after startup or reset (NRSTA="L"), the monitoring function of SPI timeout is an idle state. Monitoring judging time is 100 ms. when the kick command is written, the monitoring function of SPI timeout starts. And when the gap of writing a kick command during Function1 test exceeds 100 ms, NRSTA and NDIAG outputs low level. When NRSTA is outputted low level, the monitoring function of SPI timeout is in an idle state irrespectively.

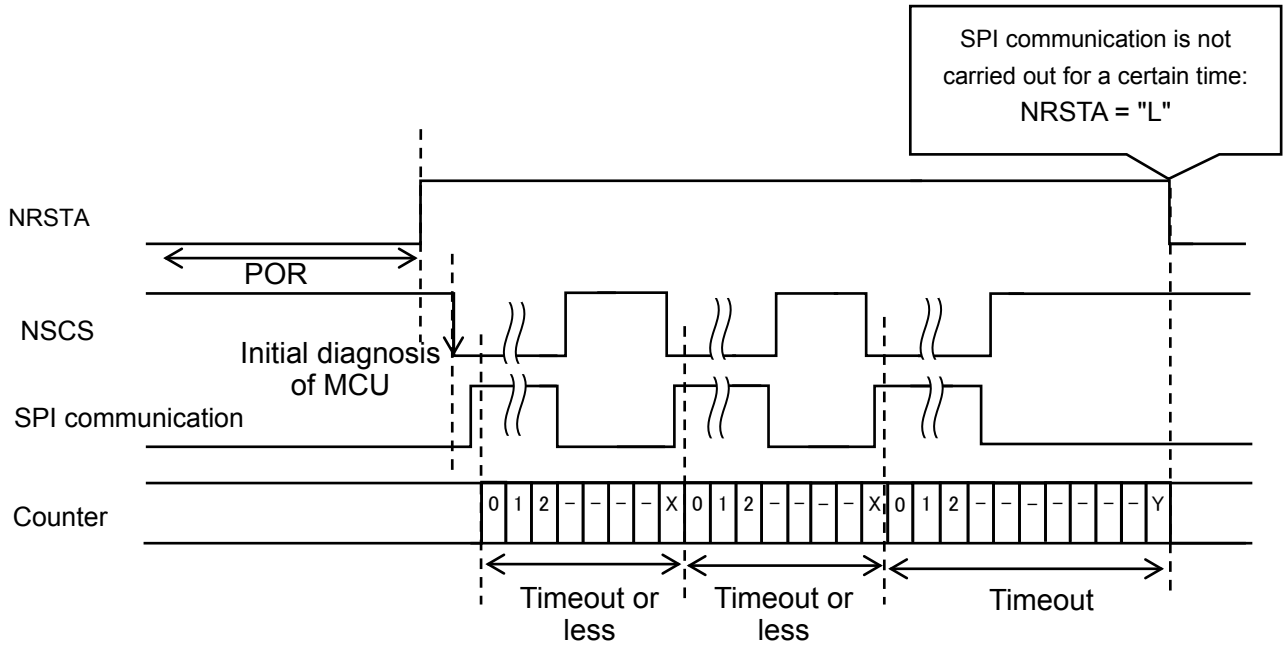
Monitoring judging time is set by a register, and it can be changed by writing to the register address 13h with SPI communication. The lower 5 bits correspond to a time setting value. Only a value which is smaller than the value before writing can be written, and it cannot change into a larger value. Moreover, a setup of the time 0 is impossible. When NRSTA is outputted low level, monitoring judging time is initialized at 100 ms irrespectively.

The relation between data of 13h and Timeout time is 5.12 ms × data. Setting 50 ms: is 5.12ms × 0Ah=51.2ms.

Initialization value: 5.12ms × 14h=102.4ms.

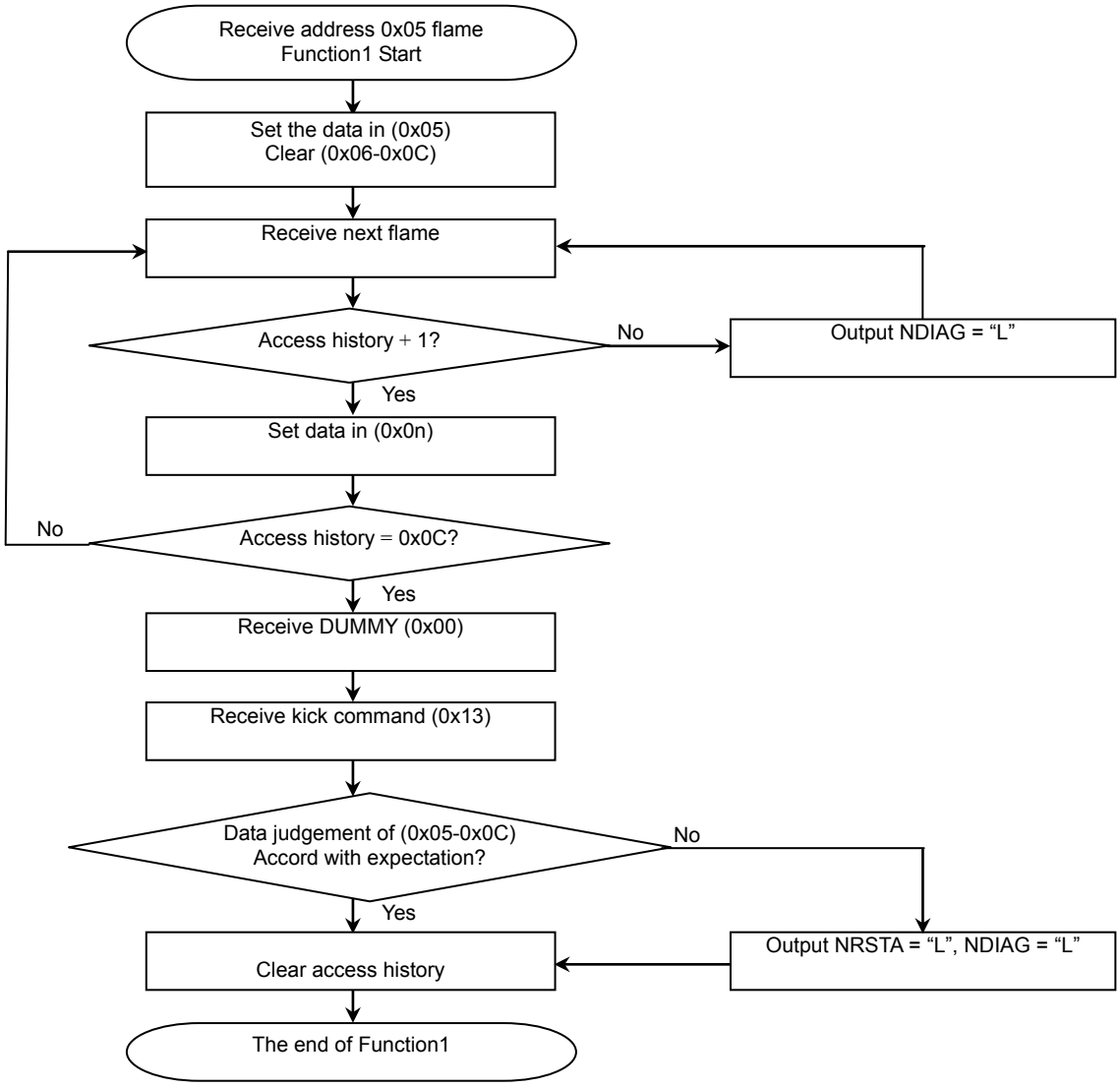
In this function, NRSTA and NDIAG output low to MCU in NG judging.

For details, please refer to “Flow of function1” in following.



Example: Communication chart of operation functional diagnosis of MCU (image figure)

The flow of Function1



(2) Function2 (judging-data function for two frames (one frame: 16bits))

This diagnostic function checks the data of 2 byte. As for the register map, please refer to "9.6 Register map". Funcion2 uses the address of 0Dh to 0Eh. The IC has the previously-defined expected value, and it is assigned with the address. For example, it can be applied for ADC diagnosis. It calculates the data of A/D conversion to the expected value by MCU, and compares and judges it by transmission to the IC.
Function2 test starts test when the data is written to the register address of 0Dh. When a data test starts, the data of 0Eh is cleared.
When a data test starts, please transmit the data of 0Eh and next transmit a dummy frame, and check the existence of a communication fault, and finally transmit a kick command of 13h. The IC compares the written data of 0Dh and 0Eh to the expected value. If both values are matched, the data test is completed. If both values are unmatched, NDIAG outputs low level and the data test is completed. Reset signal (NRSTA) does not output.
In the case of data mismatch, the information of the test error of Function2 remains in the error status of the IC.

Management of an access history

The initial value of an access history is 00h. If the data is written to the register address of 0Dh before the test starts, the register address is set. Then, if the data is written to the one more register address 0Eh, the object register address is set. If the data is written to other than one more register address, an address history does not change. An access history is initialized to 00h if the data is written to the register address of 13h.

Dummy frame

Please transmit the dummy frame of 00h after transmitting of the data of 0Dh and 0Eh is completed from MCU. The communication error of a prior communication frame can be confirmed by a Fail bit.

This data of 00h is outside object of the sequence surveillance.

Surveillance of a data write-in order (sequence surveillance)

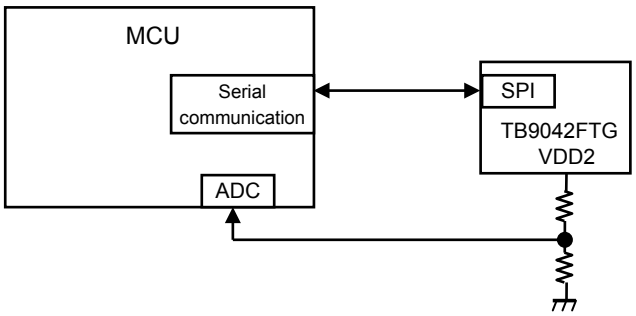
Function 2 has the same sequence monitoring function as Function1. When illegal sequence generates, it is written to the register as the error information in the IC, and NDIAG outputs low level.

Typical normal termination of data test (Function2)

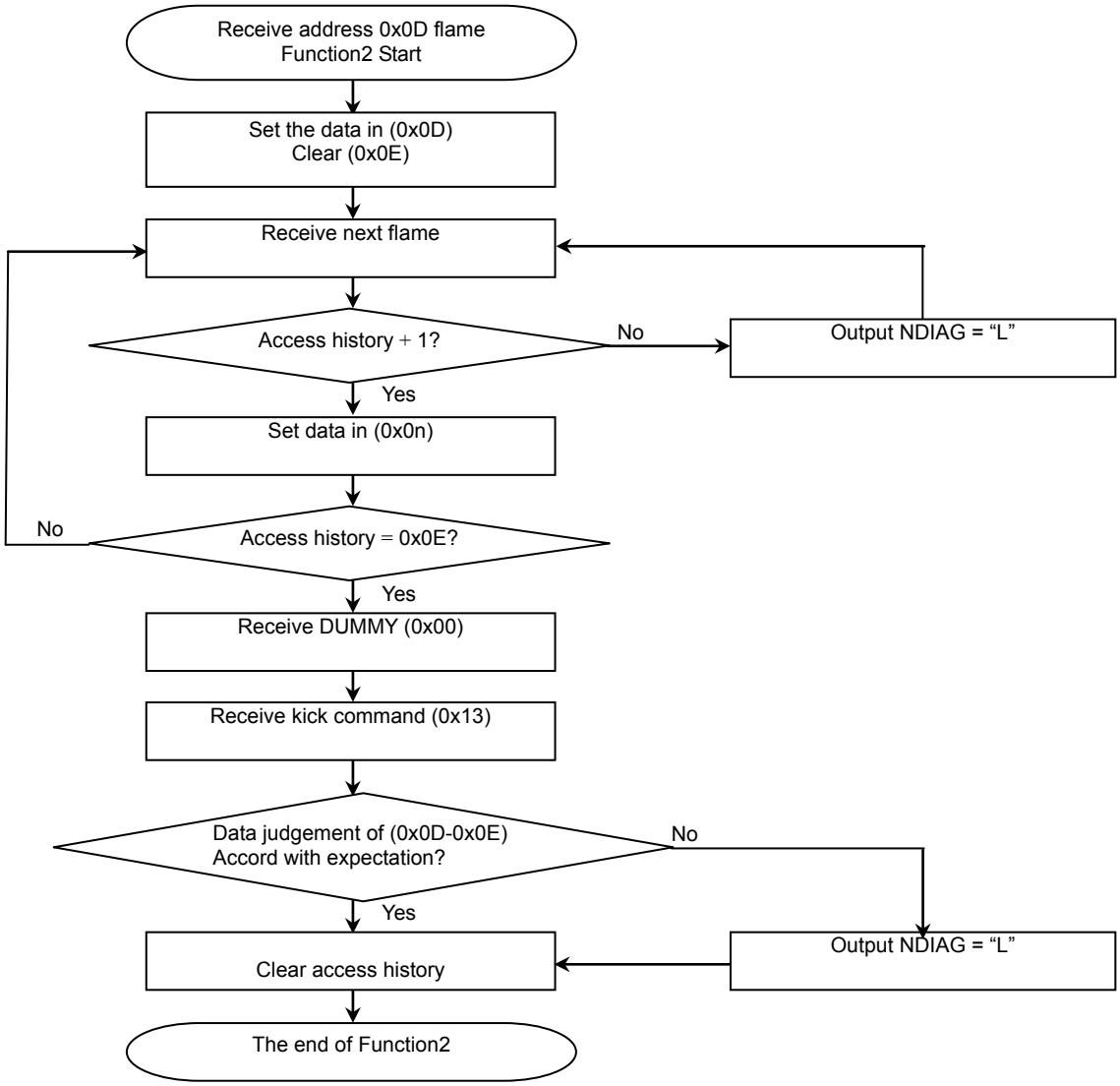
The contents of SPI communication	Comment	Access history	Data test mode
Initial value	-	00h	0
Written to 0Dh.	Sequence checks start. 0Eh clearance.	0Dh	2
Written to 0Eh.	-	0Eh	2
Written to 00 h.	A Fail bit is checked by dummy communication.	0Eh	2
Written to 13 h.	The contents of data of 0Dh and 0Eh are judged. No error output.	00h	0

For details, please refer to "Flow of function2".

Ex: ADC diagnosis



The flow of Function2



(3) Function3 (judging-data function for four frames (one frame: 16bits))

This diagnostic function checks the data of 4 byte. As for the register map, please refer to "9.6 Register map". Funcion3 uses the address of 0Fh to 12h. The IC has the previously-defined expected value, and it is assigned with the address. It calculates the data to the expected value by MCU, and compares and judges it by transmission to the IC.

Function3 test starts test when the data is written to the register address of 0Fh. When a data test starts, the data of 10h to12h are cleared.

When a data test starts, please transmit the data to the register address at the young order of an address from 10h. If all the data of 0Fh to 12h are transmitted, please transmit a dummy frame, check the existence of a communication fault, and finally, transmit a 13h kick command. When the address of 13h is transmitted, the IC compares the written data of 0Fh to 12h to the expected value. If both values are matched, the data test is completed. If both values are unmatched, NDIAG outputs low level and the data test is completed. Reset signal (NRSTA) does not output.

In the case of data mismatch, the information of the test error of Function3 remains in the error status of the IC.

Management of an access history

The initial value of an access history is 00h. If the data is written to the register address of 0Fh before the test starts, the register address is set. Then, if the data is written to the one more register address, the object register address is set. If the data is written to other than one more register address, an address history does not change. An access history is initialized to 00h if the data is written to the register address of 13h.

Dummy frame

Please transmit the dummy frame of 00h after transmitting of the data of 0Fh to 12h is completed from MCU. The communication error of a prior communication frame can be confirmed by a Fail bit.

This data of 00h is outside object of the sequence surveillance.

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Surveillance of a data write-in order (sequence surveillance)

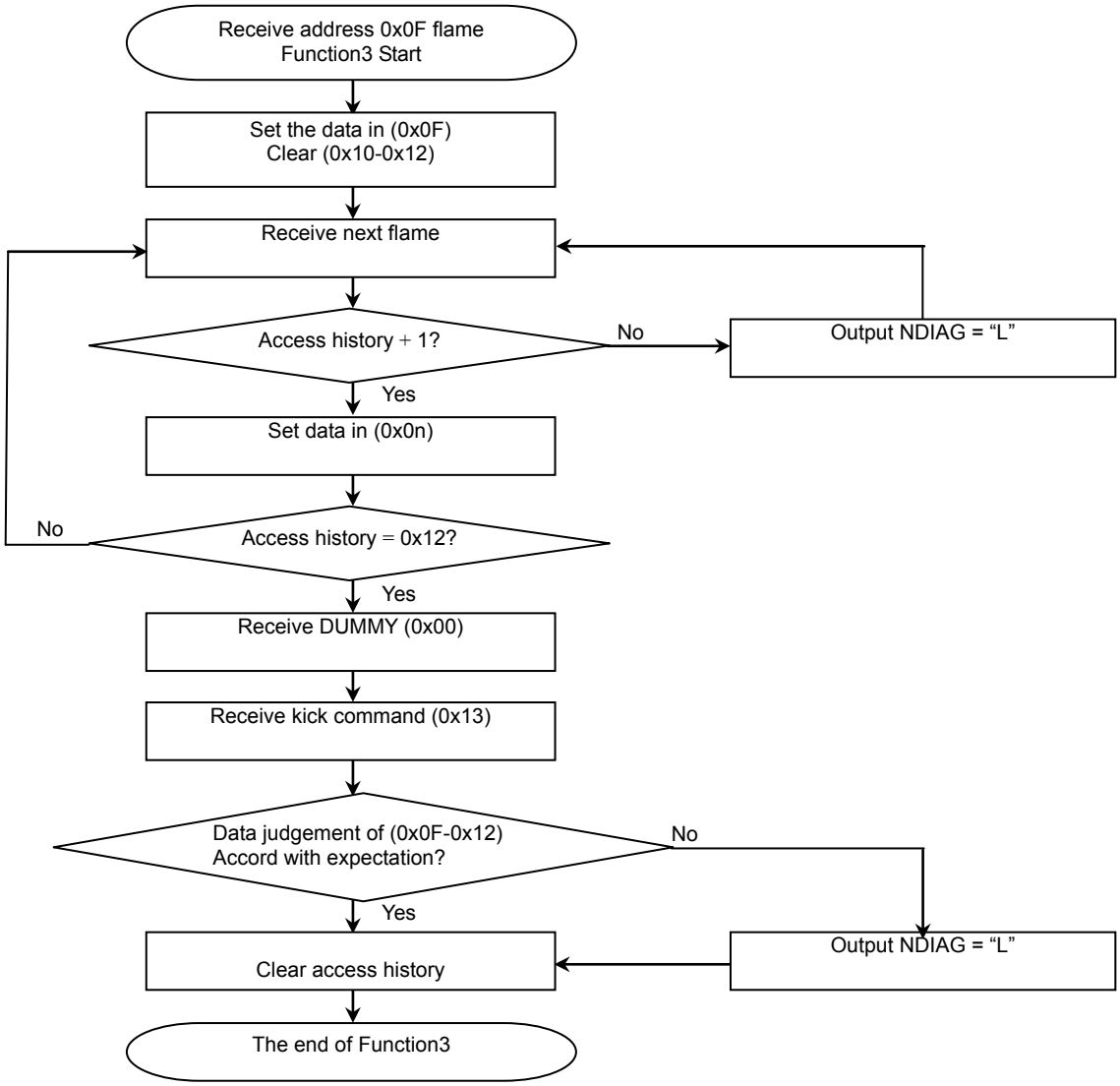
Function 3 has the same sequence monitoring function as Function1. When illegal sequence generates, it is written to the register as the error information in the IC, and NDIAG outputs low level.

Typical normal termination of data test (Function3)

The contents of SPI communication	Comment	Access history	Data test mode
Initial value	-	00h	0
Written to 0Fh.	Sequence checks start. Clear 10h - 12h.	0Fh	3
Written to 10 h.	-	10h	3
Written to 11 h.	-	11h	3
Written to 12 h.	-	12h	3
Written to 00 h.	A Fail bit is checked by dummy communication.	12h	3
Written to 13 h.	The 0Fh-12h contents of data are judged. With no error output.	00h	0

For details, please refer to "Flow of function3".

The flow of Function3



9.4. Details of communication

9.4.1. Operational mode

The operational mode is decided by "R/W" bit of SDIN and the accessed address.

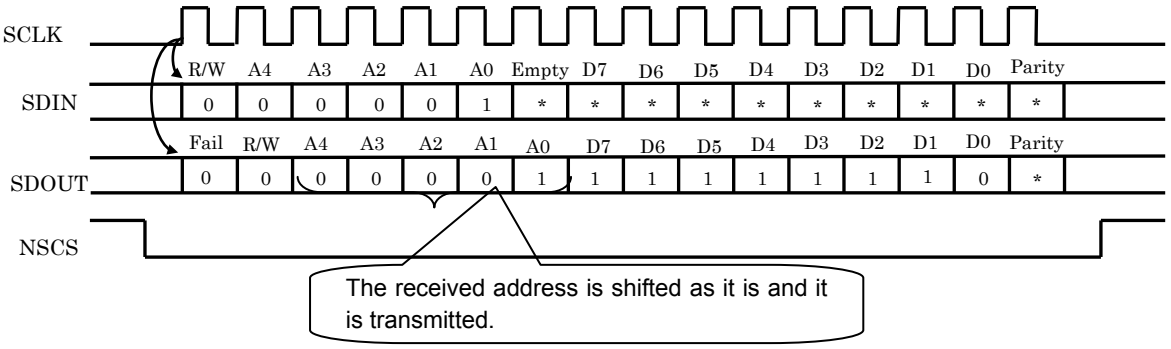
Operational mode	RW bit	Address conditions of operation
Read	0	-
Write	1	-

9.4.2. Read operation

In the read mode, the IC shifts the received address and send it as it is, and transmits henceforth the data and parity which were demanded.

From the register of the address specified by input signal A4 to A0 of SDIN, the value of a register is reed and data is outputted to D7 to D0 of SDOUT.

If the data of D7 to D0 input to SDIN is "ACh", the register data of the address is cleared. If the data is not "ACh", the register data of the address is not cleared.

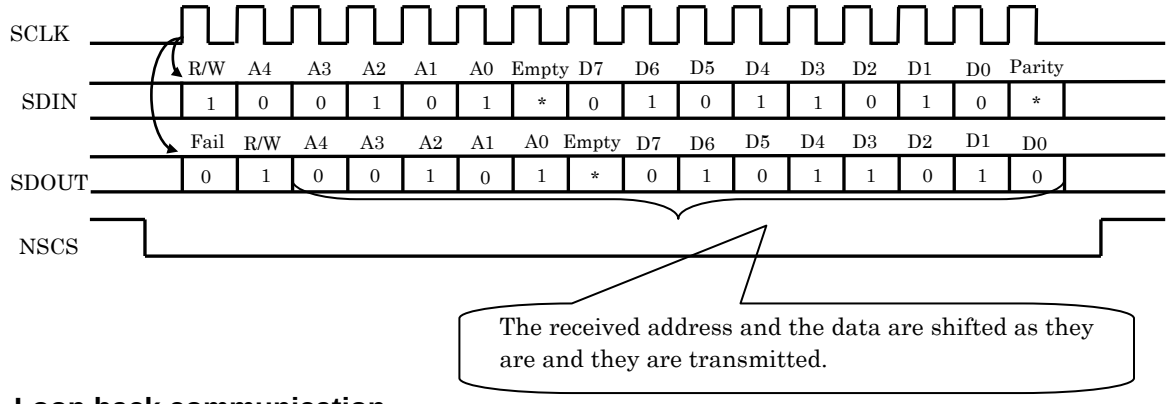


9.4.3. Write operation

In the write mode, the received data is shifted as it is, and is transmitted.

The IC writes the data of SDIN D7 to D0 to the register of the address specified by input signal A4 to A0 of SDIN.

Please refer to following figure.



9.4.4. Loop back communication

Loop back communication means the operation that the IC shifts and transmits the received data/address to the MCU, as described in "9.4.2.Read operation" and "9.4.3.Write operation".

Please check the communication path and the transmission content by using this function.

9.4.5. About NSCS at operating communication

As shown in the next page, "The timing chart figure of Fail judging", please do the communication in the NSCS = "L" for each frame.

9.4.6. Failure judging

In the below cases, the communication is judged as error, and then the Fail bit is set to "1" in the next communication. In addition, the IC writes the data to the error status register and outputs NDIAG = "L" when the transmission of the error occurred frame is finished...

This operation is common to read operation and write operation (Function 1-3).

- In the case of. one frame is other than 16 bits

(Also the case where transmitting frames are 17 bit and 15 bit, and in 8 bit x 2, it is judged as an error.)

In receiving, if the communication number of clocks during the NSCS = "L" is other than 16, it is judged as framing error, the IC invalidates the received data. When a framing error and a communication fault occur, it sets the Fail bit to 1 in the following frame and transmits it. In transmitting, in the write mode, the received data is shifted as it is, and it is transmitted. In the read mode, the received address is shifted as it is, and it is transmitted. Henceforth the IC transmits the data and the parity which were demanded.

When the clock over regulation is inputted during NSCS ="L", 1 is outputted to the bit over regulation.

- In the case of a parity check error

The empty bit is also included in a parity account.

Parity = R/W ⊕ A4 ⊕ A3 ⊕ A2 ⊕ A1 ⊕ A0 ⊕ Empty ⊕ D7 ⊕ D6 ⊕ D5 ⊕ D4 ⊕ D3 ⊕ D2 ⊕ D1 ⊕ D0

For example, when it becomes a communication fault (parity error) with the frame which transmitted in reference-data test mode, the IC ignores the frame.

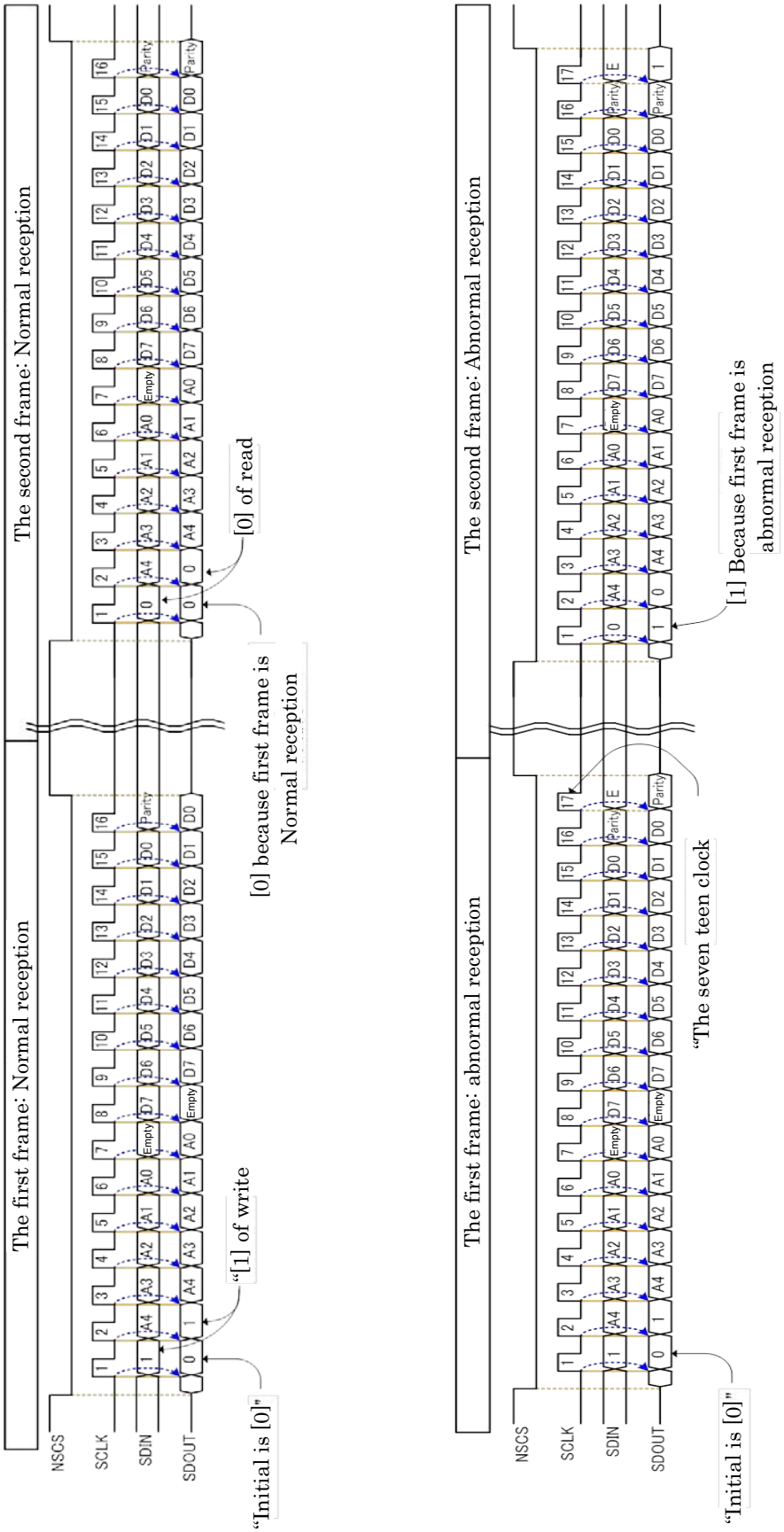
It does not determined to be normal as long as it does not resume from the frame that caused the communication error due to the status that the frame is ignored and not received.

For example, when the framing error of the 3rd frame occurs, the IC ignores the 3rd frame, so please resend the 3rd frame from MCU.

Please refer to the following clause -- "The timing chart figure of Failure judging".

The timing chart figure of Failure judging

The following figure shows the operation when this IC has received the frame over 16bit.



9.5. Communications department AC characteristics

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125℃.
And DC2IN = LDO1IN = LDO2IN = 5.8 to 6.2V unless otherwise the follows.

Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
SPI transmission rate	$RATE_{SPI}$	SCLK, SDIN	-	-	-	4	Mbps
SPI clock period	t_{CYCL}	NSCS, SCLK, SDIN, SDOUT	-	250	-	-	ns
Settling Time	t_{SETL}			200	-	-	
Enable Lag Time	t_{SETH}			100	-	-	
Transfer Inactive Time	t_{CSH}			1500	-	-	
Data Valid Time	t_{DOUT}			-	-	80	
Delay time 1	t_{DZ1}			-	-	100	
Delay time 2	t_{DZ2}					100	
Data set up time	t_{DIS}			50	-	-	
Data hold time	t_{DIH}			50	-	-	
Duty	DUTY	SCLK	-	40	-	60	%

The AC wave form is shown at Figure1.

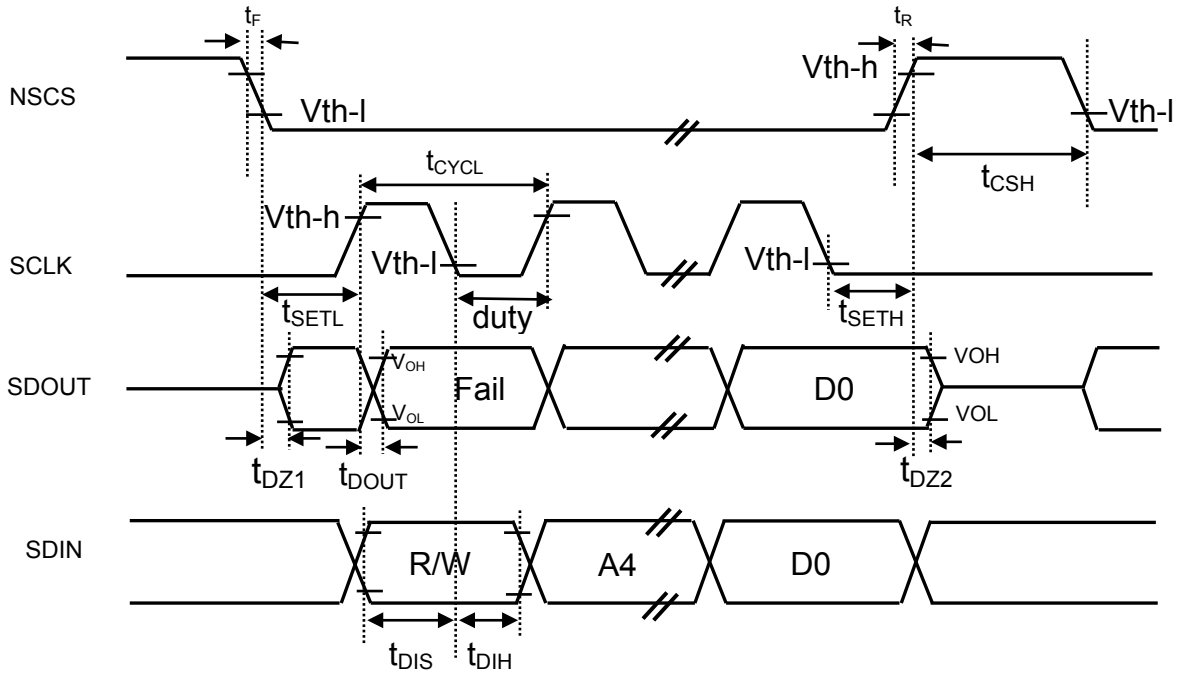


Figure1 SPI block AC wave

9.6. Register map

Address	Register
0x01 to 0x04	ESC0 to ESC3: Error status communicate mode "Error Status Comunication0" to "Error Status Comunication3"
0x05 to 0x0c	F1FRD0 to F1FRD7: Data test mode Function1 "Function1 Reference Data0" to "Function1 Reference Data7"
0x0d to 0x0e	F2FRD0 to F2FRD1: Data test mode Function2 "Function2 Reference Data0" to "Function2 Reference Data1"
0x0f to 0x12	F3FRD0 to F3FRD3: Data test mode Function3 "Function3 Reference Data0" to "Function3 Reference Data3"

<<Error status communicate mode>>

The bit that error occurred is set to 1. For getting various error status information, please refer to "10.2 The contents of error information".

"Error Status Comunication0"

Register name (Address)	bit	7	6	5	4	3	2	1	0
ESC0 (0x01)	Name	LDO1IDET	LDO1LV	LDO1HV	DC2IDET	DC2LV	DC2HV	DC1IDET	DC1HV
	Type	Read							
	Initial value	0	0	0	0	0	0	0	0

"Error Status Comunication1"

Register name (Address)	bit	7	6	5	4	3	2	1	0
ESC1 (0x02)	Name	TSD2	TSD1	VBUIDET	VBULV	VBUHV	LDO2IDET	LDO2LV	LDO2HV
	Type	Read							
	Initial value	0	0	0	0	0	0	0	0

"Error Status Comunication2"

Register name (Address)	bit	7	6	5	4	3	2	1	0
ESC2 (0x03)	Name	FUNC2	FUNC3	MCUALM1	WDTB	WDTA	NDIAG	DIAG	OSC
	Type	Read							
	Initial value	0	0	0	0	0	0	0	0

"Error Status Comunication3"

Register name (Address)	bit	7	6	5	4	3	2	1	0
ESC3 (0x04)	Name	-	-	-	SPIER	SEQ	MCUALM2	SPITO	FUNC1
	Type	Read							
	Initial value	0	0	0	0	0	0	0	0

<<Data test mode Function1>>

"Function1 Reference Data0" (it is set as 233 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD0 (0x05)	Name	Data1-7	Data1-6	Data1-5	Data1-4	Data1-3	Data1-2	Data1-1	Data1-0
	Type	Read/Write							
	Judging value	1	1	1	0	1	0	0	1
	Initial value	1	1	1	0	1	0	0	1

"Function1 Reference Data1" (it is set as 229 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD1 (0x06)	Name	Data1-15	Data1-14	Data1-13	Data1-12	Data1-11	Data1-10	Data1-9	Data1-8
	Type	Read/Write							
	Judging value	1	1	1	0	0	1	0	1
	Initial value	1	1	1	0	0	1	0	1

"Function1 Reference Data2" (it is set as 227 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD2 (0x07)	Name	Data1-23	Data1-22	Data1-21	Data1-20	Data1-19	Data1-18	Data1-17	Data1-16
	Type	Read/Write							
	Judging value	1	1	1	0	0	0	1	1
	Initial value	1	1	1	0	0	0	1	1

"Function1 Reference Data3" (it is set as 211 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD3 (0x08)	Name	Data1-31	Data1-30	Data1-29	Data1-28	Data1-27	Data1-26	Data1-25	Data1-24
	Type	Read/Write							
	Judging value	1	1	0	1	0	0	1	1
	Initial value	1	1	0	1	0	0	1	1

"Function1 Reference Data4" (it is set as 199 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD4 (0x09)	Name	Data2-7	Data2-6	Data2-5	Data2-4	Data2-3	Data2-2	Data2-1	Data2-0
	Type	Read/Write							
	Judging value	1	1	0	1	0	0	1	1
	Initial value	1	1	0	1	0	0	1	1

"Function1 Reference Data5" (it is set as 197 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD5 (0x0a)	Name	Data2-15	Data2-14	Data2-13	Data2-12	Data2-11	Data2-10	Data2-9	Data2-8
	Type	Read/Write							
	Judging value	1	1	0	0	0	1	0	1
	Initial value	1	1	0	0	0	1	0	1

"Function1 Reference Data6" (it is set as 193 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD6 (0x0b)	Name	Data2-23	Data2-22	Data2-21	Data2-20	Data2-19	Data2-18	Data2-17	Data2-16
	Type	Read/Write							
	Judging value	1	1	0	0	0	0	0	1
	Initial value	1	1	0	0	0	0	0	1

"Function1 Reference Data7" (it is set as 181 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F1FRD7 (0x0c)	Name	Data2-31	Data2-30	Data2-29	Data2-28	Data2-27	Data2-26	Data2-25	Data2-24
	Type	Read/Write							
	Judging value	1	0	1	1	0	1	0	1
	Initial value	1	0	1	1	0	1	0	1

<<Data test mode Function2>>

"Function2 Reference Data0" (it is set as 179 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F2FRD0 (0x0d)	Name	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	Type	Read/Write							
	Judging value	1	0	1	1	0	0	1	1
	Initial value	1	0	1	1	0	0	1	1

"Function2 Reference Data1" (it is set as 173 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F2FRD1 (0x0e)	Name	ADC15	ADC14	ADC13	ADC12	ADC11	ADC10	ADC9	ADC8
	Type	Read/Write							
	Judging value	1	0	1	0	1	1	0	1
	Initial value	1	0	1	0	1	1	0	1

<<Data test mode Function3>>

"Function3 Reference Data0" (it is set as 167 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F3FRD0 (0x0f)	Name	Fdata-7	Fdata-6	Fdata-5	Fdata-4	Fdata-3	Fdata-2	Fdata-1	Fdata-0
	Type	Read/Write							
	Judging value	1	0	1	0	0	1	1	1
	Initial value	1	0	1	0	0	1	1	1

"Function3 Reference Data1" (it is set as 163 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F3FRD1 (0x10)	Name	Fdata-15	Fdata-14	Fdata-13	Fdata-12	Fdata-11	Fdata-10	Fdata-9	Fdata-8
	Type	Read/Write							
	Judging value	1	0	1	0	0	0	1	1
	Initial value	1	0	1	0	0	0	1	1

"Function3 Reference Data2" (it is set as 157 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F3FRD2 (0x11)	Name	Fdata-23	Fdata-22	Fdata-21	Fdata-20	Fdata-19	Fdata-18	Fdata-17	Fdata-16
	Type	Read/Write							
	Judging value	1	0	0	1	1	1	0	1
	Initial value	1	0	0	1	1	1	0	1

"Function3 Reference Data3" (it is set as 151 with a prime number)

Register name (Address)	bit	7	6	5	4	3	2	1	0
F3FRD3 (0x12)	Name	Fdata-31	Fdata-30	Fdata-29	Fdata-28	Fdata-27	Fdata-26	Fdata-25	Fdata-24
	Type	Read/Write							
	Judging value	1	0	0	1	0	1	1	1
	Initial value	1	0	0	1	0	1	1	1

<<Data test mode KICK command>>

"Function1 Timeout Data"

Register name (Address)	bit	7	6	5	4	3	2	1	0
KICKR (0x13)	Name	-	-	-	SPITO4	SPITO3	SPITO2	SPITO1	SPITO0
	Type	Read/Write							
	Initial value	-	-	-	1	0	1	0	0

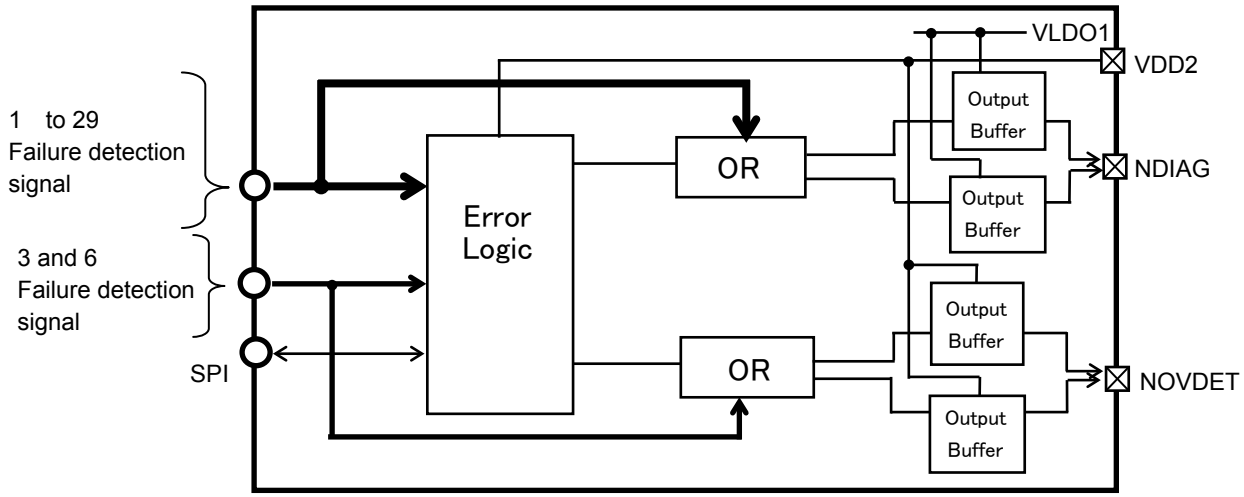
10. Error logic

10.1. About the function of error logic

When the monitoring result of the failure of the power supply IC or the MCU is NG, which are shown in "10.2 . The contents of error information", “L" is output from NDIAG terminal. At the same time, this IC writes the abnormal data in the register provided at SPI.

To avoid the "H" sticking of NDIAG by destruction of the output buffer, the output of NDIAG is duplicated. By either the one buffer operating correctly, it is possible to output the NDIAG = "L" at the abnormality occurrence.

To avoid the "H" sticking of NOVDET by destruction of the output buffer, the output of NOVDET is duplicated. By either the one buffer operating correctly, it is possible to output the NOVDET = "L" at the abnormality occurrence.



10.2. The contents of error information

The items which are the objects of error information are shown in Table1.It includes the control & outputting operation when abnormalities are detected by each item. The items without the explanation perform only the writing to the NDIAG output and the error information to the register.

The applicable items of the self-diagnostics performed during power-on reset is written by O.

Table1 Error information judging item list

No	Symbol	Item	Control & outputting operation of power supply IC	Self-diagnostics Applicable item
1	DC1HV	DCDC1 High-voltage	-	O
2	DC1IDET	DCDC1 Overcurrent	Overcurrent control of DC1	-
3	DC2HV	DCDC2 High-voltage	NOVDET signal output	O
4	DC2LV	DCDC2 Low-voltage	Reset A&B output	O
5	DC2IDET	DCDC2 Overcurrent	Overcurrent control of DC2	-
6	LDO1HV	LDO1 High-voltage	NOVDET signal output	O
7	LDO1LV	LDO1 Low-voltage	Reset A&B output	O
8	LDO1IDET	LDO1 Overcurrent	Overcurrent control of DC2	-
9	LDO2HV	LDO2 High-voltage	-	O
10	LDO2LV	LDO2 Low-voltage	-	O
11	LDO2IDET	LDO2 Overcurrent	Overcurrent control of DC2	-
12	VBUHV	VBU High-voltage	-	O
13	VBULV	VBU Low-voltage	-	O
14	VBUIDET	VBU overcurrent	Overcurrent control of DC2	-
15	TSD1	Overheating detection 1	Power supply output all OFF	-
16	TSD2	Overheating detection 2	Power supply output all OFF	-
17	OSC	OSC diagnosis	-	-
18	DIAG	Self-diagnostics	NOVDET signal output	O
19	NDIAG	NDIAG H/L operation	-	O
20	WDTA	WDTA detection	Reset A output	O
21	WDTB	WDTB detection	Reset B output	O
22	MCUALM1	MCU diagnostic critical fault	NOALM output	O
23	FUNC3	Function3	-	-
24	FUNC2	Function2	-	-
25	FUNC1	Function1	Reset A output	-
26	SPITO	SPI timeout	Reset A output	-
27	MCUALM2	The abnormalities in a logic checking circuit of MCUALM	-	-
28	SEQ	SPI sequence surveillance	-	-
29	SPIER	SPI communication Fail	-	-
30	-	-	-	-

11. Clock oscillation function

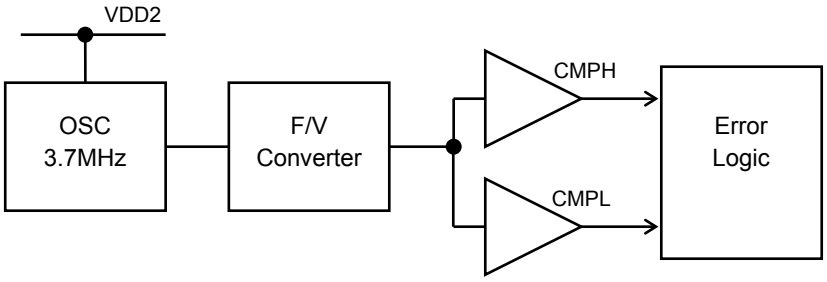
11.1. Oscillating circuit built-in

- C and R are built in with the C/R oscillator. Oscillated frequency is 3.7MHz±0.7MHz.
- It is used for switching of a DCDC converter, the clock of logic, etc.
- The detector which outputs a DIAG signal at the time of the abnormalities of oscillated frequency is built in.

11.2. Frequency monitoring function

The abnormalities of high frequency and low frequency are detected with analog-type a F/V converter and a voltage comparator.

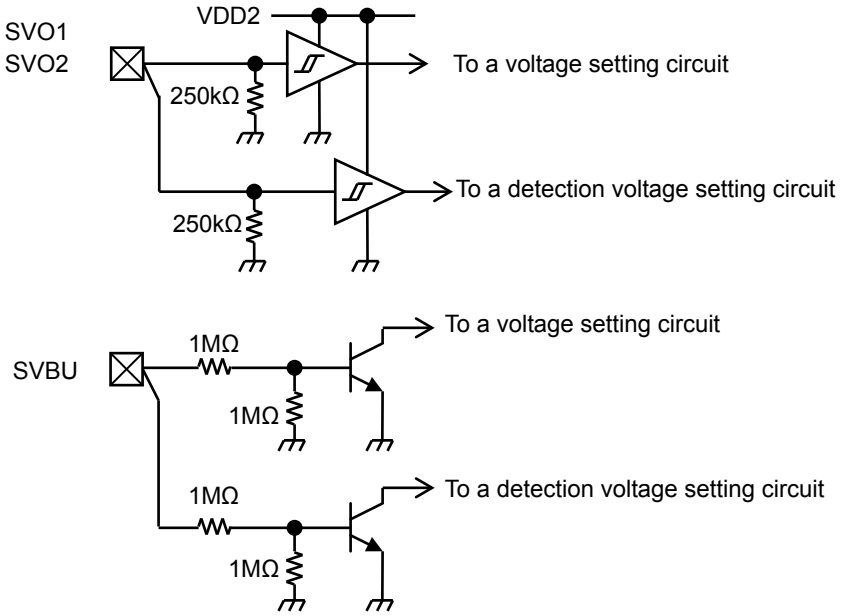
Functional block is shown below.



12. Mode setting input processing

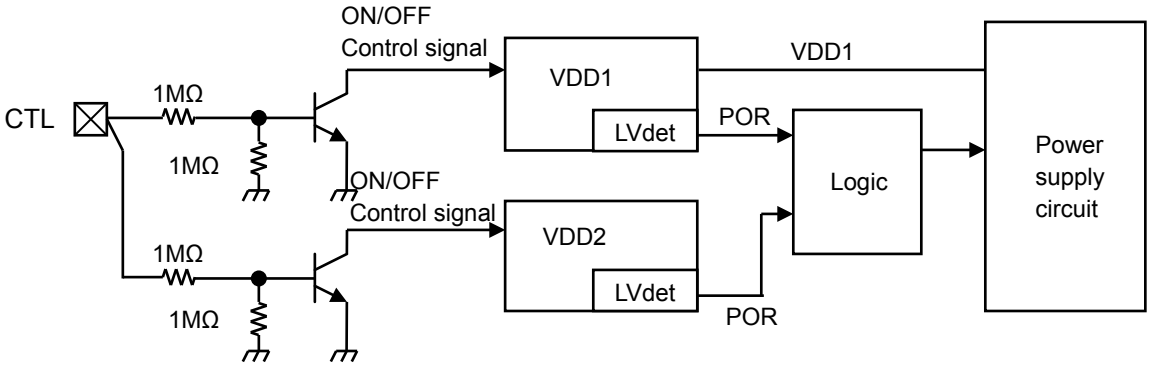
12.1. DCDC2, VBU voltage selection

To avoid that the detection voltage setting becomes abnormal (which is set to a different value from the set one) when the voltage setting circuit shows abnormality , as shown in "7. Signal input-output-terminals equivalent circuit", the detection value setting circuit and the voltage setting circuit are separated from the base of the terminal, SVO1, SVO2 or SVBU.



12.2. Power supply ON/OFF control

ON/OFF of a power supply function is controlled from CTL1.
The condition that the power supply operates is to set VDD1 to "ON" and the POR released, and to set VDD2 to "ON" and the POR released. ON / OFF control signal has two separated routes from the CTL1 pin, and each one ensure independence.



13. Internal electrical power source

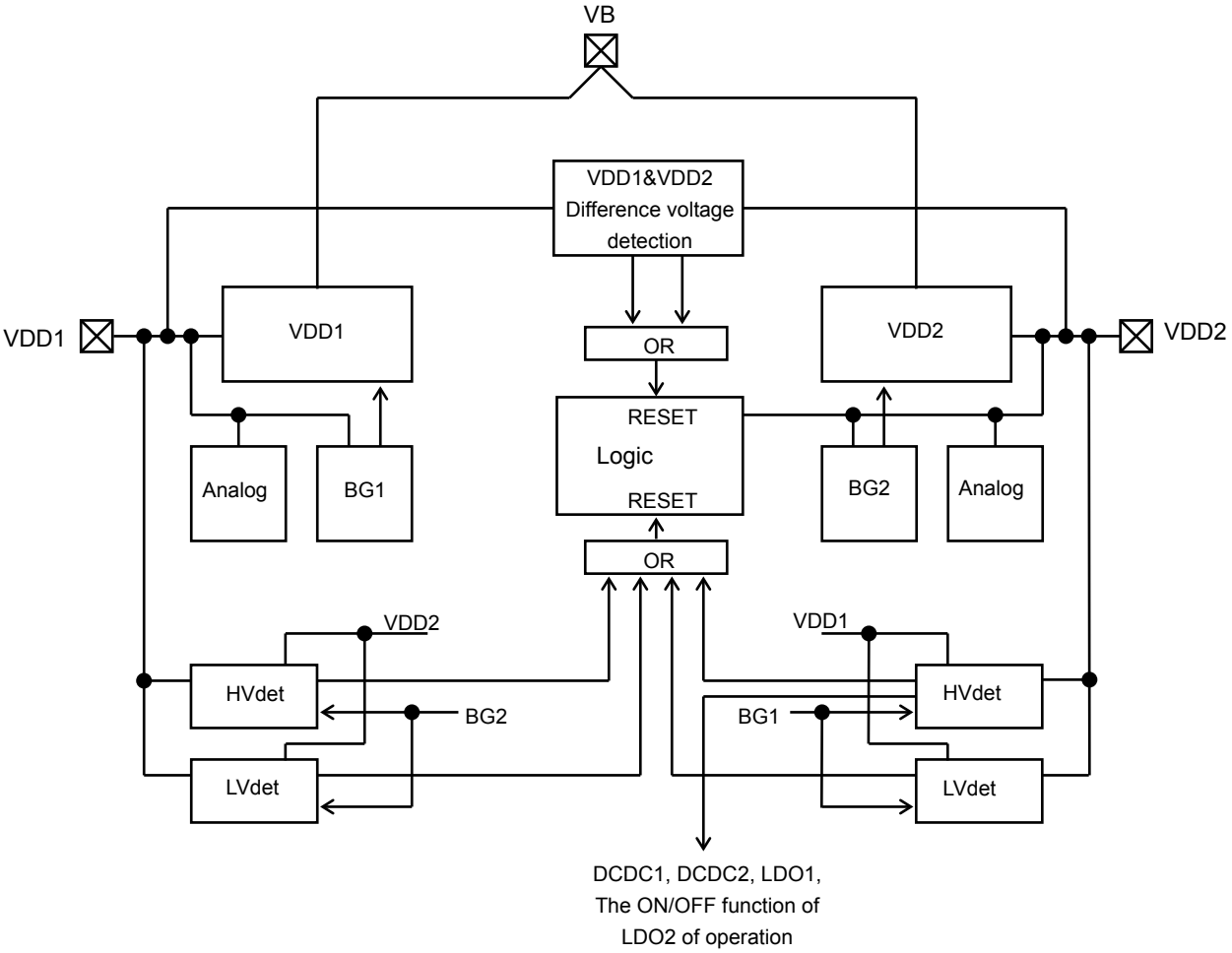
Two 5V power supplies for insides are built-in.

VDD1 is used for the control of the power supply output, and VDD2 is used for various monitor system circuits and logic. The voltage monitoring of the low-voltage & high-voltage is built in each power supply, and reset the logic circuit at the detection of a voltage abnormality.

Detection voltage and a circuit block are shown below. .

When big voltage difference occurs between VDD1 and VDD2, the IC resets the logic circuit.

	Min	Typ.	Max
High-voltage detection	5.5V	5.75V	6.0V
Low-voltage detection (POR)	3.8V	4.0V	4.2V
VDD1-VDD2 Difference voltage detection	0.4V	1.0V	1.5V



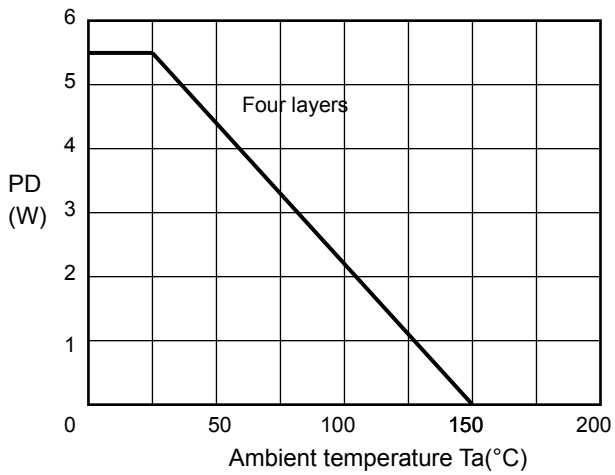
14. **Absolute maximum rating (Ta=25℃)**

Characteristics	Symbol	Pin	Rating	Unit
Input voltage	V_{IN1}	VB, CTL1, CTL2	-0.3 to 20.1 (DC)	V
			20.1 to 30 (60s)	
			30 to 40 (1s)	
	V_{IN2}	DC1SW, DC2IN, DC2R, DC2G, LDO1IN, LDO2IN, DC1CP	V_B	
	V_{IN3}	SVO1, SVO2, SEW, SLDO2, TEST	V_{DD2}	
	V_{IN4}	CKA, CKB, WSA, WSB, INALM0, INALM1, SDIN, SCLK, NSCS	V_{LDO1}	
	V_{IN5}	SVBU	V_{BU5}, V_{BU3}	
Output current	I_{OUT1}	DC1SW	±1000	mA
	I_{OUT2}	LDO1OUT	-400	
	I_{OUT3}	LDO2OUT	-100	
	I_{OUT4}	NRSTA, NRSTB, NOVDET, NDIAG, NOALM	+10	
Output voltage	V_{OUT}	NRSTA, NRSTB, NOVDET, NDIAG, NOALM, VDD2, LDO1OUT, VBU	5.5	V
Power dissipation	P_D	-	(NOTE)	W
Operating temperature	Topr	-	-40 to 125	°C
Storage temperature	Tstg	-	-55 to 150	°C

Notes: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. If an absolute maximum rating is exceeded, it will become a cause of destruction and degradation of IC, or damage, and there is a possibility give a damage to other components other than the IC. Please design not to exceed an absolute maximum rating on any operating conditions. When using it, please use it in the indicated operating range.

NOTE:

HVQFN52 PD curve



Board size
76.2x114.3x1.6 mm
Soldering to a substrate: Yes.

15. Electrical Characteristics

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125℃. unless otherwise the follows

Characteristics	Symbol	Pin	Test Condition	Min	typ.	Max	Unit
DC characteristics							
Stop current	I_{CC-OFF}	VB	Stop mode CTL1=CTL2=L	-	0	-	μA
Standby current (Note 1)	I_{CC-STB}	VB	Standby mode CTL1=L and CTL2=VB (13.5V) SVBU=VBU	-	-	250	μA
DCDC1 power supply							
Output voltage	V_{DC1}	DC1FB	VB=7 to 20.1V	-	6.0	-	V
Switching Frequency	f_{SW}	-		300	370	440	kHz
Slow start Time	t_{SS}	DC1FB	DC1Css = 0.1μF	2.5	5.0	-	ms
Load regulation	V_{LOAD}	DC1FB	VDC1IN=12V I_{LOAD}=10mA to 1A	-	0.2	1.0	%
Overcurrent detection value	I_{DET-1}	-		-	2.5	-	A
	I_{DET-2}	-		-	2.5	-	
DCDC2 power supply							
Output voltage	V_{DC2}	DC2FB	SVO1=H, SVO2=L	1.47	1.5	1.53	V
			SVO1=L, SVO2=H	1.17	1.2	1.23	
Switching Frequency	f_{SW}	-		300	370	440	kHz
Slow start Time	t_{SS}	DC2FB	DC2Css = 0.1μF	2.5	5	-	ms
Load regulation	V_{LOAD}	DC2FB	VDC2IN=6V I_{LOAD}=10mA to 1A	-	0.2	1.0	%
Temperature coefficient	-	DC2FB		-	0.01	-	% /°C
Overcurrent detection voltage	V_{DET-1}	DC2R		-	0.15	-	V
	V_{DET-2}			-	0.15	-	
LDO1							
Output voltage	V_{LDO1}	LDO1OUT		4.9	5.0	5.1	V
Input stability	V_{LINE}	LDO1OUT	VLDO1IN=5.8 to 6.2V I_{LOAD1}=300mA	-	0.1	0.2	%
Load regulation	V_{LOAD}	LDO1OUT	VLDO1IN=6V I_{LOAD1}=1 to 400mA	-	0.2	1.0	%
Temperature coefficient	-	LDO1OUT		-	0.01	-	% /°C
Current limiting	I_{LMT1}	LDO1OUT		-	800	-	mA
	I_{LMT2}			-	1200	-	

Note1. In the value of ICC-STB (standby current), the input current of CTL2 and SVBU is included.

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125 ℃. unless otherwise the follows

Characteristics	Symbol	Pin	Test Condition	Min	typ.	Max	Unit
LDO2							
Output voltage	V_{LDO2}	LDO2OUT	SLDO2=H	4.9	5.0	5.1	V
Voltage difference	V_{LDO2-1}	LDO2OUT LDO1OUT	SLDO2=L	-10	0	10	mV
Input stability	V_{LINE}	LDO2OUT	VLDO2IN=5.8 to 6.2V I_{LOAD2}=70mA	-	0.1	0.2	%
Load regulation	V_{LOAD}	LDO2OUT	VLDO2IN=6V I_{LOAD2}=1 to 100mA	-	0.2	1.0	%
Temperature coefficient	-	LDO2OUT		-	0.01	-	% /°C
Current limiting	I_{LMT1}	LDO2OUT		-	200	-	mA
	I_{LMT2}			-	300	-	
VBU							
Output voltage	V_{BU5}	VBU	SVBU=VBU	4.85	5.0	5.15	V
	V_{BU3}		SVBU=GND	3.2	3.3	3.4	
Input stability	V_{LINE}	VBU	VB=6 to 40V	-	-	20	mV
Load regulation	V_{LOAD}	VBU	I_{LOAD}=1 to 10mA	-	-	10	mV
Temperature coefficient	-	VBU		-	0.01	-	% /°C
Current limiting 1	$I_{LMTBU-1}$	VBU		-	20	-	mA
Current limiting 2	$I_{LMTBU-2}$	VBU		-	40	-	mA
RESET TIMER DC characteristic							
Output voltage	V_{OL}	NRSTA, NRSTB	I_{OL}=2mA	-	-	0.3	V
Output leakage current	I_{LEAK}		V_{IN}=V_{LDO1}	-	-	5	μA
Pull-up resistor	R_{RST}			-	10	-	kΩ
Input current	I_{IN}	TCA,TCB		-13	-10	-7	μA
Discharge resistance	R_{DIS}			-	1	-	kΩ
Threshold voltage	V_{IH}			3.75	4	4.25	V
	V_{IL}			1.8	2	2.2	
Input current	I_{IH}	CKA, CKB, WSA, WSB,	V_{IN}=V_{LDO1}	10	20	40	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}			0.8xV_{LDO1}	-	-	V
	V_{IL}			-	-	0.2xV_{LDO1}	
Input current	I_{IH}	SEW	V_{IN}=V_{DD2}	9	17	34	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}			2	-	-	V
	V_{IL}			-	-	0.5	
Low holding voltage	V_{RL}	NRSTA, NRSTB		-	-	1.5	V

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125℃. unless otherwise the follows

Characteristics	Symbol	Pin	Test Condition	Min	typ.	Max	Unit
RESET TIMER AC characteristics							
Power-on reset	t_{POR}	NRSTA, NRSTB		280xC_T	400xC_T	520xC_T	ms
Watchdog-S	t_{WD-S}			140xC_T	200xC_T	260xC_T	
Watchdog-FW	t_{WD-FW}			0.7	1.0	1.3	ms
Watchdog-FD	t_{WD-FD}			7	10	13	ms
Reset timer-S	t_{RST-S}			0.3xC_T	0.7xC_T	1.5xC_T	ms
Reset timer-F	t_{RST-F}			0.7	1.0	1.3	ms
Reset timer- CO	t_{RST-CO}			0.7	1.0	1.3	ms
Clock pulse width	t_W	CKA, CKB		1	-	-	μs
POR maximum-settings time	t_{POR-CO}	NRSTA, NRSTB		176	220	264	ms
WD maximum-settings time	t_{WD-CO}			88	110	132	ms
Supply voltage surveillance							
High-voltage detection	VhTH6	DC1FB	Detection	6.3	6.6	6.9	V
	VhTH6(-)		Release	-	6.5	-	
	dVhTH6		VhTH6-VDC1	0.4	0.6	0.8	
	Vhhys6		VhTH6-VhTH6(-)	-	0.1	-	
	VhTH1.5	DC2FB	Detection	1.58	1.61	1.642	V
	VhTH1.5(-)		Release	-	1.58	-	
	dVhTH1.5		VhTH1.5-VDC2-1.5	0.05	0.11	0.15	
	Vhhys1.5		VhTH1.5-VhTH1.5(-)	-	0.03	-	
	VhTH1.2	DC2FB	Detection	1.245	1.27	1.295	V
	VhTH1.2(-)		Release	-	1.24	-	
	dVhTH1.2		VhTH1.2-VDC2-1.2	0.05	0.07	0.15	
	Vhhys1.2		VhTH1.2-VhTH1.2(-)	-	0.03	-	
	VhTH5	LDO1OUT	Detection	5.2	5.3	5.4	V
	VhTH5(-)		Release	-	5.2	-	
	dVhTH5		VhTH5-VLDO1	0.25	0.30	0.35	
	Vhhys5		VhTH5-VhTH5(-)	-	0.10	-	
	VhTHL2	LDO2OUT	Detection	5.2	5.3	5.4	V
	VhTHL2(-)		Release	-	5.2	-	
	dVhTHL2		VhTHL2-VLDO2	0.25	0.30	0.35	
	VhhysL2		VhTHL2-VhTHL2(-)	-	0.10	-	
	VhTHB5	VBU	Detection	5.15	5.3	5.45	V
	VhTHB5(-)		Release	-	5.2	-	
	dVhTHB5		VhTHB5-VBU5	0.2	0.3	0.4	
	VhhysB5		VhTHB5-VhTH5(-)	-	0.10	-	
	VhTHB3	VBU	Detection	3.4	3.5	3.6	V
	VhTHB3(-)		Release	-	3.45	-	
	dVhTHB3		VhTHB3-VBU3	0.1	0.2	0.3	
	VhhysB3		VhTHB3-VhTH3(-)	-	0.05	-	

The specification of power-on reset, a watchdog timer, and a reset timer are the value of the IC only, please be aware that the variation in CT is not included.

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125℃. unless otherwise the follows

Characteristics	Symbol	Pin	Test Condition	Min	typ.	Max	Unit
Supply voltage surveillance							
Low-voltage detection	VTH1.5	DC2FB	Detection	1.36	1.39	1.42	V
	VTH1.5(+)		Release	-	1.42	-	
	dVTH1.5		VDC2-1.5-VTH1.5	0.01	0.11	0.15	
	Vhys1.5		VTH1.5(+)-VTH1.5	-	0.03	-	
	VTH1.2	DC2FB	Detection	1.107	1.13	1.152	V
	VTH1.2(+)		Release	-	1.16	-	
	dVTH1.2		VDC2-1.2-VTH1.2	0.01	0.07	0.15	
	Vhys1.2		VTH1.2(+)-VTH1.2	-	0.03	-	
	VTH5	LDO1OUT	Detection	4.6	4.7	4.8	V
	VTH5(+)		Release	-	4.8	-	
	dVTH5		VLDO1-VTH5	0.25	0.30	0.35	
	Vhys5		VTH5(+)-VTH5	-	0.10	-	
	VTHL2	LDO2OUT	Detection	4.6	4.7	4.8	V
	VTHL2(+)		Release	-	4.8	-	
	dVTHL2		VLDO2-VTHL2	0.2	0.3	0.4	
	VhysL2		VTHL2(+)-VTHL2	-	0.10	-	
	VTHB5	VBU	Detection	4.55	4.7	4.85	V
	VTHB5(+)		Release	-	4.8	-	
	dVTHB5		VBU5-VTHB5	0.2	0.3	0.4	
	VhysB5		VTHB5(+)-VTHB5	-	0.10	-	
	VTHB3	VBU	Detection	3.0	3.1	3.2	V
	VTHB3(+)		Release	-	3.15	-	
	dVTHB3		VBU3-VTHB3	0.1	0.2	0.3	
	VhysB3		VTHB3(+)-VTHB3	-	0.05	-	
High-voltage detection Filter	tfVhTH	DC1FB,DC2FB, LDO1OUT, LDO2OUT,VBU		5	15	30	μs
Low-voltage detection filter	tfVTH	DC2FB, LDO1OUT, LDO2OUT,VBU		5	15	30	μs

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125°C. unless otherwise the follows

Characteristics	Symbol	Pin	Test Condition	Min	typ.	Max	Unit
Input output characteristics							
Input current	I_{IH}	SVO1, SVO2	V_{IN}=VDD2	20	40	80	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}			0.8xV_{DD2}	-	-	V
	V_{IL}			-	-	0.2xV_{DD2}	
Input current	I_{IH}	CTL1	V_{IN}=VB=13.5V	13	26	40	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input current	I_{IH}	CTL2	V_{IN}=VB=13.5V	13	26	40	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}	CTL1		3	-	-	V
	V_{IL}			-	-	1.0	
Input voltage	V_{IH}	CTL2		2	-	-	V
	V_{IL}			-	-	0.5	
Input current	I_{IH}	SLDO2	V_{IN}=VDD2	10	20	40	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}			0.8xV_{DD2}	-	-	V
	V_{IL}			-	-	0.2xV_{DD2}	
Input current	I_{IH}	SVBU	V_{IN}=VBU	4	8	13	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}			2	-	-	V
	V_{IL}			-	-	0.5	
Input current	I_{IH}	TEST	V_{IN}=VDD2	250	500	1000	μA
	I_{IL}		V_{IN}=0V	-	-	10	
Input voltage	V_{IH}			0.8xV_{DD2}	-	-	V
	V_{IL}			-	-	0.2xV_{DD2}	
Output voltage	V_{OL}	NOVDET	I_{OL}=2mA	-	-	0.3	V
Output leakage current	I_{LEAK}		V_{IN}=5V	-	-	5	μA
Output voltage	V_{OL}	NDIAG	I_{OL}=2mA	-	-	0.3	V
Output leakage current	I_{LEAK}		V_{IN}=V_{LDO1}	-	-	5	μA
Pull-up resistor	R_{diag}			-	10	-	kΩ
Internal electrical power source V_{DD1}, V_{DD2}							
Output voltage	V_{DD1}	VDD1		4.8	5.0	5.2	V
	V_{DD2}	VDD2		4.8	5.0	5.2	
Low-voltage detection	VTHD	VDD1, VDD2		3.8	4.0	4.2	V
Reset hysterics voltage	VTHDhys			-	0.1	-	V
High-voltage detection	VTHhD	VDD1, VDD2		5.5	5.75	6.0	V
Detection hysterics voltage	VTHhDhys			-	0.1	-	V
OSC							
Oscillated frequency	fosc	-		3.0	3.7	4.4	MHz
Frequency failure detection	fosc-H	-		-	7.4	-	MHz
	fosc-L	-		-	1.85	-	
TSD							
Overheating detection	TSD1, TSD2	-		150	170	180	°C

Overheating detection Filter	tfTSD1, tfTSD2	-		5	15	30	μs

The follows are under condition VB = 7 to 20.1V and Ta = -40 to 125℃. unless otherwise the follows

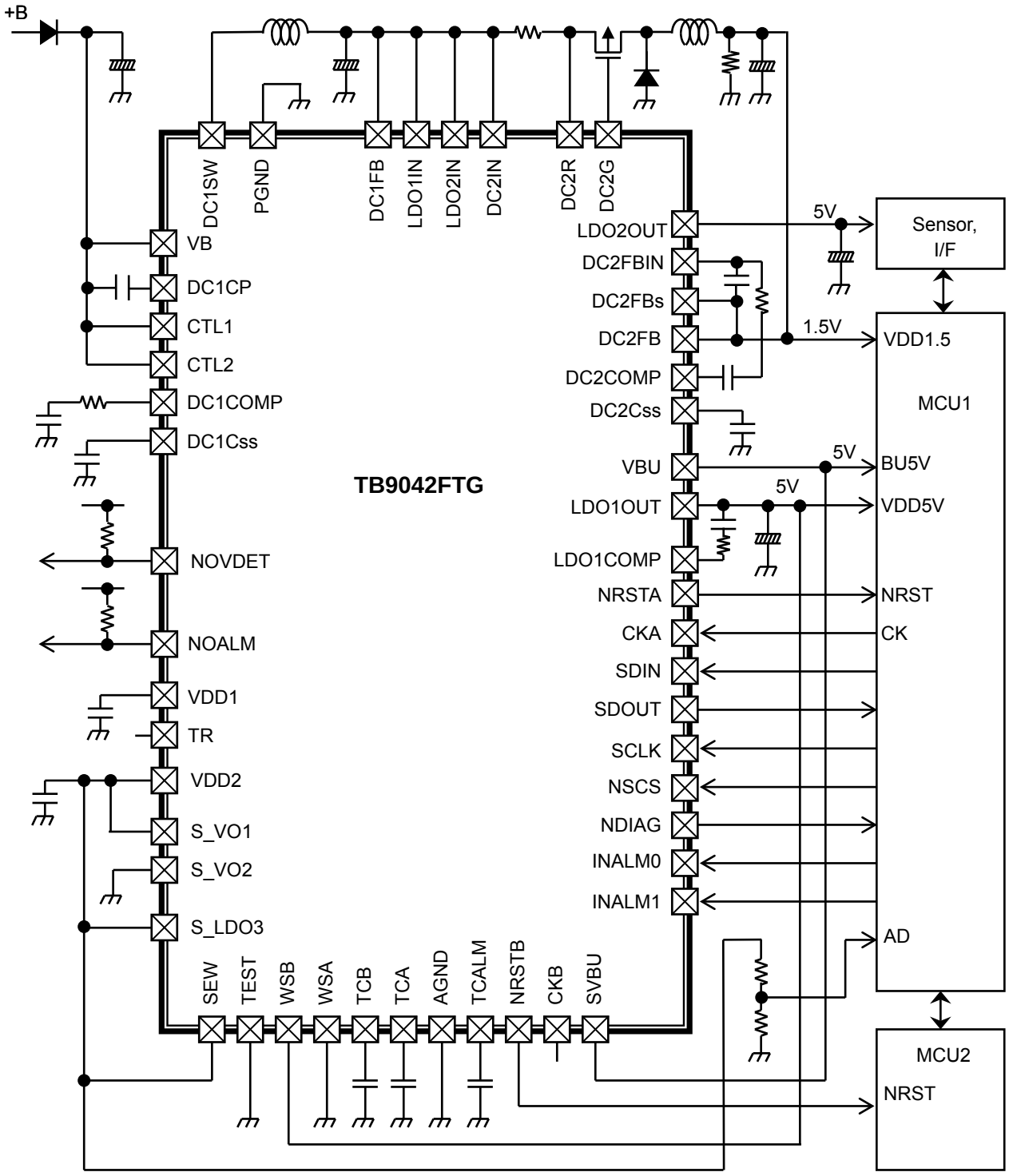
Characteristics	Symbol	Pin	Test Condition	Min	typ.	Max	Unit
Self-diagnostics							
Diagnostic stand by time	t_{DGs}	-		-	1	-	ms
Diagnostic time	t_{DGe}	-		-	1.5	-	ms
MCU alarm							
Input current	I_{IH}	INALM0	$V_{IN}=V_{LDO1}$	10	20	40	μA
	I_{IL}		V_{IN}=0V	-	-	10	
	I_{IH}	INALM1	$V_{IN}=V_{LDO1}$	-	-	10	
	I_{IL}		V_{IN}=0V	-40	-20	-10	
Input voltage	V_{IH}	INALM0, INALM1		$0.8xV_{LDO1}$	-	-	V
	V_{IL}			-	-	$0.2xV_{LDO1}$	
Input current	I_{IN}	TCALM		-	-10	-	μA
Discharge resistance	R_{DIS}			-	1	-	kΩ
Threshold voltage	V_{THAL}			-	4	-	V
MCU-ALM time	t_{ALM}	NOALM		-	$400xC_{TA}$	-	ms
Output voltage	V_{OL}	NOALM		-	-	0.3	V
Output leakage current	I_{LEAK}			-	-	5	μA
Alarm reset Time	$t_{RST-ALM}$	NOALM		-	1	-	ms
t_{ALM} maximum-settings time	t_{ALM-CO}	NOALM		15	18	21	ms
SPI DC characteristic							
Input current	I_{IH}	SDIN, SCLK	$V_{IN}=V_{LDO1}$	10	20	40	μA
	I_{IL}		V_{IN}=0V	-	-	10	
	I_{IH}	NSCS	$V_{IN}=V_{LDO1}$	-	-	10	
	I_{IL}		V_{IN}=0V	-40	-20	-10	
Input voltage	V_{IH}	SDIN, SCLK, NSCS		$0.8xV_{LDO1}$	-	-	V
	V_{IL}			-	-	$0.2xV_{LDO1}$	
Output voltage	V_{OH}	SDOUT	I_{OH}=-2mA	V_{LDO1}-0.3	-	-	V
	V_{OL}		I_{OL}=2mA	-	-	0.3	
Output leakage current	I_{LEAK}			-1	-	1	μA
The maximum TimeOut	$t_{OUT(max)}$	NRSTA, NRSTB		80	100	120	ms
SPI AC characteristics							
Communication characteristics	t_{CYCL}	NSCS, SCLK, SDIN, SDOUT		250	-	-	ns
	t_{SETL}			200	-	-	
	t_{SETH}			100	-	-	
	t_{CSH}			1500	-	-	
	t_{DOUT}			-	-	80	
	t_{DZ1}			-	-	100	
	t_{DZ2}			-	-	100	
	t_{DISU}			50	-	-	
	t_{DIH}			50	-	-	
	t_R	NSCS, SCLK, SDIN, SDOUT	20%-80%	-	-	2	
	t_F		80%-20%	-	-	2	
Transmission rate	R_{SPI}	SCLK, SDIN		-	-	4	Mbps

16. The example of an application circuit

The setting conditions of the example of application

- 6VDCDC converter
- DCDC2 voltage: 1.5V setup
- LDO1, LDO2 input: DCDC1 connection

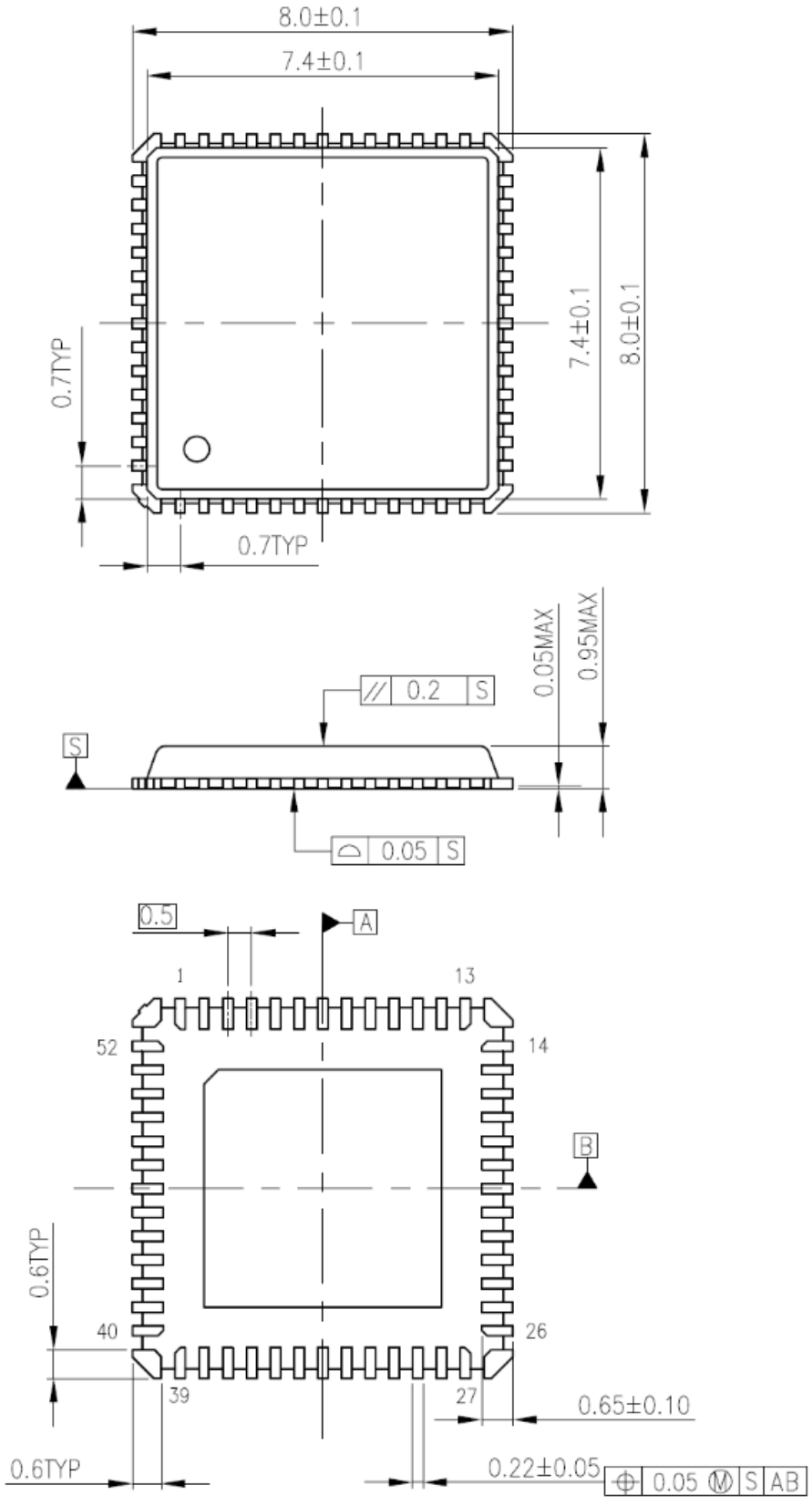
・Reset timer Ch-B is used only at the Power On Reset operation.



17. **Package Outline Dimensions**

P-HVQFN52-0808-0.50-001

Unit: mm



Weight: 0.154g (typ.)

18. Notes

Notes 1: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

Notes 2: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Notes 3: Timing charts may be simplified for explanatory purposes.

Notes 4: Please do not carry out incorrect wearing. There is a possibility of causing destruction of IC and damage to apparatus.

Notes 5: The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.

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