50 MHz, 16-BIT RESOLUTION CMOS NUMERICALLY CONTROLLED OSCILLATOR STEL-1174

ASIC Custom Products Division

STANFORD TELECOM

FEATURES

- 16-BIT FREQUENCY RESOLUTION
- 50-MHz CLOCK FREQUENCY (0 TO 70°C)
- SINE OR COSINE OUTPUT AVAILABLE
- 12-BIT AMPLITUDE RESOLUTION AND 13-BIT PHASE RESOLUTION GIVES HIGH SPECTRAL PURITY, ALL SPURS <–75 dBc (AT DIGITAL OUTPUT)
- MICROPROCESSOR BUS COMPATIBLE CONTROL INPUTS
- CASCADABLE ACCUMULATOR FOR HIGHER FREQUENCY RESOLUTION
- 2's COMPLEMENT OR OFFSET BINARY OUTPUT CODES
- LOW POWER CMOS
- MILITARY AND COMMERCIAL TEMPERATURE RANGES AVAILABLE

APPLICATIONS

- FREQUENCY SYNTHESIZERS
- SINGLE SIDEBAND CONVERTERS
- BASEBAND RECEIVERS
- DIGITAL SIGNAL PROCESSORS
- HIGH SPEED HOPPED FREQUENCY SOURCES

FUNCTIONAL DESCRIPTION

The STEL-1174 Numerically Controlled Oscillator (NCO) uses digital techniques to provide a cost-effective solution for low noise signal sources. The NCO device combines low power 1.5µ CMOS technology with a unique architectural design resulting in a power efficient, high-speed sinusoisdal waveform generator able to achieve fine tuning resolution and exceptional spectral purity with clock frequencies up to 50 MHz.

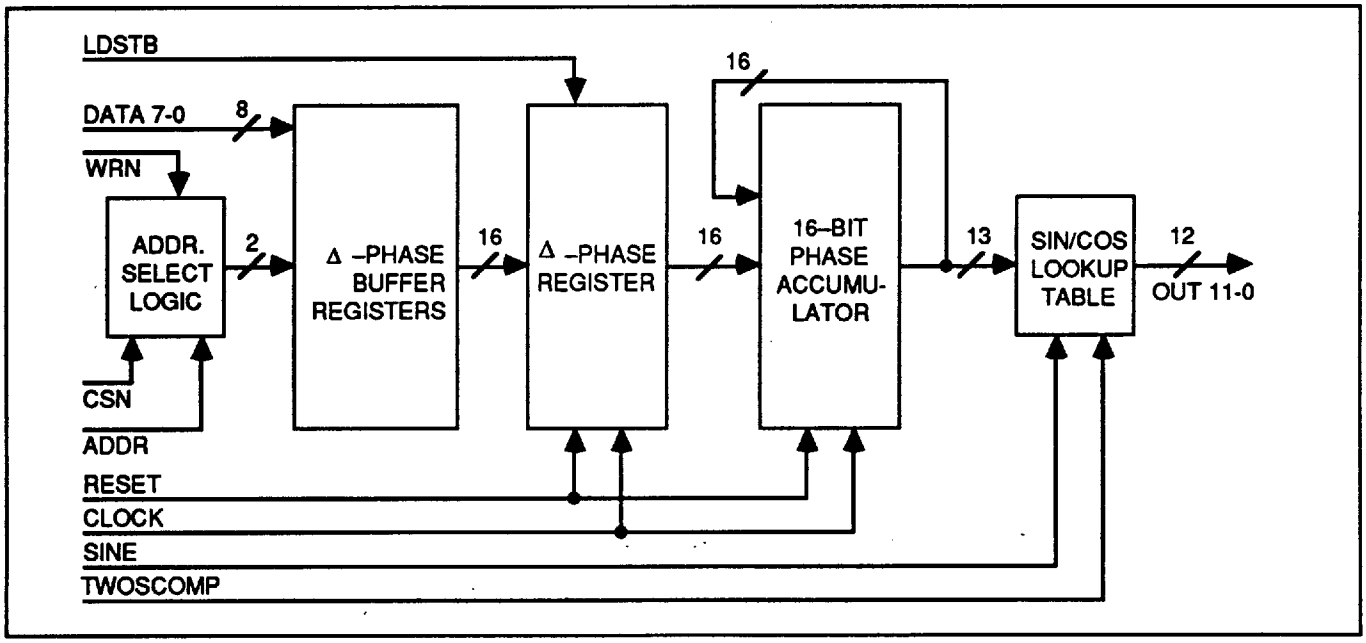
The NCO generates digital sine or cosine functions of very precise frequency to be used directly in digital signal processing applications or, in conjunction with a D/A converter, in analog frequency generation applications. The NCO is designed to interface with and be controlled from an 8-bit microprocessor bus.

The NCO maintains a record of phase which is accurate to 16 bits. At each clock cycle, the number stored in the 16 bit Δ-Phase register is added to the previous value of the phase accumulator. The number in the phase accumulator represents the current phase of the synthesized sine and cosine functions. The number in the Δ-Phase register represents the change of phase for each cycle of the clock. This number is directly related to the output frequency by the following:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{2^{16}}$$

where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

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The sine and cosine functions are generated from the 13 most significant bits of the phase accumulator. The frequency of the NCO is determined by the number stored in the Δ-Phase register which may be programmed by an eight-bit microprocessor.

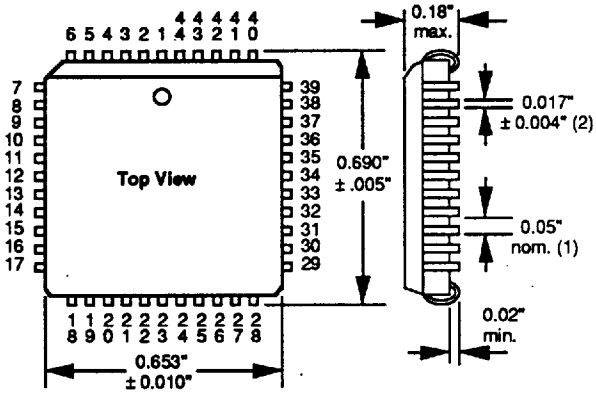
The frequency programming capability of the NCO is analogous to sampling a sine wave where the sampling function is the clock. If the output frequency is very low with respect to the clock ($< f_c/8096$), then the NCO output will sequence through each of the 8096 states of the sine function. As the output frequency is increased with respect to the clock the sine function will appear to be more discontinuous since there will be fewer samples in each cycle. At the Nyquist limit, when the output frequency is exactly half the clock, the output waveform reduces to a square wave. The practical upper limit of the NCO output frequency is about 40% of the clock frequency because spurious components created by sampling, which are at a frequency greater than half the clock frequency, become difficult to remove by filtering.

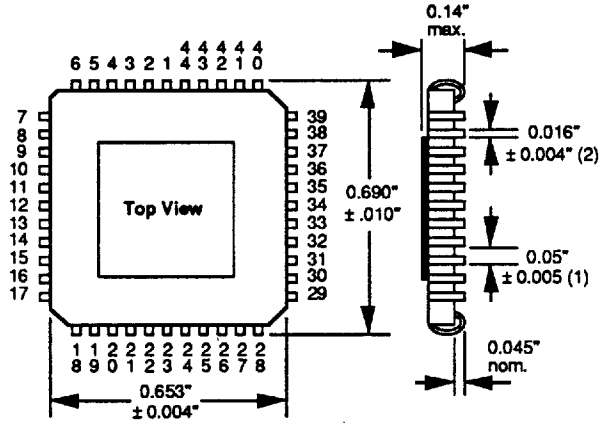
The phase noise of the NCO output signal may be determined by knowing the phase noise of the clock signal input, and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 12 clock cycles. This effectively limits the minimum possible frequency switching period of the NCO. After new frequency data is entered, the load command is given. After the 12 cycle pipeline delay, the output will instantaneously switch frequency while maintaining phase coherence. After this, the next new frequency may be entered. If a 50 MHz clock were utilized, the NCO could be continuously switched between programmed frequencies with a minimum practical average switching time of about 0.24 µsec.

PIN CONFIGURATION

Package: 44 pin PLCC Thermal coefficient, θ_{ja} = 40°/W





PIN CONNECTIONS

1	V_{SS}	12	WRN	23	V_{DD}	34	OUT_{10}
2	V_{SS}	13	V_{DD}	24	$OUT_{0\ (LSB)}$	35	$OUT_{11\ (MSB)}$
3	$DATA_0$	14	I.C.	25	OUT_1	36	V_{SS}
4	$DATA_1$	15	I.C.	26	OUT_2	37	I.C.
5	$DATA_2$	16	SINE	27	OUT_3	38	I.C.
6	$DATA_3$	17	TWOSCOMP	28	OUT_4	39	I.C.
7	$DATA_4$	18	LDSTB	29	OUT_5	40	CLOCK
8	$DATA_5$	19	I.C.	30	OUT_6	41	ADDR
9	$DATA_6$	20	CSN	31	OUT_7	42	I.C.
10	$DATA_7$	21	V_{SS}	32	OUT_8	43	V_{DD}
11	I.C.	22	RESET	33	OUT_9	44	V_{DD}

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK
This block controls the writing of data into the device via the **$DATA_{7-0}$** inputs. The data is written into the device on the rising edge of the **WRN** input, and the register into which the data is written is selected by the **ADDR** input. The writing of data is also controlled with the **CSN** input; this input must be low to enable writing.

BUFFER REGISTER BLOCK
The Buffer Register is used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously as two bytes per 16-bit Δ-Phase word. The data is transferred from this register into the Δ-Phase Register after a falling edge on the **LDSTB** input.

Δ-PHASE REGISTER BLOCK
This block controls the updating of the Δ-Phase word used in the Accumulator. The frequency data from the Buffer Register Block is loaded into this block after a falling edge on the **LDSTB** input.

PHASE ACCUMULATOR BLOCK
This block forms the core of the NCO function. It is a high-speed, pipelined, 16-bit parallel accumulator, generating a new sum in every clock cycle. The overflow signal is discarded), since the required output is the modulo (2^{16}) sum only. This represents the modulo (2π) phase angle.

SINE LOOK-UP TABLE BLOCK
This block is the sine memory. The 13 most significant bits from the Phase Accumulator are used to address this memory to generate the 12-bit **OUT_{11-0}** outputs.

INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low. When **RESET** goes low, all registers including the 16-bit input buffer are cleared within 30 nsecs. The data on the **OUT_{11-0}** bus will then be invalid for 6 clock cycles, and thereafter will remain at the value corresponding to zero phase, i.e., 2049 (801H), until a new frequency is loaded into the Δ-Phase register with a **LDSTB** command after the **RESET** returns to a logic one.

CLOCK
All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should be nominally a square wave at a maximum frequency of 50 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 8 nanoseconds. At each positive transition of the **CLOCK** signal, the number stored in the Δ-Phase register is added to the contents of the phase accumulator and the result is placed in the phase accumulator.

WRN
On the rising edge of the **WRN** input, the information on the 8-bit data bus is transferred to the buffer register selected by the **$ADDR_{2-0}$** bus.

CSN
The **CSN** (Chip Select) input is active low and can be used to control the writing of data into the chip. When this input is high all data writing via the **$DATA_{7-0}$** bus is inhibited.

ADDR
The address line **ADDR** controls the use of the **$DATA_{7-0}$** bus for writing frequency data to the Δ-Phase buffer registers as shown in the table below:

ADDR	Δ-Phase Register Field
0	Bits0 (LSB) –7
1	Bits 8–15 (MSB)

To write to all 16 bits of the phase write registers, the **$DATA_{7-0}$** bus must be used twice. Note that it is not necessary to reload unchanged bytes, and that the byte loading sequence may be random.

$DATA_7$ through **$DATA_0$**
The eight bit **$DATA_{7-0}$** bus is used to program the 16-bit Δ-Phase register. **$DATA_0$** is the least significant bit of the bus.

LDSTB
On the rising edge of the clock following the falling edge of the **LDSTB** input, the information in the 16-bit buffer register is transferred to the Δ-Phase register. The frequency of the NCO output will change 12 clock cycles after the **LDSTB** command due to pipelining delays.

TWOSCOMP
When the **TWOSCOMP** input is set high, the data appearing on the **OUT_{11-0}** bus is presented in two's complement code, and when it is set low, the data is presented in offset binary code. The limits of the data values in both codes is shown in the table:

Code →	Offset binary	2's Complement
Minimum value	+1 (001_H)	– 2047 (801_H)
Maximum value	+4095 (FFF_H)	+2047 ($7FF_H$)
Mean value	+2048 (800_H)	0 (000_H)

Both number formats produce sine or cosine waves which are symmetrical about the phase quadrant axis and the mean-value magnitude axis.

SINE
When the **SINE** input signal is set to a logic low level, the output signal appearing on the $\mathbf{OUT_{11\text{-}0}}$ bus is the cosine of the 16-bit accumulator's 13 most significant bits (bits 47-35, with 47 being the MSB). Normally set high, this signal allows the NCO to generate either sine or cosine signals. By using two devices, one set in the sine mode and the other set in the cosine mode, quadrature outputs may be obtained. The quadrature phase relationship of the two outputs will be maintained at all times provided the two devices are reset simultaneously and operate from a common clock signal.

A high level on the **SINE** input sets the output to be the sine of the 16-bit accumulator's 13 most significant bits. The value of the output for a given phase value follows the relationship:

2's comp = 2047 x sin (360 x phase)

offset bin = 2047 x sin (360 x phase) +2048

The result is accurate to within 1 LSB.

When this input is set low the output will be the cosine of the 16-bit accumulator's 13 most significant bits. The value of the output for a given phase value follows the relationship:

2's comp = 2047 x cos (360 x phase)

offset bin = 2047 x cos (360 x phase) +2048

again, accurate to within 1 LSB.

OUTPUT SIGNALS

$\mathbf{OUT_{11\text{-}0}}$
The signal appearing on the $\mathbf{OUT_{11\text{-}0}}$ bus is derived from the 13 most significant bits of the phase accumulator. The 12-bit sine or cosine function is presented in offset binary or two's complement format, depending on the status of the **TWOSCOMP** input. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 in offset binary and 1 in two's complement. The nominal phase (in degrees) of the sine wave output may be determined at any point by multiplying the decimal equivalent of the 13 most significant bits of the phase accumulator by (360/8096) and then adding (360/16384). $\mathbf{OUT_{11}}$ is the MSB, and $\mathbf{OUT_0}$ is the LSB.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{ss}.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD}+0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

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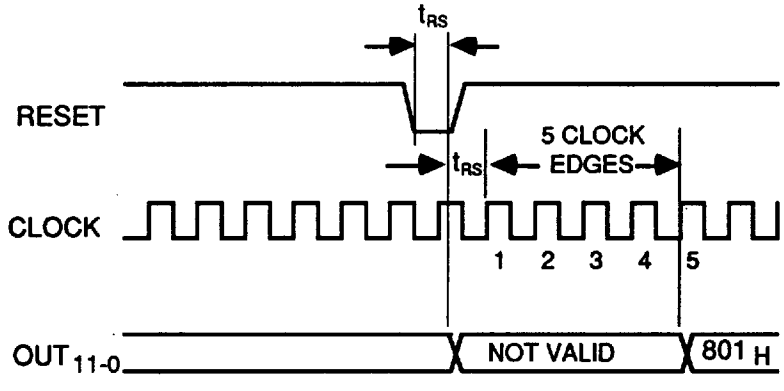
Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 5%	Volts (Commercial Conditions)
		+5 ± 10%	Volts (Military Conditions)
T_a	Operating Temperature (Ambient)	0 to +70	°C (Commercial Conditions)
		–55 to +125	°C (Military Conditions)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, V_{SS}=0 V, T_a= 0° to 70° C, Commercial
V_{DD}= 5.0 V ±10%, V_{SS}=0 V, T_a=–55° to 125° C, Military

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			3.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Commercial Operating Conditions	2.0			volts	Logic '1'
	Military Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**CIN** and **CSEL**, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–130	–45	–15	µA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –6.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +6.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

NCO RESET SEQUENCE



A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= 0° to 70° C (Commercial)
V_{DD}= 5.0 V ± 10%, V_{SS}=0 V, T_a=–55° to 125° C (Military)

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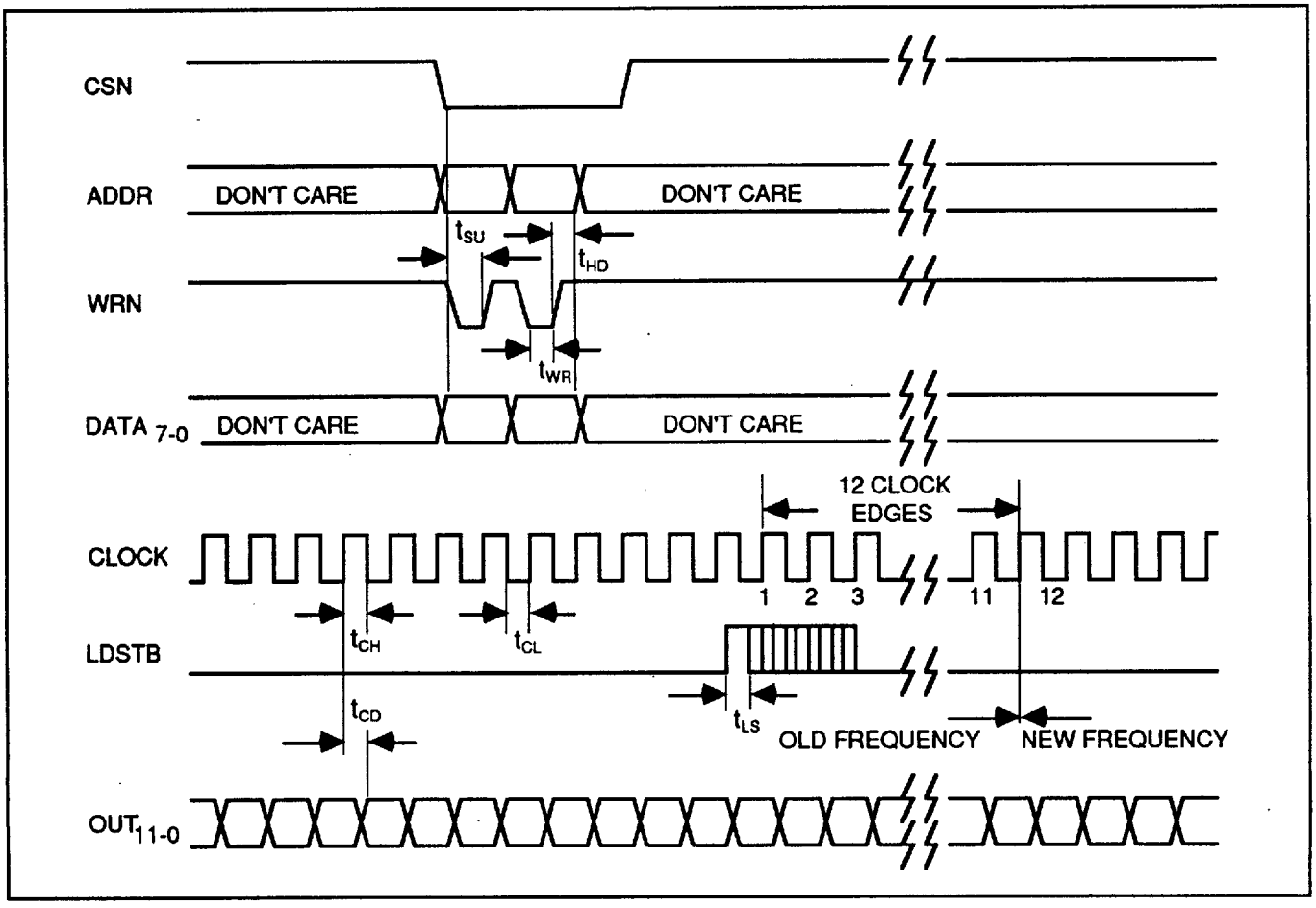
		(Commercial)		(Military)			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Conditions**
t_{RS}	**RESET** pulse width	30		35		nsec.	
t_{SR}	**RESET** to **CLOCK** Setup	10		10		nsec.	
t_{SU}	**DATA, ADDR** or **CSEL** to **WRN** Setup, and **LDSTB** to **CLOCK** Setup	18		25		nsec.	
t_{HD}	**DATA, ADDR** or **CSEL** to **WRN** Hold, and **LDSTB** to **CLOCK** Hold	12		15		nsec.	
t_{CH}	**CLOCK** high	8		10		nsec.	f_{CLK} = max.
t_{CL}	**CLOCK** low	8		10		nsec.	f_{CLK} = max.
t_W	**WRN** or **FRLD** pulse width	20		25		nsec.	
t_{CD}	**CLOCK** to output delay	5	10	3	13	nsec.	Load = 15 pF

NCO FREQUENCY CHANGE



SPECTRAL PURITY

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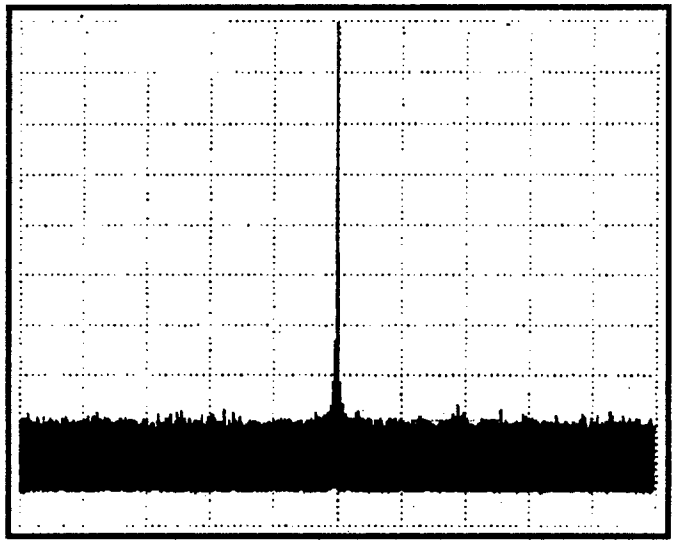
In many applications the NCO is used with a D to A converter (DAC to generate an analog signal. The spectral purity of this signal is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC. The signals generated by the STEL-1174 have 12 bits of amplitude resolution and 13 bits of phase resolution which results in spurious levels which are theoretically about –75 dBc. The highest output frequency the NCO can generate is half the clock frequency (f_c /2), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the NCO approaches $f_c/2$, the "image" spur at f_c-f_o (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 50 MHz and the output frequency is programmed to 6.789 MHz. This 10-bit DAC gives better performance than any of the currently available 12-bit DACs at clock frequencies higher than 20-25 MHz. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c- 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. A DAC with better dynamic linearity would be needed to improve the spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have larger steps from sample to sample and the DAC performance will degrade. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	6.7 MHz
Frequency Span:	10.0 MHz
Reference Level:	–5 dBm
Resolution Bandwidth:	1 KHz
Video Bandwidth:	3 kHz
Scale:	Log, 10 dB/div
Output frequency:	6.789 MHz
Clock frequency:	50 MHz



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