bq4115Y

512Kx8 NV Pseudo SRAM

Features

- Data retention in the absence of power
- Access time of 150 ns
- Automatic write-protection during power-up/power-down cycles
- Pseudo SRAM operation; unlimited read/write cycles
- Refresh handled internally
- No $\overline{CE}$ power-up cycles required
- BUSY pin indicates delayed start of read/write cycle
- Reset output for processor power-on reset
- Battery-fail warning

General Description

The CMOS bq4115Y is a nonvolatile pseudo static RAM organized as 512K words by 8 bits. The integral control circuitry and backup battery source provide reliable nonvolatility coupled with the unlimited write cycles of standard SRAM.

The control circuitry constantly monitors the single 5V supply for an out-of-tolerance condition. When V_{CC} falls out of tolerance, the PSRAM is unconditionally write-protected to prevent inadvertent write operation. At this time the external energy source is switched on to sustain the memory until after V_{CC} returns valid. After V_{CC} returns valid, the 8 start-up cycles required by the PSRAM are handled internally during the write-protect time.

Because a $\overline{CE}$ access might be requested during an internal refresh interval, a BUSY pin is provided to indicate that the PSRAM is in a refresh cycle and the output data will be delayed.

The bq4115Y uses a low-standby-current PSRAM, coupled with two small batteries to provide nonvolatility without long write-cycle times and the write-cycle limitations associated with EEPROM and flash. The internal rechargeable lithium battery can maintain data for about 2 weeks. After that time, the internal backup is switched to a lithium nonrechargeable cell that can maintain data for 7 additional months. The rechargeable battery begins charging when V_{CC} becomes valid.

If the duration of the power loss is less than 2 weeks, the bq4115Y can operate as a nonvolatile memory for greater than 10 years.

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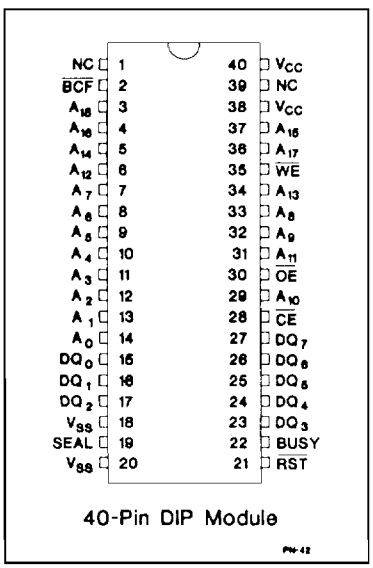
Pin Connections



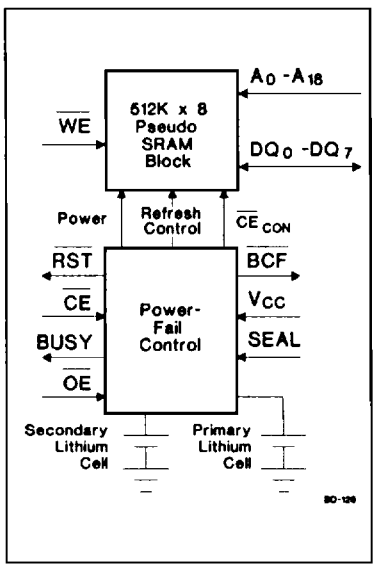
40-Pin DIP Module

PN-42

Pin Names

A_0-A_{18}	Address inputs
DQ_0-DQ_7	Data input/output
$\overline{BCF}$	Battery fail output
SEAL	Battery isolation signal input
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
$\overline{RST}$	Reset output
BUSY	Read/write cycle delay indicator open-drain output
NC	No connect
V_{CC}	+5 volt supply input
V_{SS}	Ground

Block Diagram



Functional Description

When power is valid, the bq4115Y operates as a standard CMOS PSRAM. During power-down and power-up cycles, the bq4115Y acts as a nonvolatile memory, automatically protecting and preserving the memory contents.

Power-down/power-up control circuitry constantly monitors the V_{CC} supply for a power-fail-detect threshold V_{PFD}. The bq4115Y monitors for V_{PFD} = 4.37V typical for use in systems with 10% supply tolerance.

When V_{CC} falls below the V_{PFD} threshold, the bq4115Y automatically write-protects the data. All inputs are treated as "don't care." If a valid access is in process at the time of power-fail detection, the memory cycle continues to completion. If the memory cycle fails to terminate within time t_{WPT}, write-protection takes place.

As V_{CC} falls past V_{PFD} and approaches 3V, the control circuitry switches to the internal rechargeable lithium backup supply, which provides data retention until valid V_{CC} is applied.

When V_{CC} returns to a level above the internal backup cell voltage, the supply is switched back to V_{CC}. After V_{CC} ramps above the V_{PFD} threshold, write-protection continues for a time t_{CER} (120ms maximum) to allow for processor stabilization. Normal memory operation may resume after this time.

The bq4115Y provides a power-on reset that goes active at a time t_R after V_{CC} reaches V_{PFD} on power-down and remains active for t_{RR} after V_{CC} reaches V_{PFD} on power-up. It is recommended that the $\overline{RST}$ pin be used as the reset for the micro to avoid the possibility of bus contention during this time period.

As shipped from Benchmarq, the internal batteries are electrically isolated from the memory. (Self-discharge in this condition is approximately 0.5% per year.) Following the first application of V_{CC}, this isolation is broken, and the lithium backup provides data retention on subsequent power-downs. The bq4115Y can be resealed by asserting the SEAL pin during valid V_{CC}. This causes the internal batteries to be disconnected from V_{OUT} after V_{CC} falls below V_{PFD}. Sealing a part is useful after testing, before the part is used.

Function Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0–A_{18}	DQ_0–DQ_7	Notes
Read	L	L	H	See note	Out	At $\overline{CE}$ falling edge, A_0–A_{18} are "in"; otherwise, A_0–A_{18} are "don't care."
Write	L	X	L	See note	In	At $\overline{CE}$ falling edge, A_0–A_{18} are "in"; otherwise, A_0–A_{18} are "don't care."
Standby	H	L	X	X	High Z	

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V_{CC}	DC voltage applied on V_{CC} relative to V_{SS}	-0.3 to 7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3 to 7.0	V	$V_T \le V_{CC} + 0.3$
T_{OPR}	Operating temperature	0 to +55	°C	
T_{STG}	Storage temperature	0 to +55	°C	
T_{BIAS}	Temperature under bias	-10 to +70	°C	
T_{SOLDER}	Soldering temperature	+260	°C	For 10 seconds
I_{OUT}	Short-circuit output current	300	mA	
P_D	Power dissipation	600	mW	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

Recommended DC Operating Conditions (T_A = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{SS}	Supply voltage	0	0	0	V	
V_{IL}	Input low voltage	-0.3	-	0.8	V	
V_{IH}	Input high voltage	2.2	-	V_{CC} + 0.3	V	

Note: Typical values indicate operation at T_A = 25°C.

DC Electrical Characteristics (T_A = TOPR, V_{CC} = 5V ± 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
I_{LI}	Input leakage current	-	-	± 1	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current	-	-	± 10	µA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
V_{OH}	Output high voltage	2.4	-	-	V	I_{OH} = -15 mA
V_{OL}	Output low voltage	-	-	0.55	V	I_{OL} = 64 mA
I_{SB1}	Standby supply current	-	6	10	mA	$\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ 0V, $\overline{OE}$ = V_{IH}
I_{SB2}	Standby supply current	-	20	200	µA	$\overline{CE}$ ≥ V_{CC} - 0.2V, 0V ≤ V_{IN}, $\overline{OE}$ ≥ V_{CC} - 0.2
I_{CC}	Operating supply current	-	50	65	mA	Min. cycle, duty = 100%, $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
V_{PFD}	Power-fail-detect voltage	4.30	4.37	4.50	V	

Notes: Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
Output levels are for I/O pins.

Capacitance (T_A = 25°C, F = 1MHz, V_{CC} = 5.0V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
C_{IN}	Input capacitance	-	-	8	pF	Input voltage = 0V

Note: These parameters are sampled and not 100% tested.

AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 1 and 2

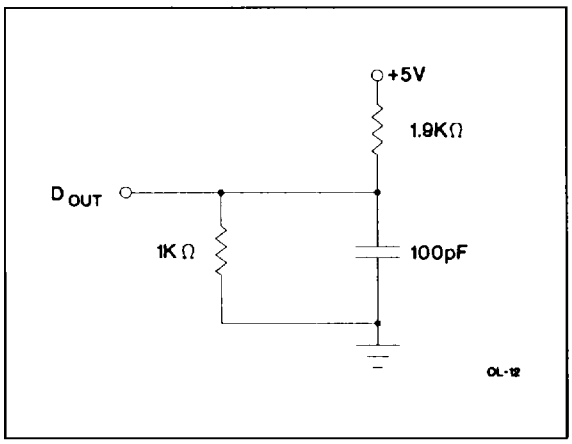


Figure 1. Output Load A

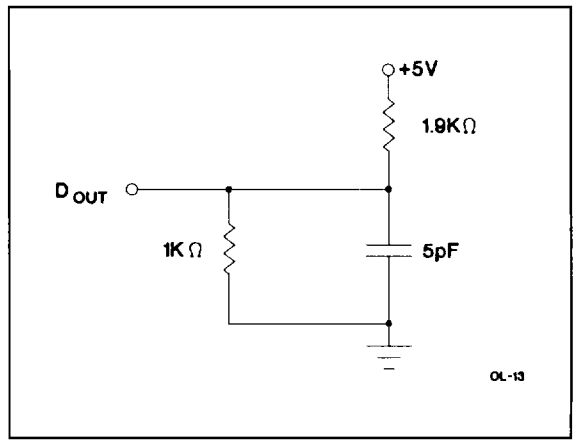


Figure 2. Output Load B

Read Cycle (T_A = 0 to 55°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{RC}	Random read,write cycle time	230	-	-	ns	
t_{RMW}	Read modify write cycle time	290	-	-	ns	
t_{CE}	Chip enable pulse width	150	-	5,000	ns	
t_P	Chip enable precharge time	80	-	-	ns	
t_{CB}	$\overline{CE}$ low to BUSY low	-	7	10	ns	
	$\overline{CE}$ low to BUSY low during refresh	-	-	400	ns	t_{CB} has a <6% probability of being longer than 150ns due to an internal refresh cycle
t_{OEA}	Output enable access time	-	-	90	ns	When not in refresh mode
t_{CLZ}	Chip enable to output in low Z	30	-	-	ns	When not in refresh mode
t_{OLZ}	Output enable to output in low Z	10	-	-	ns	
t_{BE}	BUSY low to $\overline{CE}$ high	150	-	5,000	ns	
t_{BA}	Access time from BUSY	-	-	150	ns	
t_{CHZ}	Chip disable to output in high Z	-	-	45	ns	
t_{OHZ}	Output disable to output in high Z	-	-	45	ns	
t_{OSC}	$\overline{OE}$ setup time referenced to $\overline{CE}$	0	-	-	ns	
t_{OHC}	$\overline{OE}$ hold time referenced to $\overline{CE}$	0	-	-	ns	
t_{RCS}	Read command setup time	0	-	-	ns	
t_{RCH}	Read command hold time	10	-	-	ns	
t_{AS}	Address setup time, referenced to $\overline{CE}$	0	-	-	ns	
t_{AH}	Address hold time, referenced to BUSY	30	-	-	ns	
t_{BH}	BUSY hold time from $\overline{CE}$ high to BUSY high	-	-	10	ns	
t_{OW}	Output active from end of write	5	-	-	ns	
t_T	Transition time (rise and fall)	3	-	50	ns	

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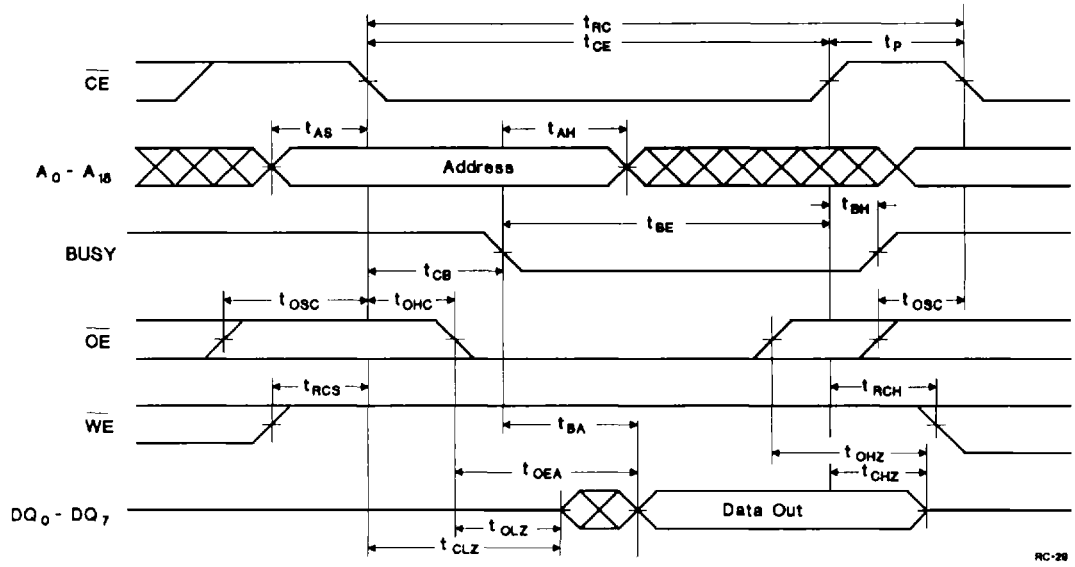
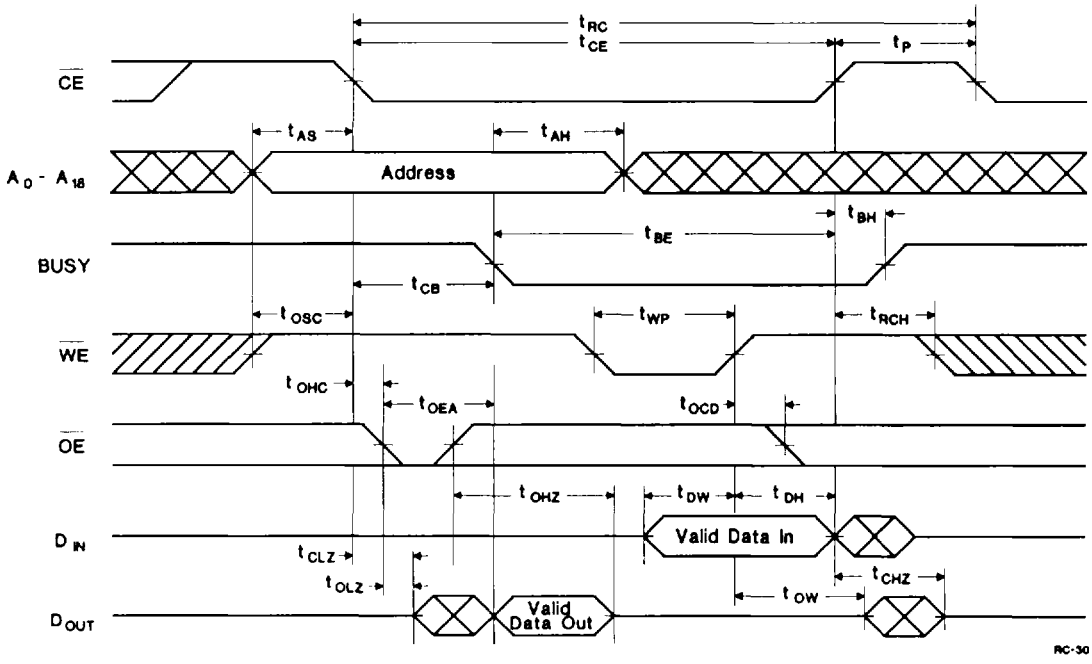
Read Cycle



Read Modify Write Cycle



Write Cycle (T_A = 0 to 55°C, V_{CC} = 5V ±10%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
t_{RC}	Random read,write cycle time	230	-	-	ns	
t_{CE}	Chip enable pulse width	150	-	5,000	ns	
t_P	Chip enable precharge time	80	-	-	ns	
t_{CB}	$\overline{CE}$ low to BUSY	-	7	10	ns	
	$\overline{CE}$ low to BUSY low during refresh	-	-	400	ns	t_{CB} has a <6% probability of being longer than 150ns due to an internal refresh cycle
t_{CLZ}	Chip enable to output in low Z	30	-	-	ns	When not in refresh mode
t_{OLZ}	Output enable to output in low Z	10	-	-	ns	
t_{BE}	BUSY to $\overline{CE}$ high	150	-	5,000	ns	
t_{OHZ}	Output disable to output in high Z	-	-	45	ns	
t_{WHZ}	Write enable to output in high Z	-	-	30	ns	
t_{WP}	Write pulse width	35	-	-	ns	
t_{CW}	Chip enable to end of write	150	-	-	ns	
t_{DW}	Data setup time from end of write	30	-	-	ns	
t_{DWH}	Data hold time from end of write	0	-	-	ns	
t_{AS}	Address setup time, referenced to $\overline{CE}$	0	-	-	ns	
t_{AH}	Address hold time, referenced to BUSY	30	-	-	ns	
t_{BH}	BUSY hold time from $\overline{CE}$	0	-	10	ns	
t_{OCD}	Chip enable to output enable delay	0	-	-	ns	
t_{OW}	Output active from end of write	5	-	-	ns	
t_T	Transition time (rise and fall)	3	-	50	ns	

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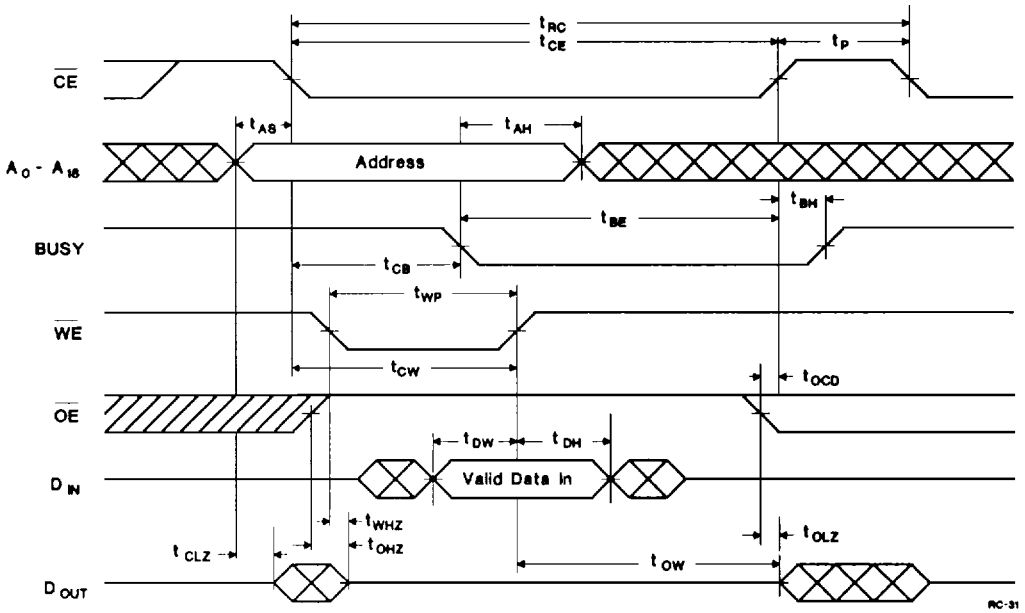
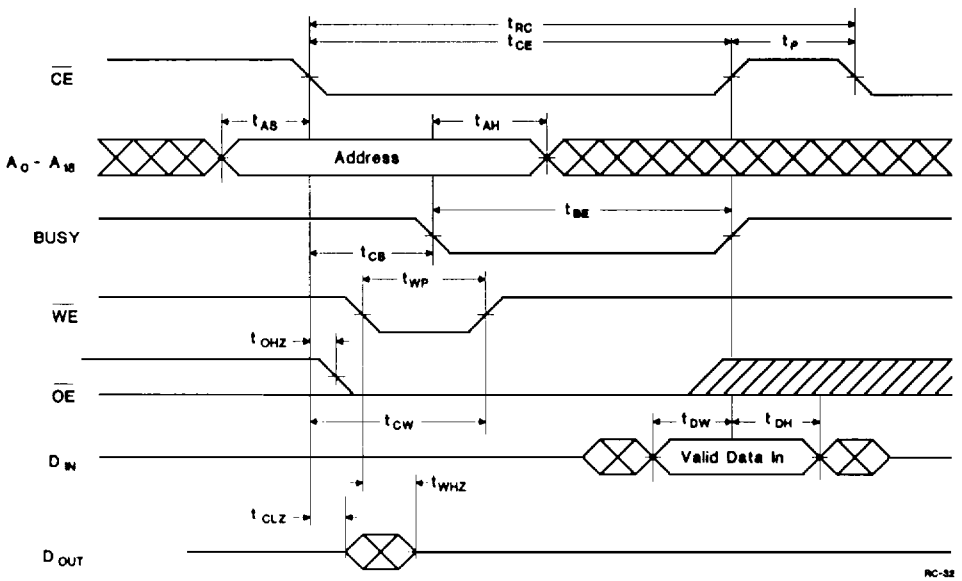
Write Cycle No. 1 ($\overline{OE}$ High)



Write Cycle No. 2 ($\overline{OE}$ Low)



Power-Down/Power-Up Cycle (T_A = 0 to 55°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
t_{PF}	V_{CC} slew, 4.75 to 4.25 V	300	-	-	µs	
t_{FS}	V_{CC} slew, 4.25 to V_{SO}	300	-	-	µs	
t_{PU}	V_{CC} slew, V_{SO} to V_{PFD} (max.)	300	-	-	µs	
t_{CER}	Chip enable recovery time	40	80	120	ms	Time during which PSRAM is write-protected after V_{CC} passes V_{PFD} on power-up.
t_{DR}	Data-retention time in absence of V_{CC}	7	-	-	months	For non-rechargeable; T_A = 25°C. (2)
		2	-	-	weeks	For rechargeable; T_A = 25°C. (2)
t_{WPT}	Write-protect time	40	100	150	µs	Delay after V_{CC} slews down past V_{PFD} before SRAM is write-protected.
t_R	V_{PFD} to $\overline{RST}$ active	40	100	150	µs	
t_{RR}	V_{PFD} to $\overline{RST}$ inactive	20	40	80	ms	

Notes:
1. Typical values indicate operation at T_A = 25°C, V_{CC} = 5V.
2. Batteries are disconnected from circuit until after V_{CC} is applied for the first time. t_{DR} is the accumulated time in absence of power beginning when power is first applied to the device.

Caution: **Negative undershoots below the absolute maximum rating of -0.3V in battery-backup mode may affect data integrity.**

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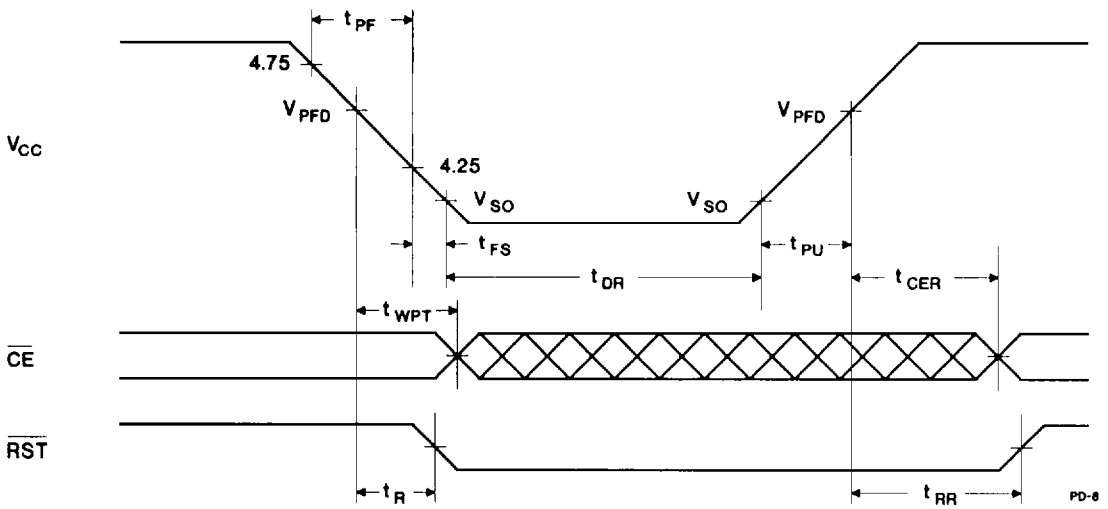
Power-Down/Power-Up Timing



Ordering Information