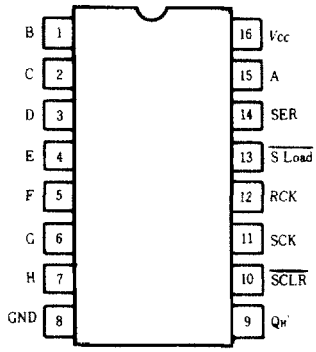
HD74HC597 ● 8-bit Latch/Shift Register

The HD74HC597 consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

■ FEATURES

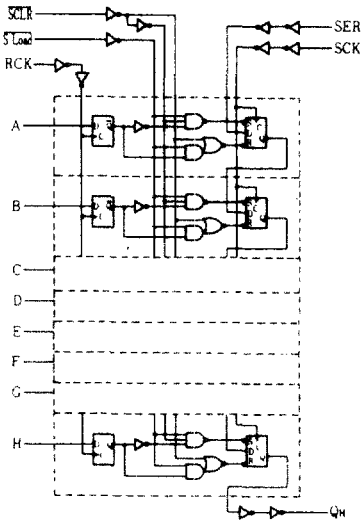
- High Speed Operation: t_{pd} (SCK to Q_H')=14ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC}=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: I_{CC} (static)=4μA max. (Ta=25°C)

■ PIN ARRANGEMENT



(Top View)

■ LOGIC DIAGRAM



■ FUNCTION TABLE

RCK	SCK	SLoad	SCLR	Function
↗	X	X	X	Data loaded to input latches
↗	X	L	H	Data loaded from inputs to shift register
X	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↗	H	H	Shift register clocked $Q_n=Q_{n-1}$, Q_A=SER

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25°C min	Ta=25°C typ	Ta=25°C max	Ta=−40~+85°C min	Ta=−40~+85°C max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25°C			Ta=−40~+85°C		Unit
				min.	typ	max.	min.	max.	
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	27	—	21	
		6.0		—	—	31	—	24	
Propagation Delay Time	t_{PLH}	2.0	SCK or $\overline{SLoad}$ or $\overline{SCLR}$ to Q_H'	—	—	175	—	220	ns
		4.5		—	14	35	—	44	
		6.0		—	—	30	—	37	
	t_{PHL}	2.0	RCK to Q_H'	—	—	210	—	265	ns
		4.5		—	17	42	—	53	
		6.0		—	—	36	—	45	
Removal Time	t_{rem}	2.0		100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
Setup Time	t_{su}	2.0	RCK to SCK	100	—	—	125	—	ns
		4.5		20	—	—	25	—	
		6.0		17	—	—	21	—	
		2.0	SER to SCK	100	—	—	125	—	ns
		4.5		20	1	—	25	—	
		6.0		17	—	—	21	—	
		2.0	Data to RCK	100	—	—	125	—	ns
		4.5		20	0	—	25	—	
		6.0		17	—	—	21	—	
Hold Time	t_h	2.0	SCK to S_A	5	—	—	5	—	ns
		4.5		5	—	—	5	—	
		6.0		5	—	—	5	—	
		2.0	LCK to Data	5	—	—	5	—	ns
		4.5		5	—	—	5	—	
		6.0		5	—	—	5	—	
Pulse Width	t_w	2.0		80	—	—	100	—	ns
		4.5		16	7	—	20	—	
		6.0		14	—	—	17	—	
Output Rise/Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	4	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF