PROGRAMMABLE UNIJUNCTION TRANSISTOR

Silicon planar PNPN trigger device in a plastic TO-92 envelope, intended for use in switching applications such as motor control, oscillators, relay replacement, timers, pulse shaper etc.

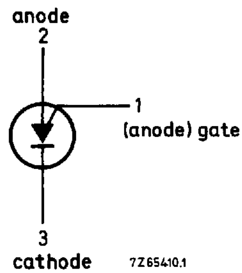
QUICK REFERENCE DATA

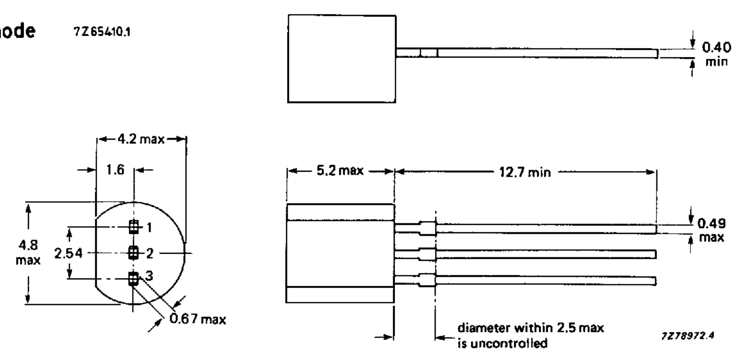
Gate-anode voltage	V_{GA}	max.	70 V
Anode current (average)	$I_{A(AV)}$	max.	175 mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
Junction temperature	T_j	max.	150 °C
Peak point current V_S = 10 V; R_G = 10 kΩ	I_P	max.	0.2 μA
Valley point current V_S = 10 V; R_G = 10 kΩ	I_V	min.	2 μA

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92.





Capability approved to CECC NECC-C-002

A and B selections are available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Gate-anode voltage	V_{GA}	max.	70	V
Anode current (average)	$I_{A(AV)}$	max.	175	mA
Repetitive peak anode current t_p = 10 μs; δ = 0,01	I_{ARM}	max.	2,5	A
Non-repetitive peak anode current t_p = 10 μs	I_{ASM}	max.	3,0	A
Rate of rise of anode current up to I_A = 2,5 A	$\frac{dI_A}{dt}$	max.	20	A/μs
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}	−65 to + 150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250	K/W

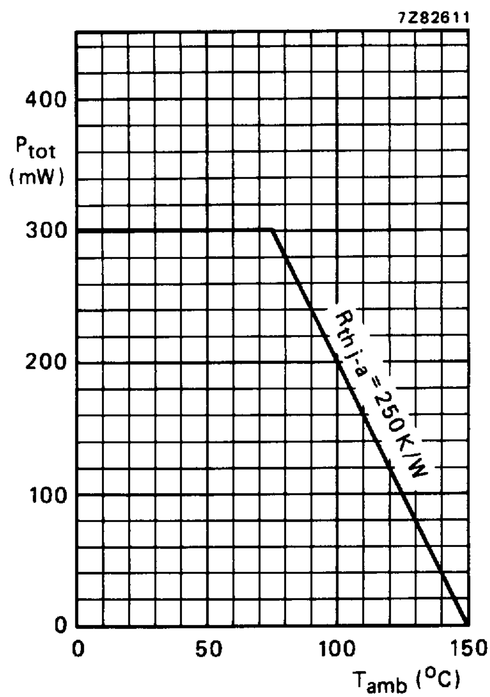


Fig. 2 Maximum permissible power dissipation as a function of ambient temperature.

CHARACTERISTICS

T_{amb} = 25 °C

Peak point current (see Fig. 10)			
V_S = 10 V; R_G = 10 kΩ	I_P	max.	0.2 μA
V_S = 10 V; R_G = 100 kΩ	I_P	max.	0.06 μA
Valley point current (see Fig. 10)			
V_S = 10 V; R_G = 10 kΩ	I_V	min.	2 μA
V_S = 10 V; R_G = 100 kΩ	I_V	min.	1 μA

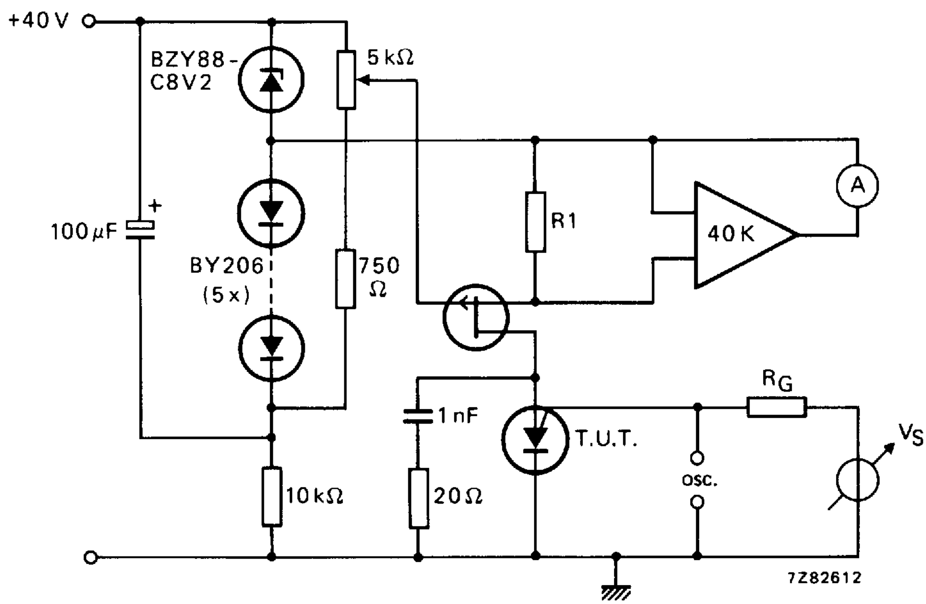


Fig. 3 Measuring circuit for I_P and I_V by means of value of R1. R1 = $\frac{1}{I_A}$ (that is maximum voltage drop over R1 is 1 V). Internal resistance of oscilloscope is 10 MΩ.

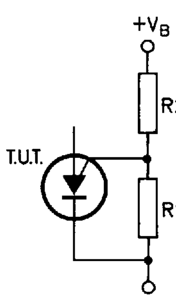


Fig. 4 **BRY56** with "program" resistors R1 and R2.

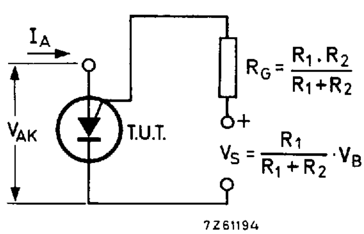


Fig. 5 Equivalent test circuit for characteristics testing.

Gate-anode leakage current (see Fig. 6)			
$I_K = 0$; $V_{GA} = 70$ V	I_{GAO}	max.	10 nA
Gate-cathode leakage current (see Fig. 7)			
$V_{AK} = 0$; $V_{GK} = 70$ V	I_{GKS}	max.	100 nA

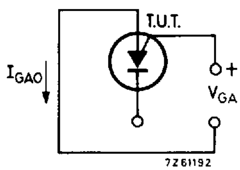


Fig. 6.

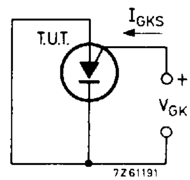


Fig. 7.

Anode-cathode voltage			
$I_A = 100$ mA	V_{AK}	max.	1,4 V
Peak output voltage (see Figs 8 and 9)			
$V_{AA} = 20$ V; C = 10 nF	V_{OM}	min.	6 V
Offset voltage (see Fig. 10) $V_{offset} = V_P - V_S$ ($I_A = 0$)			
Rise time (see Fig. 9)			
$V_{AA} = 20$ V; C = 10 nF	t_r	max.	80 ns

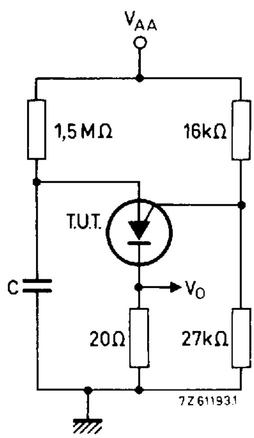


Fig. 8.

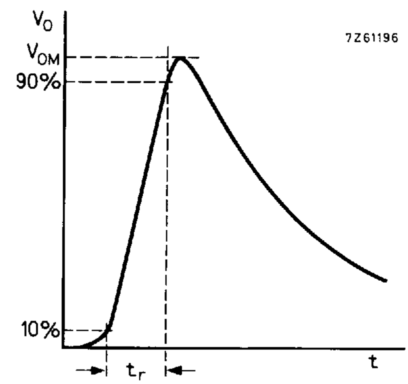


Fig. 9.

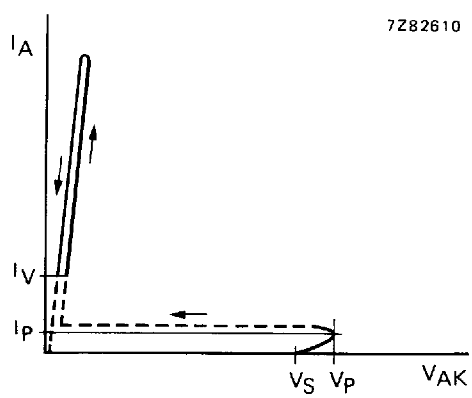


Fig. 10.