

PACE1753

SINGLE CHIP, 40MHz

CMOS MMU/COMBO

FEATURES

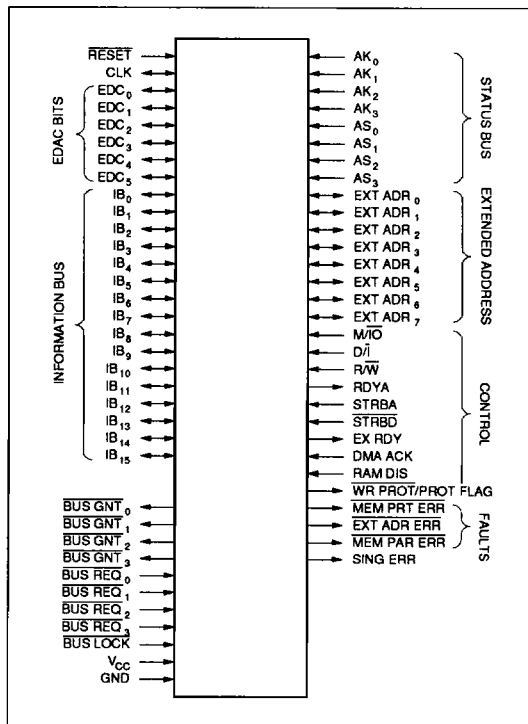
- Implements the MIL-STD-1750A Instruction Set Architecture for Memory Management and Protection of up to 1 Megaword. All mapping memory (10,240 bits) for both the MMU and BPU functions are included on the chip.
- Designed to interface memory to the PACE1750A/AE 16-bit, 40 MHz processor. Systems can be designed where no WAIT states are required up to 40 MHz clock rates when using these PACE products.
- System performance and device count are optimized when used with the PACE1754 Processor Interface Circuit (PIC) and PACE RAM™.
- Provides the following additional functions:
 - EDAC, Error Detection and Correction—or parity generation and detection
 - Correct data register—for diagnostics
 - First memory failing address register
- Illegal address error detection—programmable
- Multi-Master arbitration
- 8-bit extended address latches and drivers on chip
- Information bus and EDAC transceivers on chip
- 20, 30 and 40 MHz operation over the Military Temperature Range
- Single 5V ± 10% Power Supply
- Power Dissipation over Military Temperature Range (P_D Outputs Open)
 - < 0.20 watts at 20 MHz
 - < 0.30 watts at 30 MHz
 - < 0.40 watts at 40 MHz
- Available In:
 - 64-Pin DIP or Gull Wing (50 Mil Pin centers)
 - 68-Pin Pin Grid Array (PGA) (100 Mil centers)
 - 68-Lead Quad Pack (Leaded Chip Carrier)

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MEMORY MANAGEMENT UNIT AND BLOCK PROTECT UNIT "COMBO" (PACE1753)—FUNCTIONAL DESCRIPTION

The PACE1753 (COMBO) is a support chip for the PACE1750A/AE microprocessor family. It provides the following supporting functions to the system:

1. Memory management and access protection for up to 1M words.
2. Physical memory write protection for up to 1M words memory in pages of 1K words each. Separate protection is provided for the CPU and for DMA in systems which include DMA.
3. Detection of illegal I/O accesses (as defined by MIL-STD-1750A) or access to an unimplemented block of memory. In each case an error flag is generated to the processor.
4. Detection of double errors on the data bus and correction of single errors. An error signal is generated to the processor when a multiple error is detected.
5. RDYA generation. Up to three wait states can be inserted in the address phase of the bus by generating a not-ready, RDYA low signal. The number of wait states required can be programmed in an internal register in the COMBO.
6. Bus arbitration for up to 4 masters. Arbitration is done on a fixed priority basis (i.e. by interconnection of hardware). (In 68 pin package only).



ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage Range	0.5V to +7.0V
Input Voltage Range	0.5V to $V_{CC} + 0.5V$
Storage Temperature Range	-65°C to +150°C
Input Current Range	-30mA to +5mA
Current applied to any output ³	150mA
Maximum Power Dissipation ²	1.5W
Lead Temperature Range (soldering 10 seconds)	300°C
Thermal resistance (θ_{JC}): Cases X and T Cases Y and U Case Z	8°C/W 5°C/W 6°C/W

Notes

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Must withstand the added power dissipation due to short circuit test e.g., I_{OS} .
3. Duration 1 second or less.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	4.5V to +5.5V
Case Operating Temperature Range	-55°C to +125°C
Operating Maximum Power Dissipation (Outputs Open)	
Device Type 20MHz	0.20W
Device Type 30MHz	0.30W
Device Type 40MHz	0.40W

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Conditions ¹
V _{IH}	Input HIGH Voltage	2.0	V _{CC} + 0.5	V	
V _{IL}	Input LOW Voltage ²	-0.5	0.8	V	
V _{CD}	Input Clamp Diode Voltage		-1.2	V	V _{CC} = 4.5V, I _{IN} = -18mA
V _{OH}	Output HIGH Voltage	2.4		V	V _{CC} = 4.5V, I _{OH} = -8.0mA
		V _{CC} - 0.2		V	V _{IN} = 0.8V, 2.0V I _{OH} = -300μA
V _{OL}	Output LOW Voltage, except EXT ADR ₀ - EXT ADR ₇		0.5	V	V _{CC} = 4.5V, I _{OL} = 8.0mA
			0.2	V	V _{IN} = 0.8V, 2.0V I _{OL} = 300μA
V _{OL}	Output LOW Voltage, EXT ADR ₀ - EXT ADR ₇		0.5	V	V _{CC} = 4.5V, I _{OL} = 20.0mA
			0.2	V	V _{IN} = 0.8V, 2.0V I _{OL} = 300μA
I _{IH}	Input HIGH Current, except IB ₀ - IB ₁₅ , EDC ₀ - EDC ₅ , EXT ADR ₀ - EXT ADR ₇		10	μA	V _{IN} = V _{CC} , V _{CC} = 5.5V
I _{IH}	Input HIGH Current, IB ₀ - IB ₁₅ , EDC ₀ - EDC ₅ , EXT ADR ₀ - EXT ADR ₇		50	μA	V _{IN} = V _{CC} , V _{CC} = 5.5V
I _{IL}	Input LOW Current, except IB ₀ - IB ₁₅ , EDC ₀ - EDC ₅ , EXT ADR ₀ - EXT ADR ₇		-10	μA	V _{IN} = GND, V _{CC} = 5.5V
I _{IL}	Input LOW Current, IB ₀ - IB ₁₅ , EDC ₀ - EDC ₅ , EXT ADR ₀ - EXT ADR ₇		-50	μA	V _{IN} = GND, V _{CC} = 5.5V
I _{OZH}	Output Three-State Current		50	μA	V _{OUT} = 2.4V, V _{CC} = 5.5V
I _{OZL}	Output Three-State Current		-50	μA	V _{OUT} = 0.5V, V _{CC} = 5.5V
I _{CCQC}	Quiescent Power Supply Current (CMOS Input Levels, Active)		60	mA	V _{IN} < 0.2V or < V _{CC} - 0.2V f = 0MHz, Outputs Open, V _{CC} = 5.5V
I _{CCQT}	Quiescent Power Supply Current (TTL Input Levels, Active)		110	mA	V _{IN} = 3.4V, f = 0MHz, All Inputs, Outputs Open, V _{CC} = 5.5V
I _{CCD}	Dynamic Power Supply Current		40	mA	V _{CC} = 0V to V _{CC} , tr = tf = 2.5 ns, F = 20MHz
			50	mA	Outputs Open, F = 30MHz
			60	mA	V _{CC} = 5.5V, F = 40MHz
I _{OS}	Output Short Circuit Current ³	-25		mA	V _{OUT} = GND, V _{CC} = 5.5V
C _{IN}	Input Capacitance		10	pF	Inputs Only
C _{OUT}	Output/Bi-directional Capacitance		15	pF	Outputs Only (Including I/O Buffers)

Notes

1. 4.5V ≤ V_{CC} ≤ 5.5V, -55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.

2. V_{IL} = -3.0V for pulse widths less than or equal to 20ns.

3. Duration of the short should not exceed one second; only one output may be shorted at a time.



AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 4.5V$)

Symbol	Parameter	20 MHz		30MHz		40 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$TD/\bar{I}$ (EXT ADR) _V	MMU Cache Hit		25		23		23	ns
$TSTRBD$ (EXT ADR ERR) _L	External Address Error		25		20		16	ns
TC (IBD CORR)	Error Correction Read Cycle		25		20		19	ns
IBD_V (SING ERR) _H	Error Correction Read Cycle		35		30		25	ns
TC (SING ERR) _L	Error Correction Read Cycle		25		20		12	ns
$TIBD_V$ (EDC GEN) _V	EDAC or Parity Write Cycle		30		25		23	ns
$TSTRBD$ (EX RDY) _L	MMU Cache Miss		25		20		12	ns
TC (EX RDY) _H	MMU Cache Miss		25		20		12	ns
TC ($\overline{WR PROT}$) _L	MMU Cache Miss		25		22		18	ns
$TSTRBD_H$ ($\overline{WR PROT}$) _H	MMU Cache Miss		25		20		16	ns
TC ($\overline{GNT1}$) _H	Arbiter LOW to HIGH Priority		35		25		18	ns
TC ($\overline{GNT0}$) _L	Arbiter LOW to HIGH Priority		35		25		18	ns
TC ($\overline{GNT0}$) _H	Arbiter HIGH to LOW Priority		35		25		18	ns
TC ($\overline{GNT1}$) _L	Arbiter HIGH to LOW Priority		35		25		18	ns
TC (RDYA)	Address Ready		30		25		17	ns
TFC (IB OUT) _V	Clock to IB Out Valid (I/O Read)		30		28		25	ns
$TIBD_{IN}$ (MEM PAR ERR)	Parity Mode		34		30		25	ns
TC ($\overline{MEM PRT ERR}$)	Memory Protect Error		50		45		40	ns
$TSTRBD$ ($\overline{WR PROT}$)	Write Protect Cache Hit		25		20		16	ns
TC ($\overline{WR PROT}$) _L	Write Protect Cache Miss		25		22		18	ns
$TSTRBD_H$ ($\overline{WR PROT}$) _H	Write Protect Cache Miss		25		22		18	ns
$TD/\bar{I}$ (PROT FLAG)	Cache Hit (BPU Protection Error)		50		45		40	ns
$TD/\bar{I}$ (PROT FLAG)	Cache Hit (MMU Key-Lock Error)		40		35		30	ns
TC (PROT FLAG)	Cache Miss (BPU Protection Error)		45		35		30	ns
TC (PROT FLAG)	Cache Hit (MMU Key-Lock Error)		25		20		20	ns
TC (EXT ADR)	Clock to EXT ADR Valid (Miss)		32		30		23	ns

Notes:

1. $4.5V \leq V_{CC} \leq 5.5V$, $-55^\circ C \leq T_C \leq +125^\circ C$. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. $V_{IL} = -3.0V$ for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.
4. Pulse width of $\overline{WR PROT}$ /PROT FLAG shall be $\geq 80\%$ of STRBD pulse width.

TERMINAL CONNECTIONS

Case Outlines		T and X			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	23	IB ₁₃	44	AS ₁
2	EDC ₀	24	IB ₁₄	45	AS ₀
3	EDC ₁	25	IB ₁₅	46	GND
4	EDC ₂	26	MEM PRT ERR	47	AK ₃
5	RESET	27	MEM PAR ERR	48	AK ₂
6	EDC ₃	28	EXT ADR ERR	49	AK ₁
7	EDC ₄	29	RAM DIS	50	AK ₀
8	EDC ₅	30	SING ERR	51	CLK
9	IB ₀	31	DMA ACK	52	STRBA
10	IB ₁	32	GND	53	STRBD
11	IB ₂	33	EXT ADR ₀	54	GND
12	IB ₃	34	EXT ADR ₁	55	EX RDY
13	IB ₄	35	EXT ADR ₂	56	WR PROT/PROT FLAG
14	IB ₅	36	EXT ADR ₃	57	R/W
15	IB ₆	37	EXT ADR ₄	58	D/I
16	IB ₇	38	EXT ADR ₅	59	M/I $\bar{O}$
17	IB ₈	39	EXT ADR ₆	60	RDYA
18	IB ₉	40	EXT ADR ₇	61	NC
19	VCC	41	VCC	62	NC
20	IB ₁₀	42	AS ₃	63	NC
21	IB ₁₁	43	AS ₂	64	VCC
22	IB ₁₂				

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TERMINAL CONNECTIONS

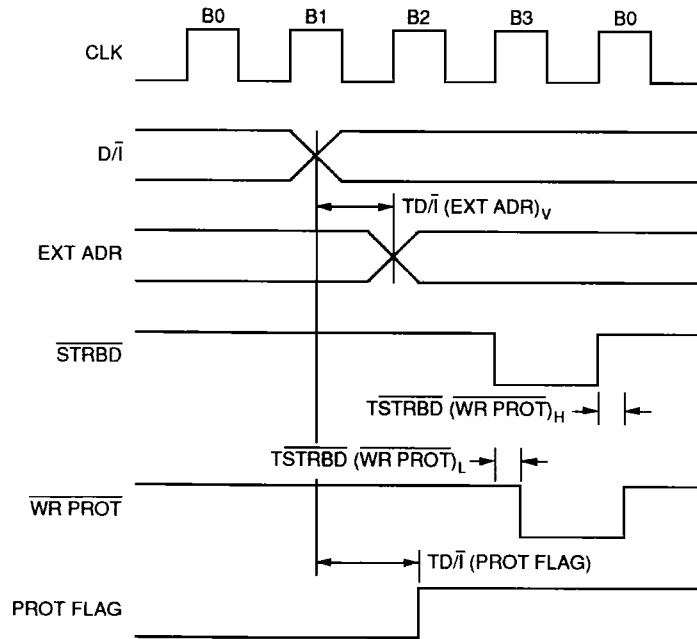
Case Outlines		U and Y			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	24	IB ₁₂	47	AS ₁
2	EDC ₀	25	IB ₁₃	48	AS ₀
3	EDC ₁	26	IB ₁₄	49	BUS REQ ₂
4	EDC ₂	27	IB ₁₅	50	AK ₃
5	RESET	28	MEM PRT ERR	51	AK ₂
6	EDC ₃	29	MEM PAR ERR	52	BUS GNT ₁
7	EDC ₄	30	EXT ADR ERR	53	AK ₁
8	EDC ₅	31	RAM DIS	54	AK ₀
9	BUS GNT ₂	32	SING ERR	55	CLK
10	IB ₀	33	DMA ACK	56	STRBA
11	IB ₁	34	GND	57	STRBD
12	IB ₂	35	V _{CC}	58	BUS REQ ₀
13	IB ₃	36	EXT ADR ₀	59	EX RDY
14	IB ₄	37	EXT ADR ₁	60	WR PROT/PROT FLAG
15	IB ₅	38	EXT ADR ₂	61	R/W
16	IB ₆	39	EXT ADR ₃	62	D/I
17	IB ₇	40	EXT ADR ₄	63	M/I _O
18	BUS REQ ₃	41	EXT ADR ₅	64	RDYA
19	IB ₈	42	EXT ADR ₆	65	BUS GNT ₀
20	IB ₉	43	EXT ADR ₇	66	BUS LOCK
21	BUS GNT ₃	44	GND	67	BUS REQ ₁
22	IB ₁₀	45	AS ₃	68	V _{CC}
23	IB ₁₁	46	AS ₂		

TERMINAL CONNECTIONS

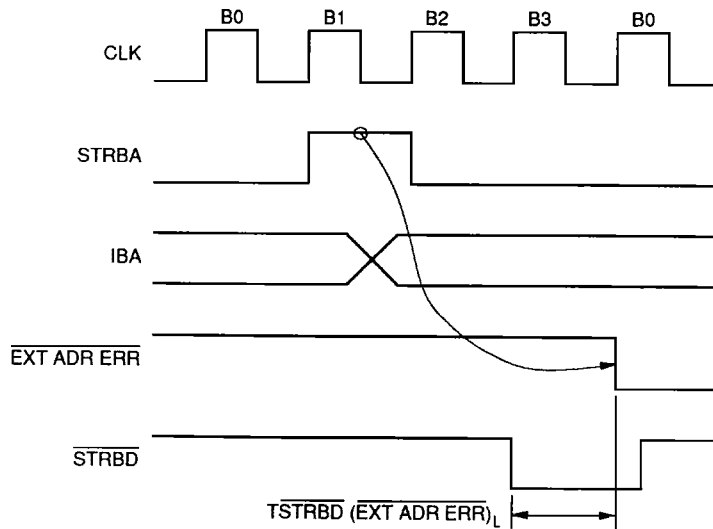
Case Outline		Z			
Pin	Pin Name	Pin	Pin Name	Pin	Pin Name
B1	IB ₁₄	L5	EDC ₁	D11	AS ₀
B2	IB ₁₃	K5	EDC ₀	D10	AS ₁
C1	IB ₁₂	L6	GND	C11	AS ₂
C2	IB ₁₁	K6	VCC	C10	AS ₃
D1	IB ₁₀	L7	$\overline{\text{BUS REQ}}_1$	B11	VCC
D2	$\overline{\text{BUS GNT}}_3$	K7	BUS LOCK	A10	GND
E1	IB ₉	L8	$\overline{\text{BUS GNT}}_0$	B10	EXT ADR ₇
E2	IB ₈	K8	RDYA	A9	EXT ADR ₆
F1	$\overline{\text{BUS REQ}}_3$	L9	M/ $\overline{\text{IO}}$	B9	EXT ADR ₅
F2	IB ₇	K9	D/ $\overline{\text{I}}$	A8	EXT ADR ₄
G1	IB ₆	L10	R/ $\overline{\text{W}}$	B8	EXT ADR ₃
G2	IB ₅	K11	$\overline{\text{WR PROT}}/\text{PROT FLAG}$	A7	EXT ADR ₂
H1	IB ₄	K10	EX RDY	B7	EXT ADR ₁
H2	IB ₃	J11	$\overline{\text{BUS REQ}}_0$	A6	EXT ADR ₀
J1	IB ₂	J10	STRBD	B6	GND
J2	IB ₁	H11	STRBA	A5	DMA ACK
K1	IB ₀	H10	CLK	B5	SING ERR
L2	$\overline{\text{BUS GNT}}_2$	G11	AK ₀	A4	RAM DIS
K2	EDC ₅	G10	AK ₁	B4	$\overline{\text{EXT ADR ERR}}$
L3	EDC ₄	F11	$\overline{\text{BUS GNT}}_1$	A3	$\overline{\text{MEM PAR ERR}}$
K3	EDC ₃	F10	AK ₂	B3	$\overline{\text{MEM PRT ERR}}$
L4	$\overline{\text{RESET}}$	E11	AK ₃	A2	IB ₁₅
K4	EDC ₂	E10	$\overline{\text{BUS REQ}}_2$		

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MMU Cache Hit



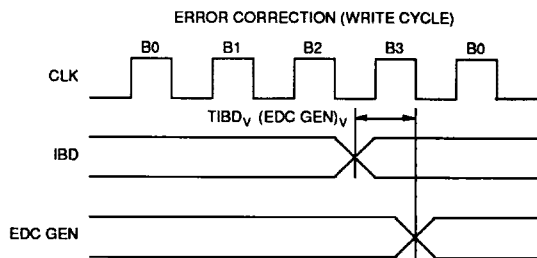
External Address Error



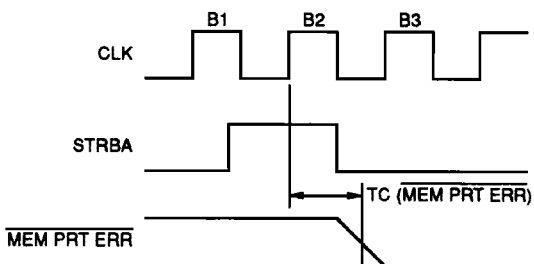
Note:

All time measurements on active signals relate to 1.5V levels.

Error Correction (Write Cycle)

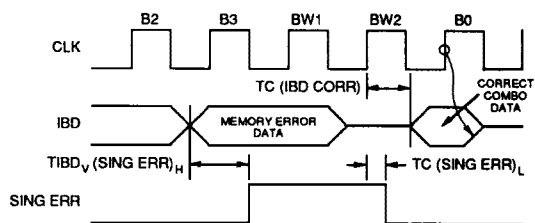


Memory Protect Error

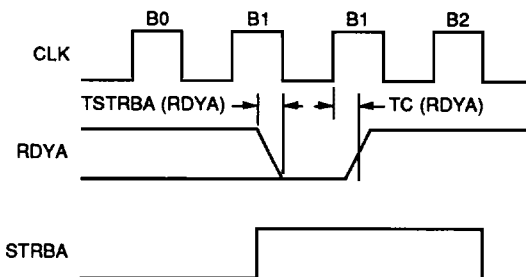


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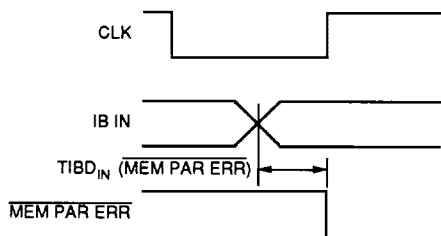
Error Correction (Read Cycle)



Ready Address



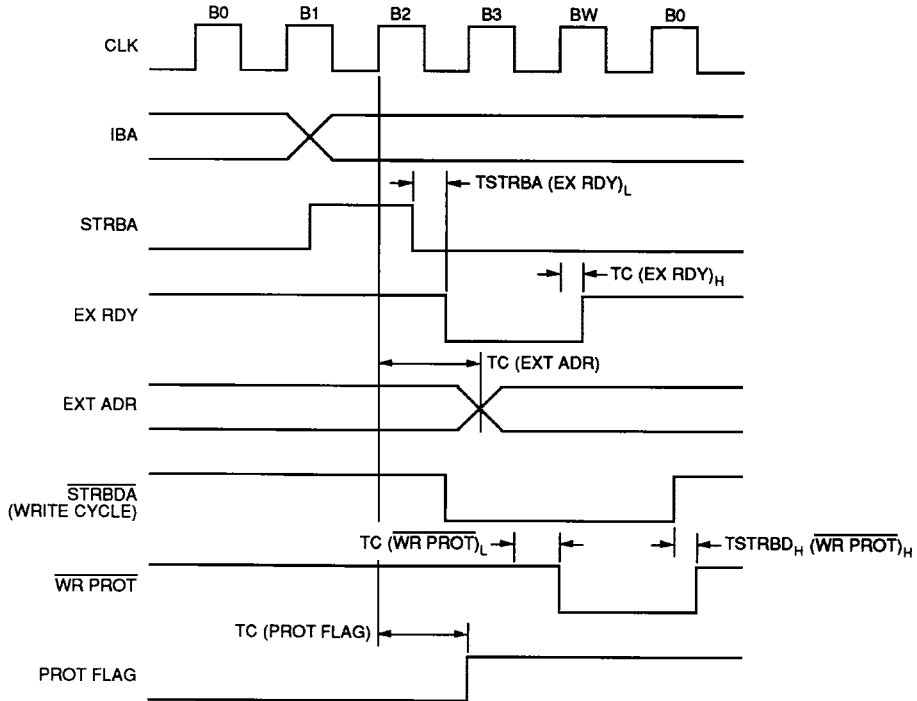
Memory Parity Error



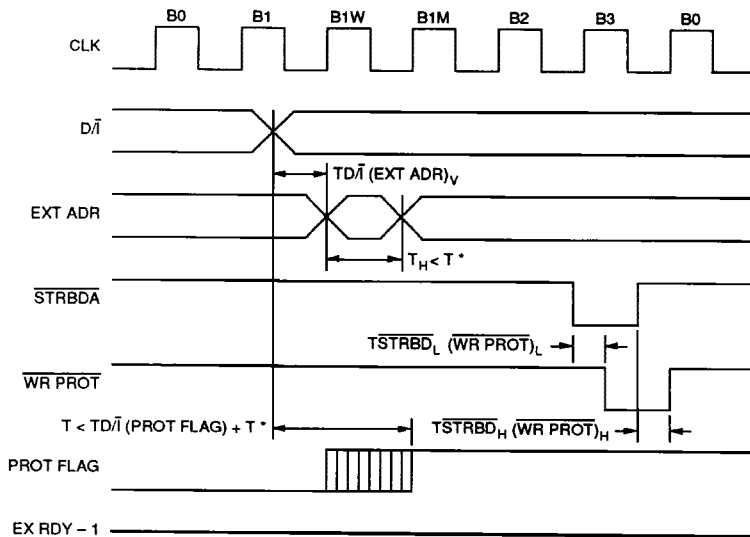
Note:

All time measurements on active signals relate to 1.5V levels.

MMU Cache Miss Cycle (WA = 0)



MMU Cache Miss Cycle (WA > 0)

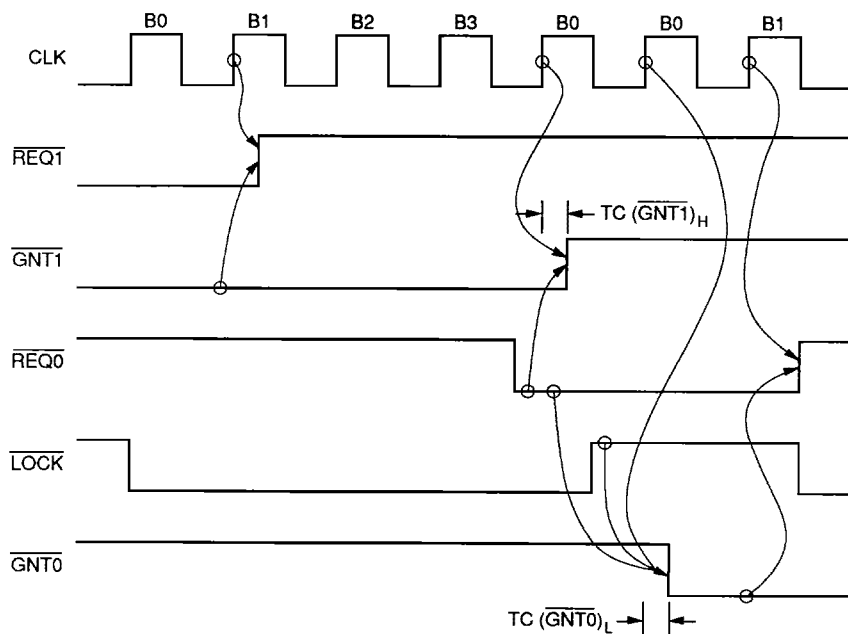


* The WR PROT/PROT FLAG signal is programmed as WR PROT or PROT FLAG. (See BPU Description), $T = 1$ Clock Period.

Note:

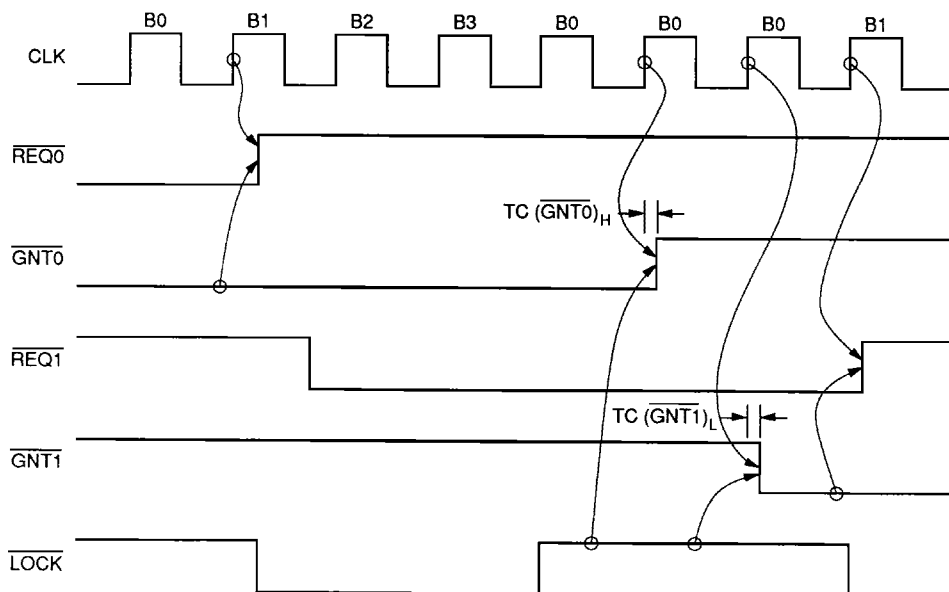
All time measurements on active signals relate to 1.5V levels.

Low Priority to High Priority Transition



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Bus Arbitrator High Priority to Low Priority Transition

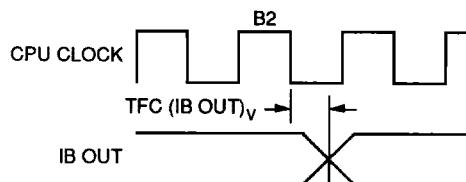


Note:

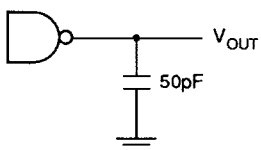
All time measurements on active signals relate to 1.5V levels.

SWITCHING WAVEFORMS AND TEST CIRCUIT (Continued)

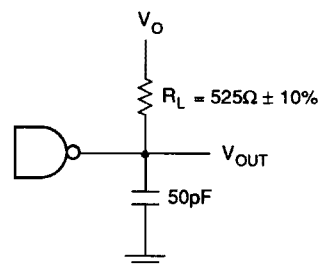
IB Bus Output (0:15)



Standard Output (Non Three-State)



Three-State



Note:

All time measurements on active signals relate to 1.5V levels.

Parameter	V_O	V_{MEA}
TPLZ	$\geq 3V$	0.5V
TPHZ	0V	$V_{CC} - 0.5V$
TPXL	$V_{CC}/2$	1.5V
TPXH	$V_{CC}/2$	1.5V

PIN FUNCTIONS

Symbol	Name	Description
BUS REQ ₀ - BUS REQ ₃	Bus Request ¹	Active low inputs that indicate a requirement for the bus from 4 masters on the bus. The master assigned to pin BUS-REQ ₀ has highest priority; the master assigned to pin BUS-REQ ₃ has lowest priority.
BUS LOCK	Bus Lock ¹	An active low input that indicates that the one master assigned the bus is using the bus. A new master will receive a bus grant only after this signal becomes inactive.
BUS GNT ₀ - BUS GNT ₃	Bus Grant ¹	Active low outputs indicating which master was granted the bus. It remains active during BUS LOCK unless a higher master request occurs, which resets it. However, the higher master will be granted the bus only after the present master's BUS LOCK releases the bus.
M/I $\bar{O}$	Memory or I/O	An input signal that indicates whether the current bus cycle is a memory (high) or I/O (low) cycle.
D/ $\bar{I}$	Data or Instruction	An input signal that indicates whether the current bus cycle access is for data (high) or instruction (low).
R/ $\bar{W}$	Read or Write	An input signal that indicates the direction of data flow on the bus. A high indicates a memory read or input operation into the master and a low indicates a memory write or output operation from the master.
STRBA	Address Strobe	An active high input used to latch the address at the high-to-low transition of the strobe.
STRBD	Data Strobe	An active low input used to strobe data in memory and I/O cycles.
CPU-CLK	CPU Clock	A single-phase input clock signal (0-40MHz, 40% to 60% duty cycle.)
RESET	Reset	An active low input that initializes the device.
AK ₀ - AK ₃	Access Key	Active high inputs used to match the access lock in the MMU page for memory accesses. A mismatch will cause the MEM PRT ERR signal to become active.
AS ₀ - AS ₃	Address State	Active high inputs that select the page register group in the MMU. In the DMA physical demultiplexed mode, AS(0:1) will receive the 9th and 10th most significant bits of the physical address for use in the BPU function.
EXT ADR ₀ - EXT ADR ₇	Extended Addresses Bus	A bi-directional active high bus. In CPU cycles, it is an output bus which is used to select one of 256 pages, 4K words each, expanding the direct addressing space to 1M word. In DMA cycles, indicated by DMA-ACK being active, it is also an output bus except when programmed for the physical demultiplexed DMA mode. In this case it becomes an input to receive the 8 most significant bits of the DMA physical address for use in the BPU function.
IB ₀ - IB ₁₅	Information Bus	An active high bi-directional time multiplexed address/data bus. IB ₀ is the most significant bit.
EDC ₀ - EDC ₅	Detection/Correction Bus	An active high bi-directional bus used for detection of errors on the data bus (IB ₀ - IB ₁₅) and correction of single errors. When working in parity mode EDC ₀ is the parity bit. EDC ₀ - EDC ₅ are undefined in this case.

PIN FUNCTIONS (Continued)

Symbol	Name	Description
MEM PRT ERR	Memory Protect Error	An active low output generated by the MMU or BPU blocks to signal to the CPU a protected memory violation. The error is generated in one of the following conditions: a mismatch in the access keys in the MMU page, an access to an execution protected page during instruction cycles, an access to a write-protected page during data cycles, or an access to a page write-protected by the BPU.
MEM PAR ERR	Memory Parity Error	An active low output which signals to the CPU an error on the data bus during a memory cycle. Two detection modes can be selected by programming the control register: EDAC mode (6 Hamming code parity bits) or single bit parity mode (even or odd parity). The signal is inactive when none of the above modes are selected (default after Reset).
EXT ADR ERR	External Address Error	An active low output which signals to the CPU an unimplemented memory or illegal I/O access.
SING ERR	Single Error	An active high output to signal detection of a single error on the data bus in memory cycles. It is high impedance when the EDAC function is disabled by the program (default state after Reset).
RAM DIS	RAM-Disable	An active high input from the 5962-88642 device which enables the corrected data on the data bus when the EDAC function is enabled. An internal one clock delay is generated before the data is output on the bus to allow external memory to disconnect itself from the bus.
EX RDY	Data Ready	An active high output that indicates that no wait states are requested. It becomes inactive for one clock (inserting one wait state) whenever a memory page different than the current one is accessed (causing a miss).
RDYA	Address Ready	An active high output that indicates that no wait states are requested when STRBA is active. Wait states are inserted when this signal becomes inactive during STRBA. Up to three wait states can be inserted by programming an internal register. Three wait states are inserted after Reset (default).
WR PROT/ PROT FLAG	Write Protected/ Protection Flag	Either an active low output (following STRBD timing) during legal memory write cycles, when no protection error occurs, or an active high level indicating a protection error in a write cycle. Each mode can be selected by programming the control register. Default mode after Reset is write-protected.
DMA ACK	DMA Acknowledge	An active high input from the DMA controller which indicates a DMA cycle. Used to select the DMA table in the BPU memory for protection. For example, this could allow the DMA channel to update the program which could be write-protected from the processor. In the physical DMA mode, it will cause the Extended Address Lines (EXT ADR ₀₋₇) to become inputs, providing BPU protection of the DMA transfers.

Note:

1. Used for Bus Arbitration; only available on 68-lead devices.

Standardized Military Drawing PIN	Vendor CAGE Number	Vendor similar PIN
5962-8950501UX	75569	P1753-20QLMB
5962-8950501YX	75569	P1753-20QGMB
5962-8950501ZX	75569	P1753-20PGMB
5962-8950502UX	75569	P1753-30QLMB
5962-8950502YX	75569	P1753-30QGMB
5962-8950502ZX	75569	P1753-30PGMB
5962-8950503UX	75569	P1753-40QLMB
5962-8950503YX	75569	P1753-40QGMB
5962-8950503ZX	75569	P1753-40PGMB
5962-8950504TX	75569	P1753-20GMB
5962-8950504XX	75569	P1753-20CMB
5962-8950505TX	75569	P1753-30GMB
5962-8950505XX	75569	P1753-30CMB
5962-8950506TX	75569	P1753-40GMB
5962-8950506XX	75569	P1753-40CMB

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ORDERING INFORMATION

