HARRIS

HSP45102

PRELIMINARY

May 1991

12-Bit Numerically Controlled Oscillator

Features

- 33MHz, 40MHz, 50MHz Versions
- 32-Bit Frequency Control
- Binary FSK Modulation
- Quadrature Phase Modulation
- Serial Frequency Load
- 12-Bit Sine Output
- Offset Binary Output Format
- 0.012Hz Tuning Resolution at 50MHz
- Spurious Frequency Components < -69dBc
- Fully Static CMOS
- Available in 28 Pin DIP and 28 Pin SOIC
- Low Cost

Applications

- Direct Digital Synthesis
- Modulation — QPSK and FSK

Description

The Harris HSP45102 is a 12 bit Numerically Controlled Oscillator (NCO12) for Direct Digital Synthesis Applications where low cost is important. As shown in the block diagram, the chip consists of a Frequency Control Section, a 32 bit phase accumulator, a phase offset adder and a Sine ROM.

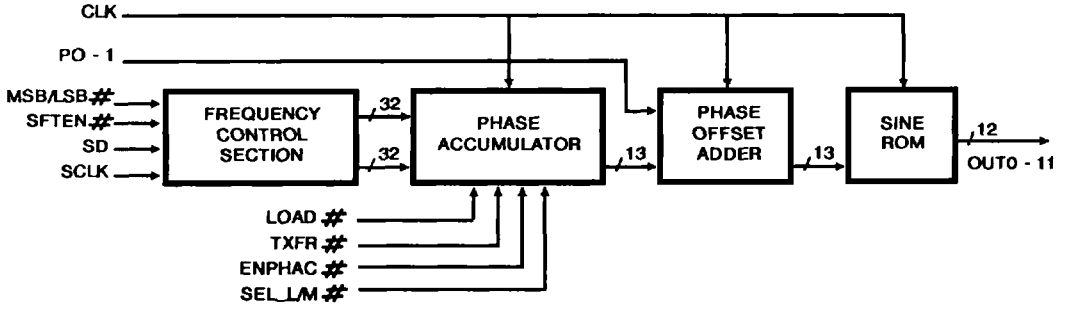
Two frequency control words are loaded serially, MSB or LSB first. A single control pin, SEL__L/M#, selects which word is used to determine the output frequency. This pin is toggled for FSK modulation. The output of the Frequency Control Section is two 32 bit phase increments to the Phase Accumulator, of which one is selected using SEL__L/M#.

Two pins are provided for phase modulation. These two bits, P0-1, are encoded and added to the top two bits of the phase accumulator to offset the phase in 90^{0} increments.

The 13 bit output of the Phase Offset Adder is mapped to the sine wave amplitude via the Sine ROM. The output data format is offset binary to simplify interfacing to D/A converters. Spurious frequency components in the output sinusoid are less than -69dBc.

The NCO12 has applications as a Direct Digital Synthesizer and modulator in low cost digital radios, satellite terminals, and function generators.

Block Diagram

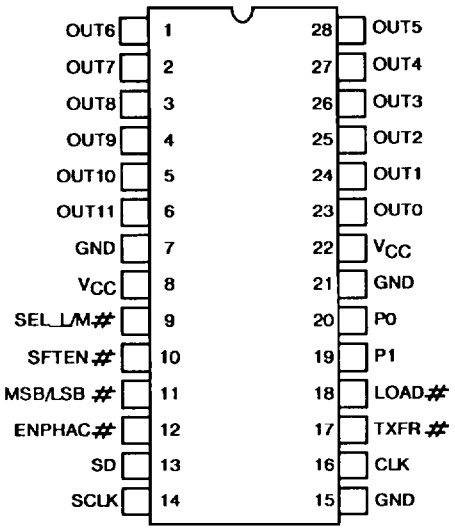


5 SIGNAL SYNTHESIZERS

File Number **2810**

Pinout

28 PIN DIP, 28 PIN SOIC
TOP VIEW



Pin Description

NAME	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	8, 22		+5V power supply pin.
GND	7, 15, 21		Ground
P0-1	19, 20	I	Phase modulation inputs (become active after a pipeline delay of four clocks). A phase shift of 0, 90, 180, or 270 degrees can be selected (Table 1).
CLK	16	I	NCO clock. (CMOS level)
SCLK	14	I	This pin clocks the frequency control shift register.
SEL_L/M#	9	I	A high on this input selects the least significant 32 bits of the 64 bit frequency register as the input to the phase accumulator; a low selects the most significant 32 bits.
SFTEN#	10	I	The active low input enables the shifting of the frequency register.
MSB/LSB#	11	I	This input selects the shift direction of the frequency register. A low on this input shifts in the data LSB first; a high shifts in the data MSB first.
ENPHAC#	12	I	This pin, when low, enables the clocking of the Phase Accumulator. This input has a pipeline delay of four clocks.
SD	13	I	Data on this pin is shifted into the frequency register by the rising edge of SCLK when SFTEN# is low.
TXFR#	17	I	This active low input is clocked onto the chip by CLK and becomes active after a pipeline delay of four clocks. When low, the frequency control word selected by SEL_L/M# is transferred from the frequency register to the phase accumulator's input register.
LOAD#	18	I	This input becomes active after a pipeline delay of five clocks. When low, the feedback in the phase accumulator is zeroed.
OUT0-11	1-6, 23-28	O	Output data. OUT0 is LSB.

All inputs are TTL level, with the exception of CLK.

sign designates active low signals.

Functional Description

The NCO12 produces a 12 bit sinusoid whose frequency and phase are digitally controlled. The frequency of the sine wave is determined by one of two 32 bit words. Selection of the active word is made by SEL__L/M#. The phase of the output is controlled by the two bit input P0-1, which is used to select a phase offset of 0^o, 90^o, 180^o, or 270^o.

As shown in the Block Diagram, the NCO12 consists of a Frequency Control Section, a Phase Accumulator, a Phase Offset Adder and a Sine ROM. The Frequency Control section serially loads the frequency control word into the frequency register. The Phase Accumulator and Phase Offset Adder compute the phase angle using the frequency control word and the two phase modulation inputs. The Sine ROM generates the sine of the computed phase angle. The format of the 12 bit output is offset binary.

Frequency Control Section

The Frequency Control Section (Figure 1), serially loads the frequency data into a 64 bit, bidirectional shift register. The shift direction is selected with the MSB/LSB# input. When this input is high, the frequency control word on the SD input is shifted into the register MSB first. When MSB/LSB# is low the data is shifted in LSB first. The register shifts on the rising edge of SCLK when SFTEN# is low. The timing of these signals is shown in Figure 2.

The 64 bits of the frequency register are sent to the Phase Accumulator Section where 32 bits are selected to control the frequency of the sinusoidal output.

Phase Accumulator Section

The phase accumulator and phase offset adder compute the phase of the sine wave from the frequency control word and the phase modulation bits P0-1. The architecture is shown in Figure 1. The most significant 13 bits of the 32 bit phase accumulator are summed with the two bit phase offset to generate the 13 bit phase input to the Sine Rom. A value of 0 corresponds to 0^o, a value of 1000 hexadecimal corresponds to a value of 180^o.

The phase accumulator advances the phase by the amount programmed into the frequency control register. The output frequency is equal to $N*Fclk/2^{32}$, where N is the selected 32 bits of the frequency control word. For example, if the control word is 20000000 hexadecimal and the clock frequency is 30Mhz, then the output frequency would be Fclk/8 or 3.75Mhz.

The frequency control multiplexer selects the least significant 32 bits from the 64 bit frequency control register when SEL__L/M# is high, and the most significant 32 bits when SEL__L/M# is low. When TXFR# is asserted, the 32 bits selected by the frequency control multiplexer are clocked into the phase accumulator input register. At each clock, the contents of this register are summed with the current contents of the accumulator to step to the new phase. The phase accumulator stepping may be inhibited by holding ENPHAC# high. The phase accumulator may be loaded with the value in the input register by asserting LOAD#, which zeroes the feedback to the phase accumulator.

The phase adder sums the encoded phase modulation bits P0-1 and the output of the phase accumulator to offset the phase by 0, 90, 180 or 270 degrees. The two bits are encoded to produce the phase mapping shown in Table 1. This phase mapping is provided for direct connection to the in-phase and quadrature data bits for QPSK modulation.

TABLE 1

P0-1 CODING		
P1	**P0**	**PHASE SHIFT (DEGREES)**
0	0	0
0	1	90
1	0	270
1	1	180

ROM Section

The ROM section generates the 12 bit sine value from the 13 bit output of the phase adder. The output format is offset binary and ranges from 001 to FFF hexadecimal, centered around 800 hexadecimal.

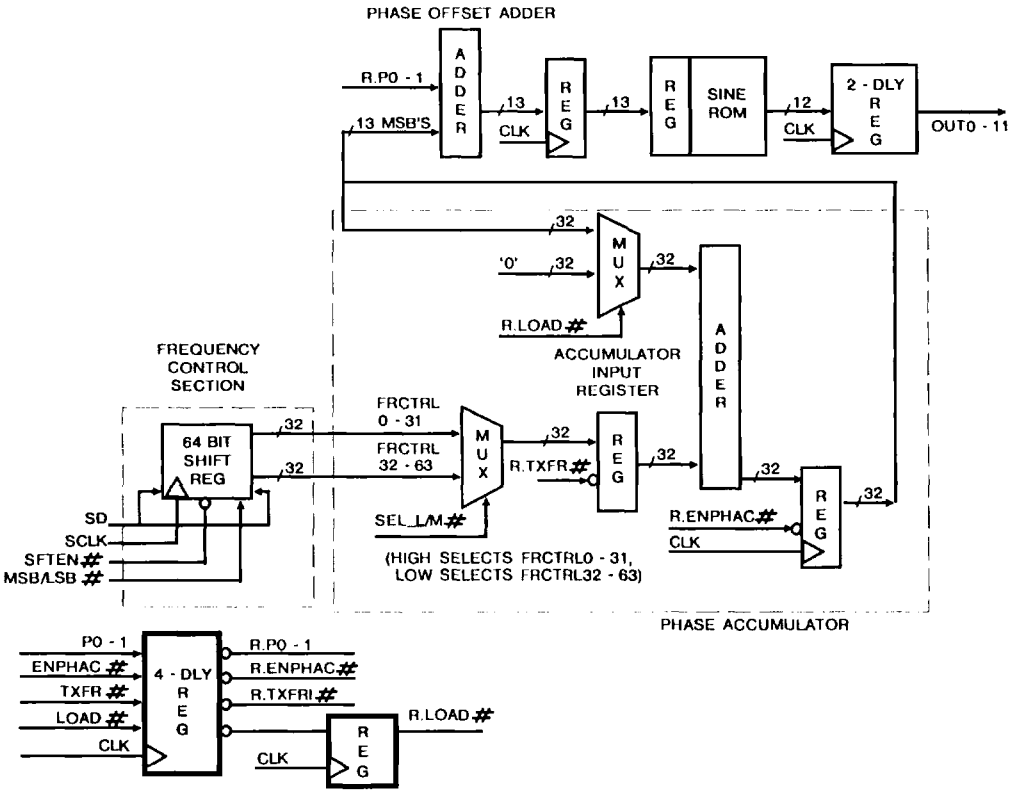


FIGURE 1. NCO-12 FUNCTIONAL BLOCK DIAGRAM

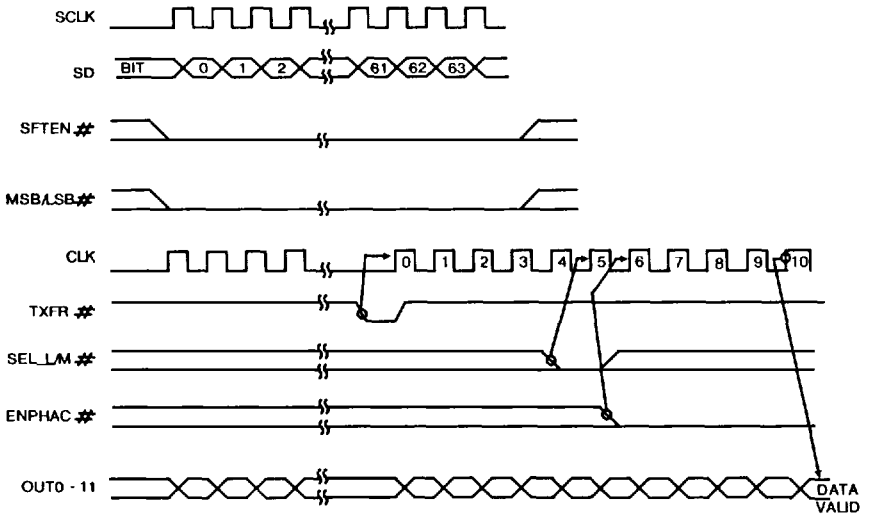


FIGURE 2. I/O TIMING

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output or I/O Voltage Applied ..... GND -0.5V to V_{CC} +0.5V
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C
ESD Classification ..... Class 1

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.75V to +5.25V
Operating Temperature Range ..... 0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = 5.25V
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = 4.75V
V_{IHC}	High Level Clock Input	3.0	-	V	V_{CC} = 5.25V
V_{ILC}	Low Level Clock Input	-	0.8	V	V_{CC} = 4.75V
V_{OH}	Output HIGH Voltage	2.6	-	V	I_{OH} = -400µA, V_{CC} = 4.75V
V_{OL}	Output LOW Voltage	-	0.4	V	I_{OL} = +2.0mA, V_{CC} = 4.75V
I_I	Input Leakage Current	-10	10	µA	V_{IN} = V_{CC} or GND, V_{CC} = 5.25V
I_O	I/O Leakage Current	-10	10	µA	V_{OUT} = V_{CC} or GND, V_{CC} = 5.25V
I_{CCSB}	Standby Power Supply Current	-	500	µA	V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Note 3
I_{CCOP}	Operating Power Supply Current	-	TBD	mA	f = 33MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.25V, Notes 1 and 3

Capacitance (T_A = +25°C, Note 2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance	-	10	pF	FREQ = 1MHz, V_{CC} = Open, All measurements are referenced to device ground
C_O	Output Capacitance	-	10	pF	

NOTES:

1. Power supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 10mA/MHz.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Output load per test load circuit with switch open and C_L = 40pF.

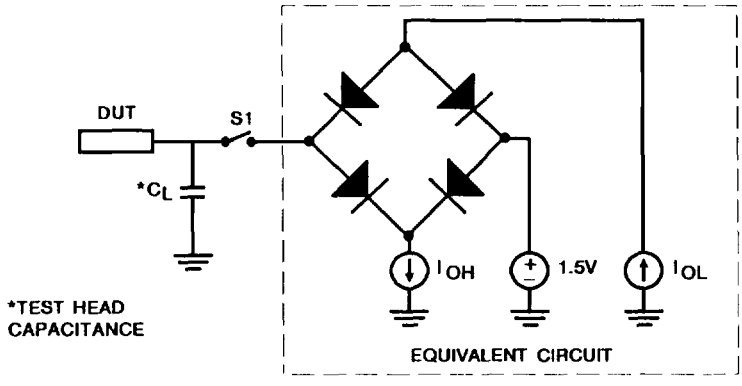
A.C. Electrical Specifications (Note 1)

SYMBOL	PARAMETER	-33 (33MHz)		-40 (40MHz)		-50 (50MHz)		COMMENTS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{CP}	Clock Period	30	-	25	-	20	-	ns
T_{CH}	Clock High	12	-	10	-	8	-	ns
T_{CL}	Clock Low	12	-	10	-	8	-	ns
T_{SW}	SCLK High/Low	16	-	14	-	13	-	ns
T_{DS}	Set-up Time SD to SCLK going high	15	-	13	-	12	-	ns
T_{DH}	Hold Time SD from SCLK going high	0	-	0	-	0	-	ns
T_{MS}	Set-up Time SFTEN#, MSB/LSB# to SCLK going high	18	-	15	-	12	-	ns
T_{MH}	Hold Time SFTEN#, MSB/LSB# from SCLK going high	0	-	0	-	0	-	ns
T_{SS}	Set-up Time SCLK high to CLK going high	23	-	20	-	15	-	ns, Note 2
T_{PS}	Set-up Time P0-1 to CLK going high	18	-	15	-	12	-	ns
T_{PH}	Hold Time P0-1 from CLK going high	0	-	0	-	0	-	ns
T_{ES}	Set-up Time LOAD#, TXFR#, ENPHAC#, SEL__L/M# to CLK going high	18	-	15	-	12	-	ns
T_{EH}	Hold Time LOAD#, TXFR#, ENPHAC#, SEL__L/M# from CLK going high	0	-	0	-	0	-	ns
T_{OH}	CLK to Output Delay	2	20	2	16	2	12	ns
T_{RF}	Output Rise, Fall Time	TBD	-	TBD	-	TBD	-	ns, Note 3

NOTES

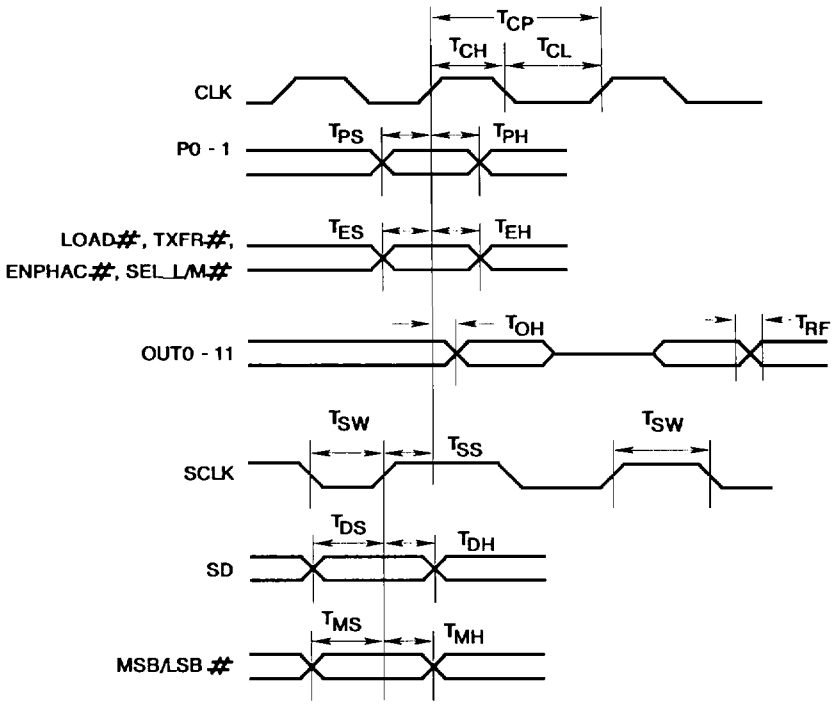
1. A.C. testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Input rise and fall times driven at 1ns/V. Output load per test load circuit with switch closed and C_L = 40 pF. Output transition is measured at $V_{OH} \geq 1.5V$ and $V_{OL} \leq 1.5V$.
2. If TXFR# is active, care must be taken to not violate set-up and hold times as data from the shift registers may not have settled before CLK occurs.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or design changes.

A.C. Test Load Circuit



Switch S1 open for I_{CCSB} and I_{CCOP}

Waveforms


TCP
TCH
TCL
CLK
TPS
TPH
P0 - 1
TES
TEH
LOAD#, TXFR#,
ENPHAC#, SEL_L/M#
TOH
TRF
OUT0 - 11
TSW
TSS
TSW
SCLK
TDS
TDH
SD
TMS
TMH
MSB/LSB #