DRAM

64K x 16 DRAM

STATIC COLUMN MODE, LOW POWER, EXTENDED REFRESH

NEW WIDE DRAM

FEATURES

- Industry standard x16 pinouts, timing, functions and packages
- High-performance, CMOS silicon-gate process
- Single +5V ±10% power supply
- All device pins are fully TTL compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional STATIC COLUMN MODE access cycle
- BYTE WRITE access cycle (MT4C1670 L only)
- NONPERSISTENT MASKED WRITE access cycle (MT4C1671 L only)
- 256 cycle extended refresh distributed across 32ms
- Low power, 1mW standby; 225mW active, typical

OPTIONS	MARKING
• Timing	
70ns access	- 7
80ns access	- 8
100ns access	-10
• Write Enable	
Byte or Word	MT4C1670 L
Word only	MT4C1671 L
• Mask Enable	
Not Available	MT4C1670 L
Always Available	MT4C1671 L
• Packages	
Plastic SOJ (400 mil)	DJ
Plastic TSOP (400 mil)	TG
Plastic ZIP (475 mil)	Z

NOTE: Available in die form Please consult factory for die data sheets.

- Part Number Example: MT4C1670DJ-7 L

GENERAL DESCRIPTION

The MT4C1670/1 L are randomly accessed solid-state memories containing 1,048,576 bits organized in a x16 configuration. The MT4C1670 L has both BYTE and WORD WRITE access cycles while the MT4C1671 L has only WORD WRITE access cycles.

The MT4C1670 L functions in a similar manner to the MT4C1671 L except that replacing $\overline{WE}$ with $\overline{WEL}$ and $\overline{WEH}$ allows for BYTE WRITE access cycles. $\overline{WEL}$ and $\overline{WEH}$ function in an identical manner to $\overline{WE}$: either $\overline{WEL}$ or $\overline{WEH}$ will generate an internal $\overline{WE}$ through an AND gate (Inverted NOR gate).

PIN ASSIGNMENT (Top View)

40-Pin SOJ (Q-6)

Vcc	1	40	Vss
DQ1	2	39	DQ16
DQ2	3	38	DQ15
DQ3	4	37	DQ14
DQ4	5	36	DQ13
DQ5	6	35	DQ12
DQ6	7	34	DQ11
DQ7	8	33	DQ10
DQ8	9	32	DQ9
NC	10	31	NC
Vcc	11	30	Vss
*NC/$\overline{WEH}$	12	29	$\overline{CAS}$
*$\overline{WE}$/$\overline{WEL}$	13	28	$\overline{OE}$
$\overline{RAS}$	14	27	NC
A0	15	26	NC
A1	16	25	NC
A2	17	24	A7
A3	18	23	A6
A4	19	22	A5
Vcc	20	21	Vss

40-Pin Zip (O-4)

NC	1	2	DQ9
DQ10	3	4	DQ11
DQ12	5	6	DQ13
DQ14	7	8	DQ15
DQ16	9	10	Vss
DQ1	11	12	DQ2
Vcc	13	14	DQ3
DQ4	15	16	DQ5
DQ6	17	18	DQ7
DQ8	19	20	NC
Vcc	21	22	*NC/$\overline{WEH}$
*$\overline{WE}$/$\overline{WEL}$	23	24	$\overline{RAS}$
A0	25	26	A1
A2	27	28	A3
A4	29	30	Vcc
NC	31	32	NC
Vss	33	34	A5
A6	35	36	A7
NC	37	38	$\overline{OE}$
$\overline{CAS}$	39	40	Vss

40-Pin TSOP (R-5)

Vcc	1	44	Vss
DQ1	2	43	DQ16
DQ2	3	42	DQ15
DQ3	4	41	DQ14
DQ4	5	40	DQ13
DQ5	6	39	DQ12
DQ6	7	38	DQ11
DQ7	8	37	DQ10
DQ8	9	36	DQ9
NC	10	35	NC
Vcc	13	32	Vss
*NC/$\overline{WEH}$	14	31	$\overline{CAS}$
*$\overline{WE}$/$\overline{WEL}$	15	30	$\overline{OE}$
$\overline{RAS}$	16	29	NC
A0	17	28	NC
A1	18	27	NC
A2	19	26	A7
A3	20	25	A6
A4	21	24	A5
Vcc	22	23	Vss

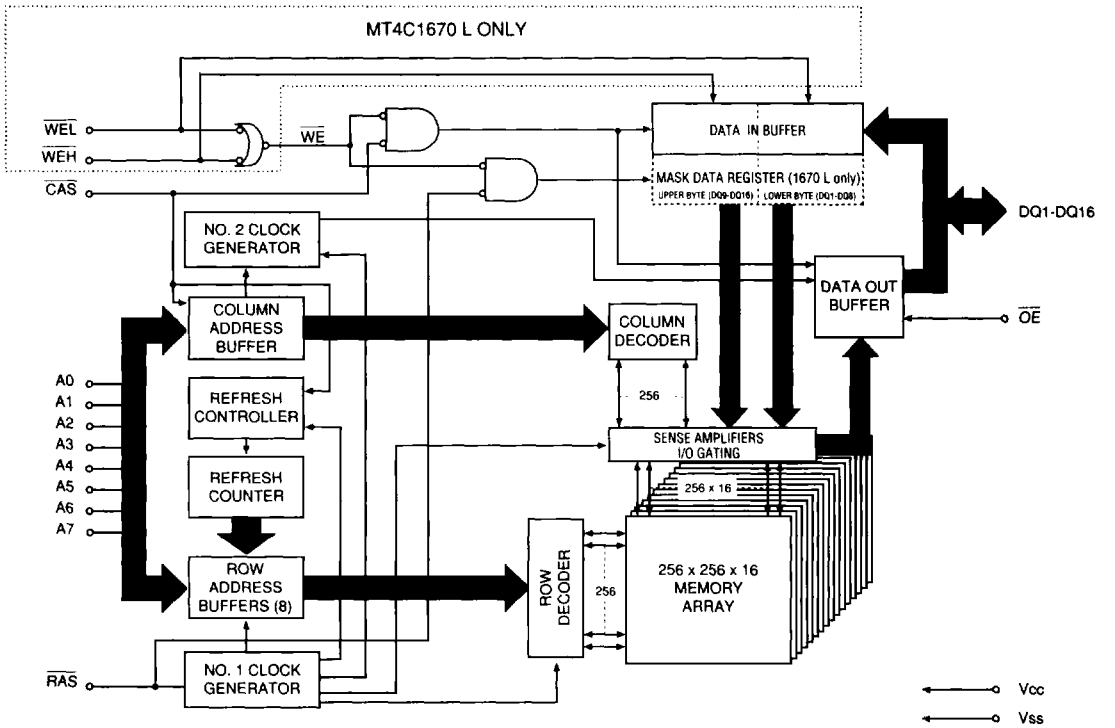
*MT4C1671 L/MT4C1670 L

The MT4C1670 L "$\overline{WE}$" function and timing are determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle: $\overline{WEL}$ transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) or $\overline{WEH}$ transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16).

The MT4C1671 L has NONPERSISTENT MASKED WRITE capability.

NEW WIDE DRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ PIN NUMBERS	ZIP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14	24	16	$\overline{RAS}$	Input	ROW Address Strobe: $\overline{RAS}$ is used to clock-in the 8 row address bits and strobe the $\overline{WEL}$, $\overline{WEH}$ and DQ inputs for the MASKED WRITE function.
29	39	31	$\overline{CAS}$	Input	Column Address Strobe: $\overline{CAS}$ is used to clock-in the 8 column address bits, enable the DRAM output buffers, and strobe the data inputs on WRITE cycles.
28	38	30	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WEL}$ and $\overline{WEH}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise the output buffers are in a High-Z state.
13	23	15	$\overline{WE}$/$\overline{WEL}$*	Input	Write Enable Lower Byte: $\overline{WEL}$ on MT4C1670 L is $\overline{WE}$ control for the DQ1 through DQ8 inputs. $\overline{WE}$ on MT4C1671 L controls DQ1 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. The DQ outputs for the byte not being written will remain in a High-Z state (byte WRITE cycle only).
12	22	14	NC/$\overline{WEH}$*	Input	Write Enable Upper Byte: $\overline{WEH}$ on MT4C1670 L is $\overline{WE}$ control for the DQ9 through DQ16 inputs. If ($\overline{WEL}$ or $\overline{WEH}$)/$\overline{WE}$ is LOW, the access is a WRITE cycle. This pin is a no connect on the MT4C1671 L as it has only WORD WRITE access cycles.
15-19, 22-24	25-29, 34-36	17-21, 24-26	A0-A7	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one 16-bit word out of the 64K available words.
2-9, 32-39,	11, 12, 14-17, 2, 18, 19, 3-9	2-9, 36-43	DQ1-DQ16	Input/ Output	Data I/O: For WRITE cycles, DQ1-DQ16 act as inputs to the addressed DRAM location. BYTE WRITEs can be performed by using $\overline{WEL}$ or $\overline{WEH}$ to select the byte to be written. For READ access cycles, DQ1-DQ16 act as outputs for the addressed DRAM ocation. All 16 I/Os are active for READ cycles (there is no BYTE READ cycle).
10, 25, 26, 27, 31	1, 20, 31, 32, 37	13, 27-29, 35	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 11, 20	13, 21, 30	1, 13, 22	Vcc	Supply	Power Supply: +5V ± 10%
21, 30, 40	10, 33, 40	23, 32, 44	Vss	Supply	Ground

NOTE: *MT4C1671 L/MT4C1670 L

NEW WIDE DRAM

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 16 address-bits during READ or WRITE cycles. These are entered 8 bits (A0-A7) at a time. $\overline{RAS}$ is used to latch the first 8 bits and $\overline{CAS}$ the latter 8 bits.

READ or WRITE cycles on the MT4C1671 L are selected with the $\overline{WE}$ input while either $\overline{WEL}$ or $\overline{WEH}$ perform the "$\overline{WE}$" on the MT4C1670 L. The MT4C1670 L "$\overline{WE}$" function is determined by the first BYTE WRITE ($\overline{WEL}$ or $\overline{WEH}$) to transition LOW and the last one to transition back HIGH.

A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ16. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by $\overline{OE}$, $\overline{WEL}$ and $\overline{WEH}$ (MT4C1670 L) or $\overline{WE}$ (MT4C1671 L).

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A7) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed-in by $\overline{RAS}$ followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled by holding $\overline{RAS}$ LOW and strobing-in different column addresses, thus executing faster memory cycles. Faster STATIC COLUMN WRITE cycles must have $\overline{CAS}$ or $\overline{WE}$ toggled strobing-in the different column addresses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE, $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$, or HIDDEN refresh) so that all 256 combinations of $\overline{RAS}$ addresses (A0-A7) are executed at least every 32ms, regardless of sequence. The $\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh cycle will also invoke the refresh counter and controller for row address control.

BATTERY BACKUP MODE (BBU) is a CBR refresh performed at the extended refresh rate with CMOS input levels. This mode provides a very low current, data retention cycle. $\overline{RAS}$ must be clocked by an external source during the BBU MODE or "SLEEP MODE".

BYTE WRITE ACCESS CYCLE (MT4C1670 L ONLY)

The BYTE WRITE mode is determined by the use of $\overline{WEL}$ and $\overline{WEH}$. Enabling $\overline{WEL}$ will select a lower BYTE WRITE cycle (DQ1-DQ8) while Enabling $\overline{WEH}$ will select an upper BYTE WRITE (DQ9-DQ16). Enabling both $\overline{WEL}$ and $\overline{WEH}$ selects a WORD WRITE cycle.

The MT4C1670 L may be viewed as two 64K x 8 DRAMS, which have common input controls, with the exception of the WE input. Figure 1 illustrates the MT4C1670 L BYTE and WORD WRITE cycles.

MASKED WRITE DESCRIPTION (MT4C1671 L ONLY)

Every WRITE access cycle may be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when mask data is supplied on the DQ pins and $\overline{WE}$ is LOW at $\overline{RAS}$ time. The MT4C1671 L is only word selectable when $\overline{WE}$ is LOW at $\overline{RAS}$ time (the MT4C1670 L does not have a MASKED WRITE cycle function).

The data (mask data) present on the DQ1-DQ16 inputs at $\overline{RAS}$ time will be written to an internal bit mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ16 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

New mask data must be supplied each time a MASKED WRITE cycle is initiated, even if the previous cycle's mask was the same mask.

Figure 2 illustrates the MT4C1671 L MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

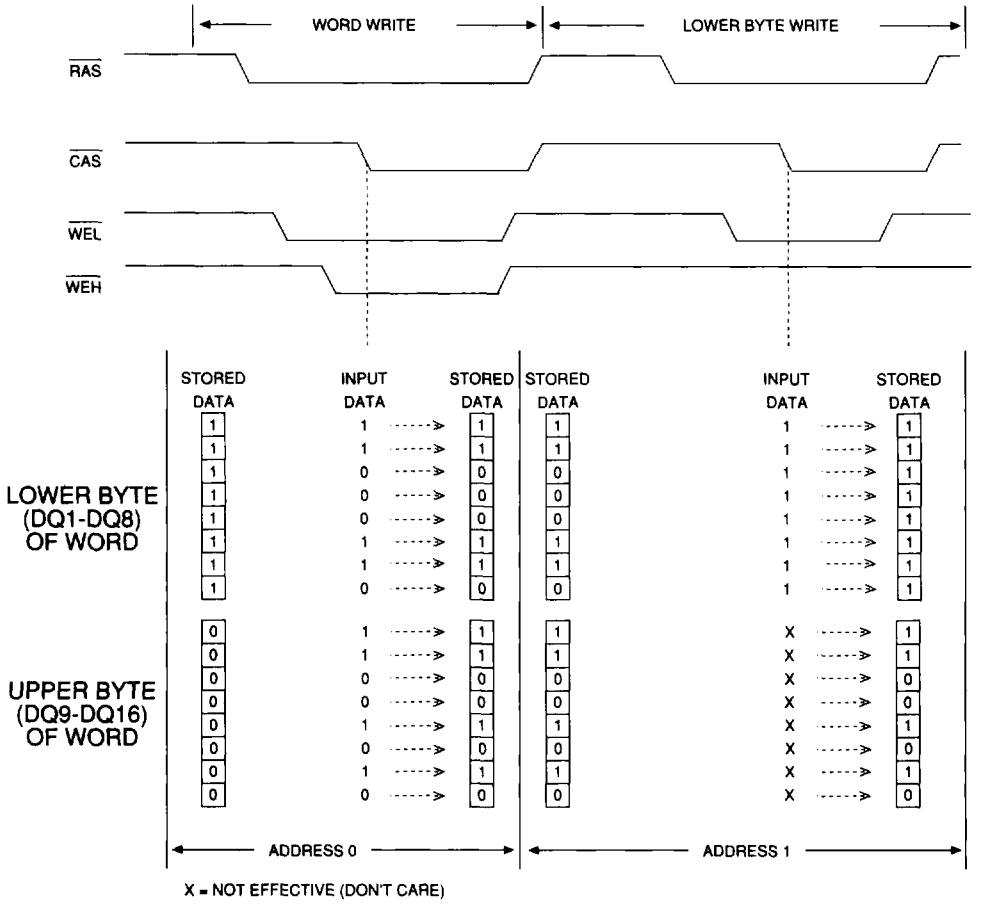


Figure 1
MT4C1670 L WORD AND BYTE WRITE EXAMPLE

NEW WIDE DRAM

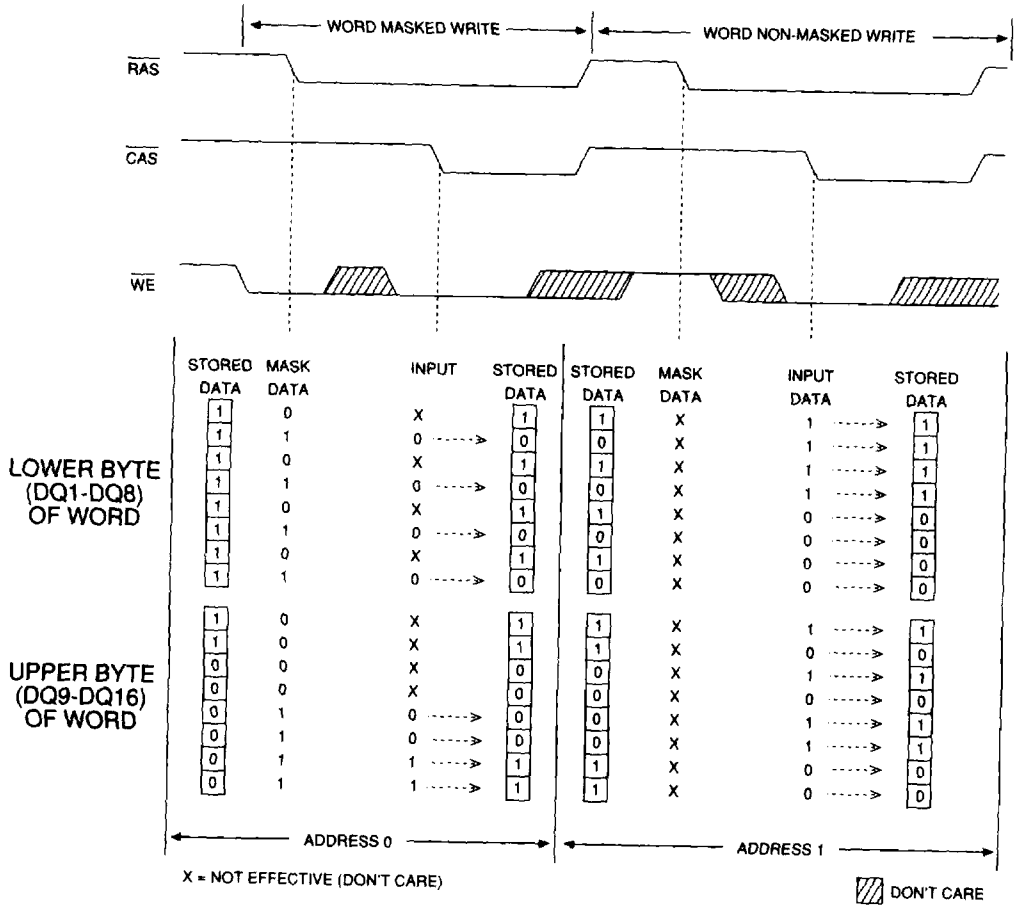


Figure 2
MT4C1671 L MASKED WRITE EXAMPLE

TRUTH TABLE: MT4C1670 L

FUNCTION		RAS	CAS	WEL	WEH	OE	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	X	High-Z	
READ		L	L	H	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	L	X	ROW	COL	Data In	
WRITE: LOWER BYTE (EARLY)		L	L	L	H	X	ROW	COL	Lower Byte, Data In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data In	
READ-WRITE		L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN READ	1st Cycle	L	L	H	H	L	ROW	COL	Data Out	
	2nd Cycle	L	L	H	H	L	n/a	COL	Data Out	
STATIC COLUMN EARLY-WRITE	1st Cycle	L	L	L	L	X	ROW	COL	Data In	1
	2nd Cycle	L	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN READ-WRITE	1st Cycle	L	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In	1
	2nd Cycle	L	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN REFRESH	READ	L→H→L	L	H	H	L	ROW	COL	Data Out	
	WRITE	L→H→L	L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	X	High-Z	

NOTE: 1. These cycles may also be BYTE WRITE cycles (either WEL or WEH active).
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

TRUTH TABLE: MT4C1671 L

FUNCTION		RAS	CAS	WE	OE	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data Out	
WRITE: WORD (EARLY-WRITE)		L	L	L	X	ROW	COL	Data In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
STATIC COLUMN	1st Cycle	L	L	H	L	ROW	COL	Data Out	
READ	2nd Cycle	L	L	H	L	n/a	COL	Data Out	
STATIC COLUMN	1st Cycle	L	L	L	X	ROW	COL	Data In	1
EARLY-WRITE	2nd Cycle	L	L	L	X	n/a	COL	Data In	1, 3
STATIC COLUMN	1st Cycle	L	L	H→L	L→H	ROW	COL	Data Out, Data In	1
READ-WRITE	2nd Cycle	L	L	H→L	L→H	n/a	COL	Data Out, Data In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data In	1, 2
RAS-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CAS-BEFORE-RAS REFRESH		H→L	L	X	X	X	X	High-Z	
BATTERY BACKUP REFRESH		H→L	L	X	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided. Refer to Figure 2.
2. EARLY-WRITE only.
3. Either CAS or WEL / WEH must latch in each additional column address and input data.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0V to +7.0V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 3, 4, 6, 7) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	1
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4	V_{CC}+1	V	1
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any Input 0V ≤ V_{IN} ≤ V_{CC} (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2.5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2.1mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	300	300	300	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC3}	120	115	90	mA	3, 4, 31
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tSC = ^tSC (MIN))	I_{CC4}	110	95	80	mA	3, 4, 31
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC (MIN))	I_{CC5}	120	115	90	mA	3, 31
REFRESH CURRENT: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC (MIN))	I_{CC6}	120	115	90	mA	3, 5
REFRESH CURRENT: BATTERY BACKUP (BBU) Average power supply current during BATTERY BACKUP refresh: $\overline{CAS}$ 0.2V or $\overline{CAS}$-BEFORE-$\overline{RAS}$ cycling; $\overline{RAS}$ = ^tRAS (MIN) to 1,000ns; $\overline{WE}$, A0-A9 and D_{IN} = V_{CC} - 0.2V or 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	400	400	400	µA	3, 5, 28

NEW WIDE DRAM

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A7	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$,($\overline{WEL}$, $\overline{WEH}$)/ $\overline{WE}$, $\overline{OE}$	C_{I2}		7	pF	2
Input/Output Capacitance: DQ	C_{IO}		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	^tRC	130		150		180		ns	
READ-WRITE cycle time	^tRWC	175		185		220		ns	
STATIC-COLUMN READ or WRITE cycle time	^tSC	45		50		55		ns	
STATIC-COLUMN READ-WRITE cycle time	^tSRWC	95		100		120		ns	
Access time from $\overline{RAS}$	^tRAC		70		80		100	ns	14
Access time from $\overline{CAS}$	^tCAC		25		35		40	ns	15
Output Enable time	^tOE		25		35		40	ns	
Access time from column address	^tAA		40		45		55	ns	
Access time from $\overline{CAS}$ precharge	^tCPA		45		50		55	ns	
$\overline{RAS}$ pulse width	^tRAS	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	^tRASC	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	^tRSH	20		35		40		ns	
$\overline{RAS}$ precharge time	^tRP	50		60		70		ns	
$\overline{CAS}$ pulse width	^tCAS	25	100,000	35	100,000	40	100,000	ns	
$\overline{CAS}$ hold time	^tCSH	70		80		100		ns	
$\overline{CAS}$ precharge time	^tCPN	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	^tCP	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	^tRCD	20	45	20	45	25	60	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	5		10		10		ns	
Row address setup time	^tASR	0		0		0		ns	
Row address hold time	^tRAH	10		12		15		ns	
$\overline{RAS}$ to column address delay time	^tRAD	15	35	17	40	20	55	ns	18
Column address setup time	^tASC	0		0		0		ns	
Column address hold time	^tCAH	15		15		20		ns	
Column address hold time (referenced to $\overline{RAS}$)	^tAR	55		60		70		ns	
Column address to $\overline{RAS}$ lead time	^tRAL	35		45		55		ns	
Read command setup time	^tRCS	0		0		0		ns	26
Read command hold time (referenced to $\overline{CAS}$)	^tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to $\overline{RAS}$)	^tRRH	0		10		10		ns	19
$\overline{CAS}$ to output in Low-Z	^tCLZ	0		0		0		ns	
Output buffer turn-off delay	^tOFF	0	20	0	20	0	20	ns	20, 30

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

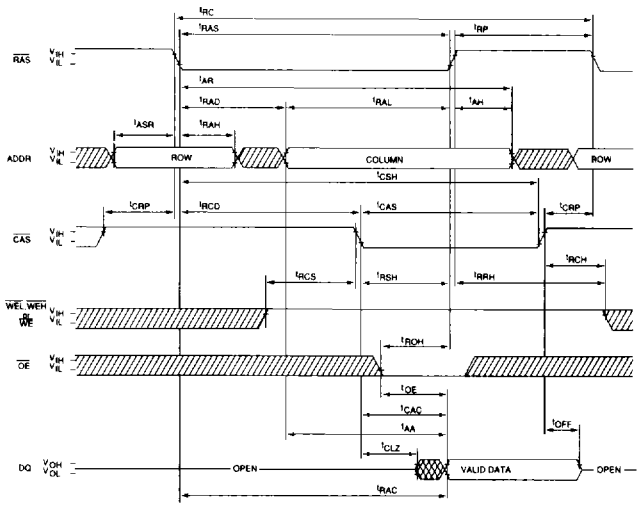
(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (0°C ≤ T_A ≤ +70°C; Vcc = 5V ± 10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Output Disable time	tOD		15		20		20	ns	30
Write command setup time	tWCS	0		0		0		ns	21, 26
Write command hold time	tWCH	15		15		20		ns	26
Write command hold time (referenced to $\overline{RAS}$)	tWCR	50		60		70		ns	26
Write command pulse width	tWP	15		15		20		ns	26
Write command to $\overline{RAS}$ lead time	tRWL	20		35		40		ns	26
Write command to $\overline{CAS}$ lead time	tCWL	20		35		40		ns	26
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	50		60		70		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	90		100		125		ns	21
Column address to $\overline{WE}$ delay time	tAWD	65		70		80		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	50		55		70		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (256 cycles)	tREF		32		32		32	ms	28
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		10		10		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time ($\overline{CAS}$-BEFORE-$\overline{RAS}$ refresh)	tCHR	15		25		30		ns	5
MASKED WRITE command to $\overline{RAS}$ setup time	tWRS	0		0		0		ns	26, 27
MASKED WRITE command to $\overline{RAS}$ hold time	tWRH	15		15		15		ns	26, 27
Mask data to $\overline{RAS}$ setup time	tMS	0		0		0		ns	26
Mask data to $\overline{RAS}$ hold time	tMH	15		15		15		ns	26
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	tOEH	10		20		20		ns	29
$\overline{OE}$ setup prior to $\overline{RAS}$ during HIDDEN REFRESH cycle	tORD	0		0		0		ns	
Last WRITE to column address delay	tLWAD	20	30	20	35	25	45	ns	
Access time from last WRITE	tALW	65		75		95		ns	
Output data enable from WRITE	tOW	tAA		tAA		tAA		ns	
Output data hold time from column address	tAOH	5		5		5		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	tROH	10		10		10		ns	
Column address hold time referenced to $\overline{RAS}$ HIGH	tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC-COLUMN mode	tCSC	tCAS		tCAS		tCAS		ns	
Write command inactive time	tWI	10		10		10		ns	

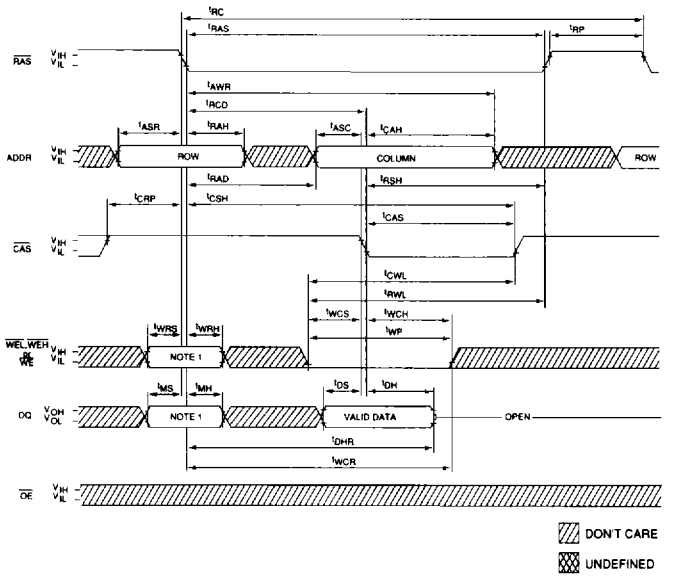
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-up should be repeated any time the 4ms refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 1 TTL gates and 50pF.
14. Assumes that $^tRCD < ^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq ^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out (Q) will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq ^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq ^tRWD$ (MIN), $^tAWD \geq ^tAWD$ (MIN) and $^tCWD \geq ^tCWD$ (MIN), the cycle is a LATE-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out are indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$ controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in early WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$=HIGH.
25. All other inputs at Vcc -0.2V.
26. WRITE command is defined as either $\overline{WEL}$ or $\overline{WEH}$ or both going LOW on the MT4C1670 L. WRITE command is defined as $\overline{WE}$ going LOW on the MT4C1671 L.
27. Must be held LOW to ensure MASKED WRITE is enabled and must be held HIGH to ensure MASKED WRITE is disabled.
28. BBU current is reduced as ^tRAS is reduced from its maximum specification during the BBU cycle.
29. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after ^tOEH is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
30. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH first, $\overline{OE}$ becomes a "don't care." If $\overline{OE}$ goes HIGH and $\overline{CAS}$ stays LOW, $\overline{OE}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{OE}$ is taken back LOW (while $\overline{CAS}$ remains LOW).
31. Column address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.

READ CYCLE



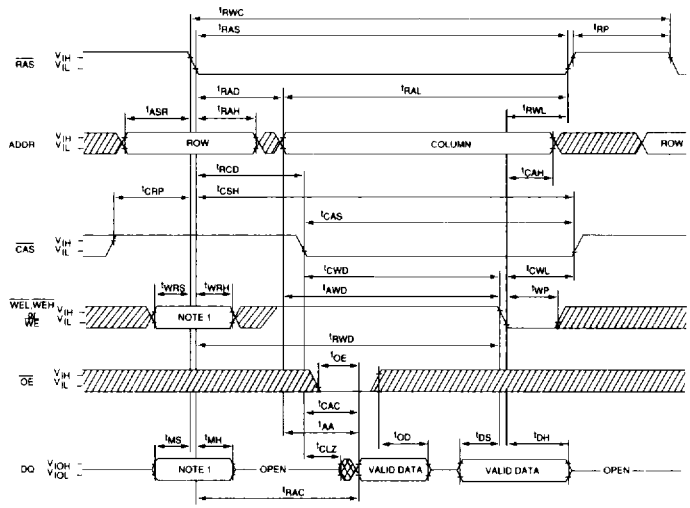
EARLY-WRITE CYCLE



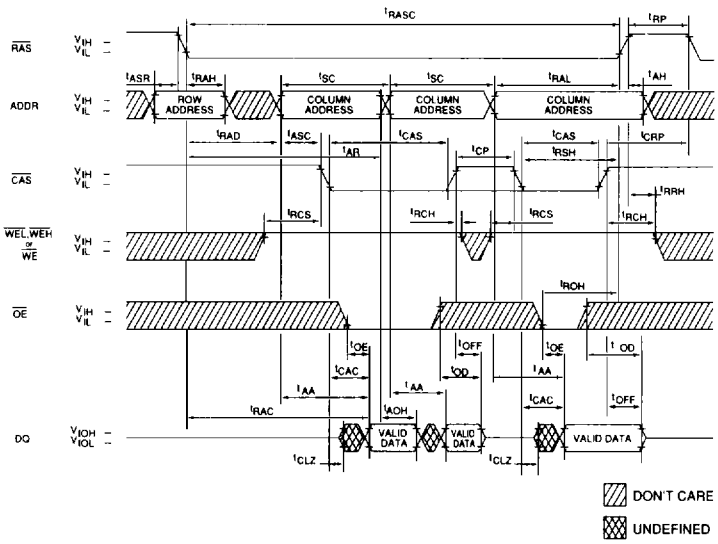
NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

NEW WIDE DRAM

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

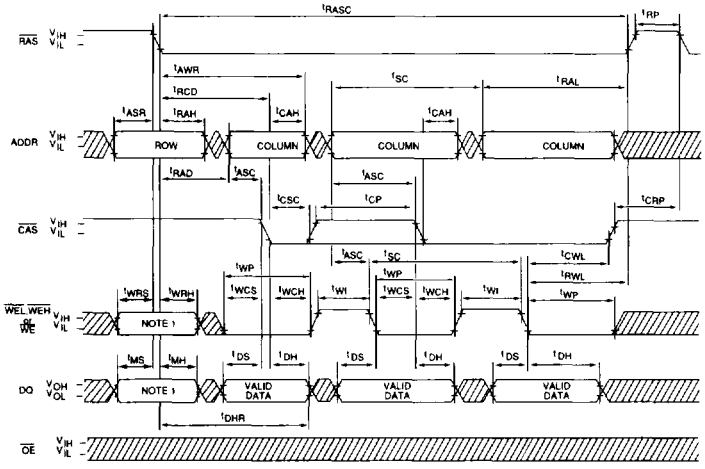


STATIC-COLUMN READ CYCLE

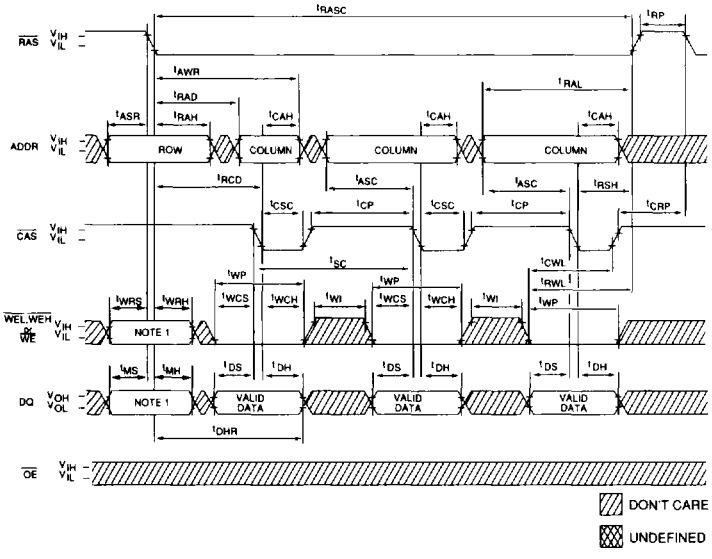


NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

STATIC-COLUMN EARLY-WRITE CYCLE
(WE CONTROLLED)



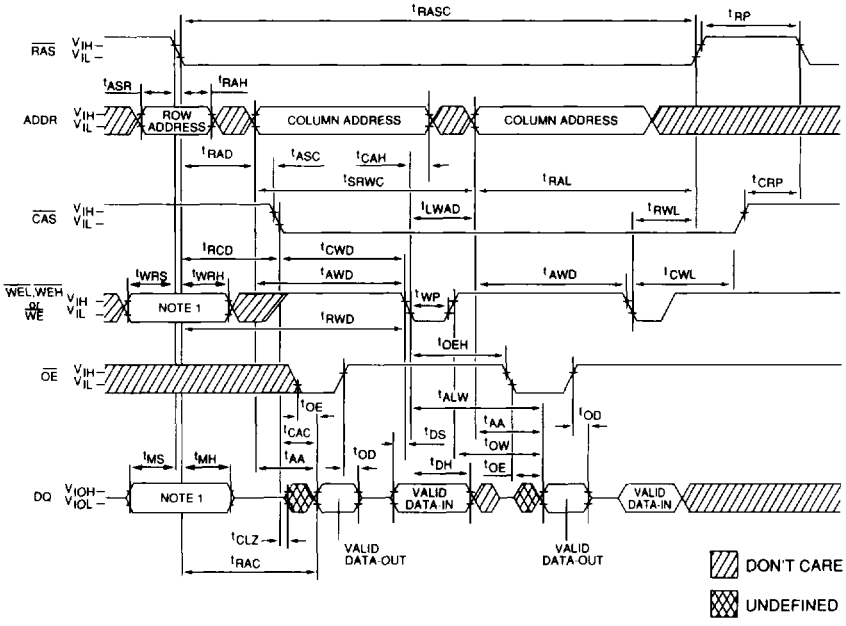
STATIC-COLUMN EARLY-WRITE CYCLE
(CAS CONTROLLED)



NOTE: 1. Applies to MT4C1671 L only; WEL, WEH and DQ inputs on MT4C1670 L are "don't care" at RAS time. WE selects between normal WRITE and MASKED WRITE at RAS time. The DQ inputs are "don't care" for a normal WRITE, WE HIGH at RAS time. The DQ inputs provide the mask data at RAS time for a MASKED WRITE, WE LOW at RAS time.

NEW WIDE DRAM

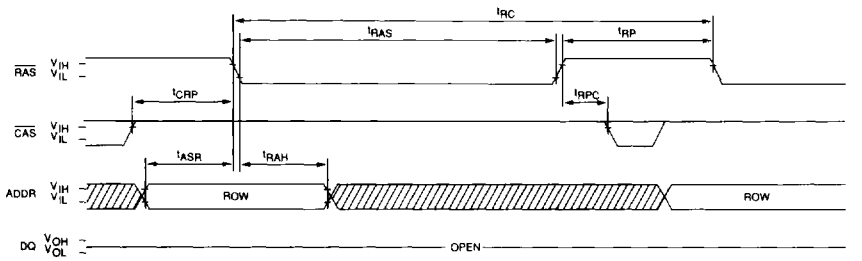
STATIC-COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



NOTE: 1. Applies to MT4C1671 L only; $\overline{WEL}$, $\overline{WEH}$ and DQ inputs on MT4C1670 L are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE, $\overline{WE}$ HIGH at $\overline{RAS}$ time. The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

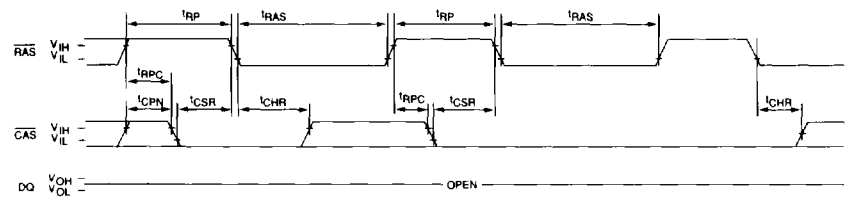
RAS-ONLY REFRESH CYCLE

(ADDR = A0-A7, OE; WEL, WEH or WE = DON'T CARE)



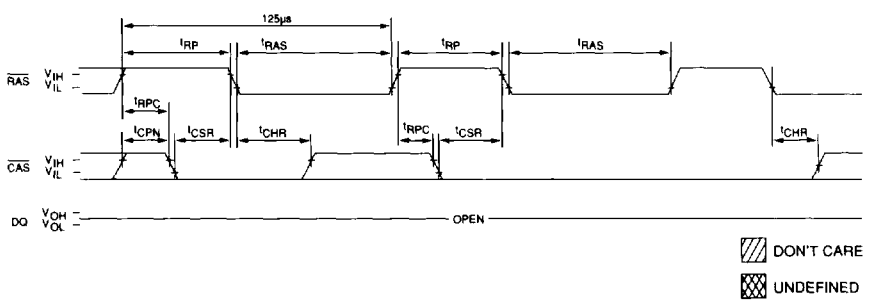
CAS-BEFORE-RAS REFRESH CYCLE

(A0-A7; WEL, WEH or WE, and OE = DON'T CARE)



BATTERY BACKUP REFRESH CYCLE

(A0-A7; WEL, WEH or WE, and OE = DON'T CARE)



NEW WIDE DRAM

HIDDEN REFRESH CYCLE [24]

($\overline{WEL}$, $\overline{WEH}$ or $\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)