Two Modulus Prescaler

Military 12509

ELECTRICALLY TESTED PER:
5962-8774801

The 12509 is a two-modulus prescaler which will divide by 5 and 6. A MECL-to-MTTL translator is provided to interface with the 12514 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 600 MHz (Typ) Toggle Frequency
- 12509 (÷ 5/6)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- + 5.0 or – 5.2 V Operation *
- Buffered Clock Input — Series-Input RC Typ, 20 Ohms and 4.0 pF
- V_{BB} Reference Voltage
- 460 mW Max/Pkg (No Load)

AVAILABLE AS

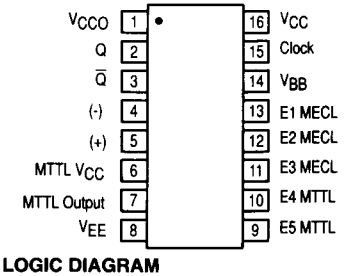
1) JAN: N/A
2) SMD: 5962-8774801
3) 883: 12509/BXAJC

X = CASE OUTLINE AS FOLLOWS:

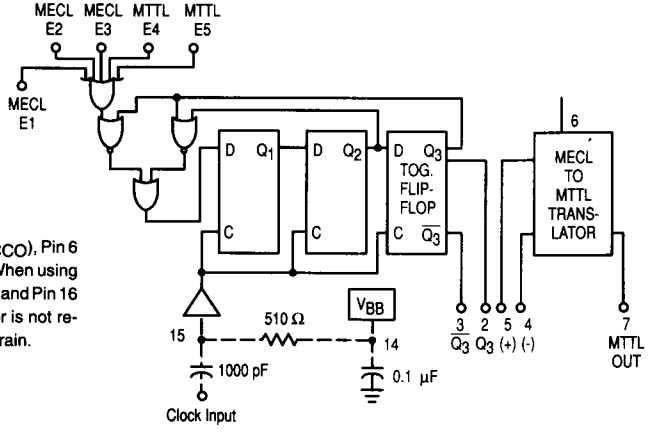
PACKAGE: CERDIP: E

PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CCO}	1	GND
Q	2	51 Ω to V_{TT}
$\overline{Q}$	3	51 Ω to V_{TT}
(-)	4	51 Ω to V_{TT}
(+)	5	GND
MTTL V_{CC}	6	GND
MTTL Output	7	51 Ω to V_{TT}
V_{EE}	8	V_{EE}
E5 MTTL	9	GND
E4 MTTL	10	GND
E3 MECL	11	51 Ω to V_{TT}
E2 MECL	12	51 Ω to V_{TT}
E1 MECL	13	51 Ω to V_{TT}
V_{BB}	14	OPEN
Clock	15	51 Ω to V_{TT}
V_{CC}	16	GND



LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

* When using a + 5.0 V supply, apply + 5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using –5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply 5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

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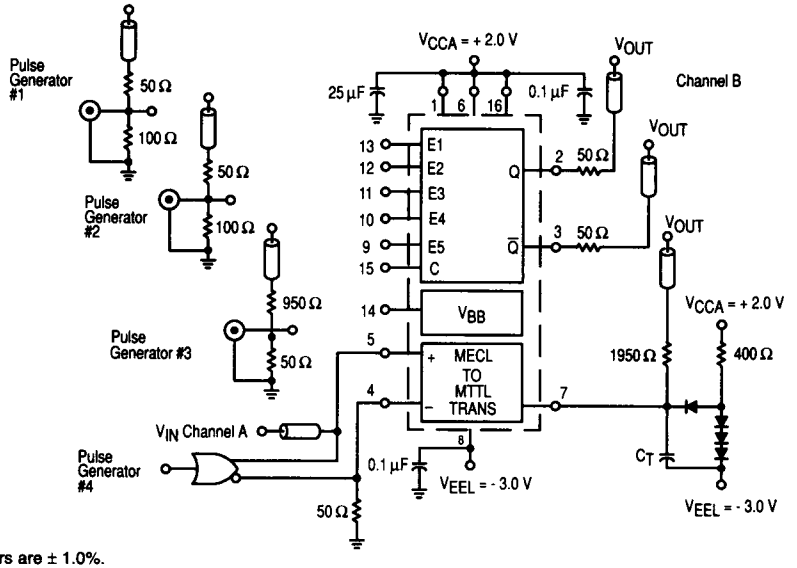
ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+ 7.0	Vdc
Output Voltage	V_{OUT}		+ 5.5	Vdc
Input Voltage	V_{IN}		+ 5.5	Vdc
Operating Temperature Range	T_A	− 55	+ 125	°C
Storage Temperature Range	T_{stg}	− 65	+ 165	°C



NOTES

1. All resistors are ± 1.0%.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
3. The 1950 Ω resistor at pin 7 and the scope termination impedance constitute a 40:1 attenuator probe.
4. All unused outputs must be terminated with 100 Ω to ground.
5. Pulse generator 1, 2, and 4 have the following characteristics:
   a) PRF = 10 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 2.0$ ns ± 0.2 ns.
6. Pulse generator 3 has the following characteristics:
   a) PRF = 2.0 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 5.0$ ns ± 0.5 ns.

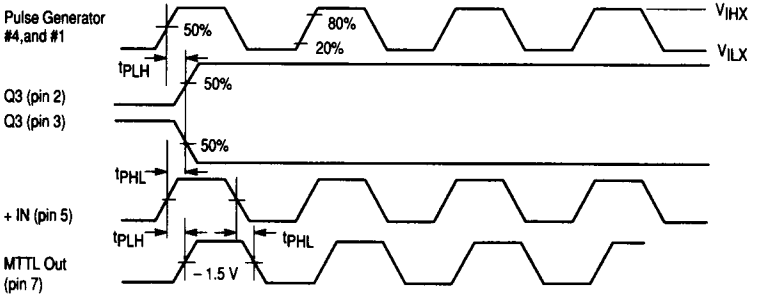


Figure 1. Switching Test Circuit and Waveforms

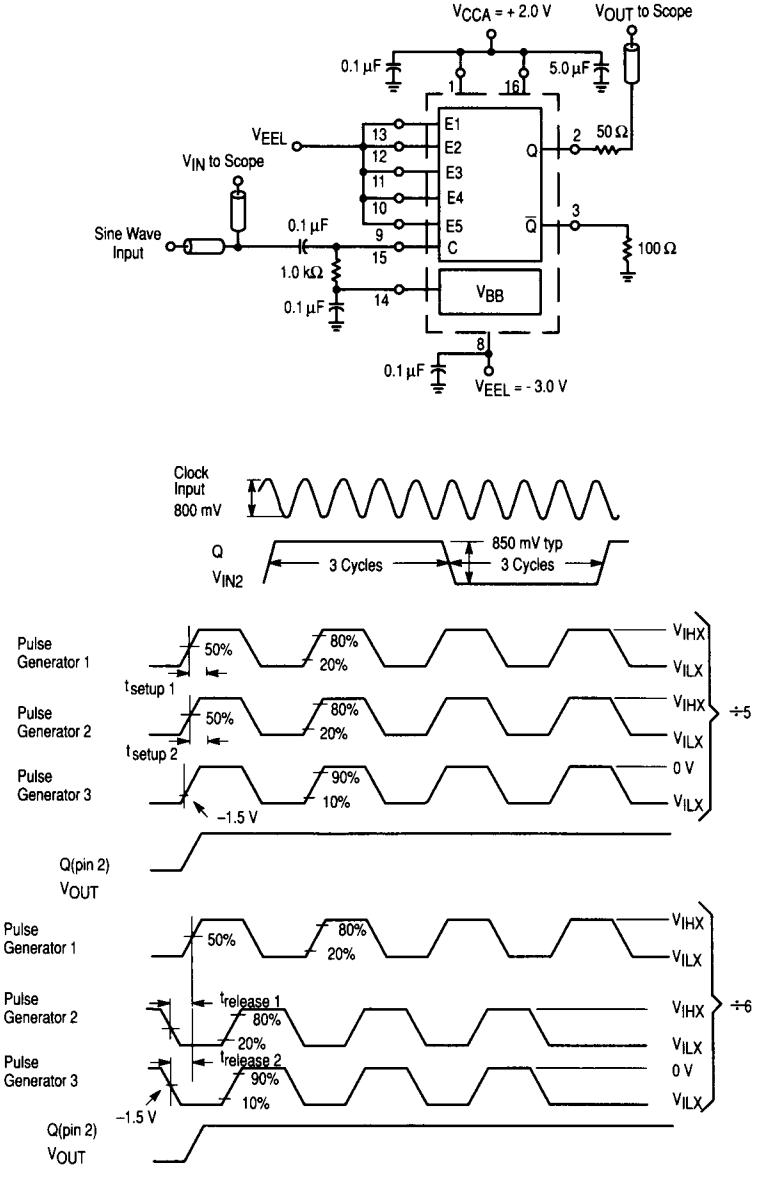


Figure 2. Switching Test Circuit and Waveforms

Sequence Table 1

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS						
TTL 9	TTL 10	ECL 10	ECL 12	ECL 13	ECL 15	
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	+6
V_{IH}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IH}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IL}	V_{IHB}	V_{ILB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IL}	V_{ILB}	V_{IHB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{IHB}	C_{P1}	+5

Sequence Table 2

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS						
TTL 9	TTL 10	ECL 11	ECL 12	ECL 13	ECL 15	
V_{ILT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	6
V_{IL}	V_{ILT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	6
V_{IL}	V_{IL}	V_{ILA}	V_{ILB}	V_{ILB}	C_{P1}	6
V_{IL}	V_{IL}	V_{ILB}	V_{ILA}	V_{ILB}	C_{P1}	6
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILA}	C_{P1}	6
V_{IHT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	5
V_{IL}	V_{IHT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	5
V_{IL}	V_{IL}	V_{IHA}	V_{ILB}	V_{ILB}	C_{P1}	5
V_{IL}	VIL	V_{ILB}	V_{IHA}	V_{ILB}	C_{P1}	5
V_{IL}	VIL	V_{ILB}	V_{ILB}	V_{IHA}	C_{P1}	5

State Diagram

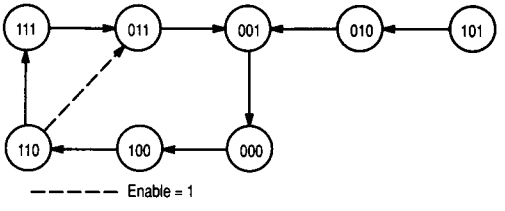
6

Enable = 0

Q_1	Q_2	Q_3
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0

Enable = 1

NOTE: The state of the enable is important only for the positive clock transition when the counter is in the state 110.



12509
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)														Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	C_{P1}	$I_{OH/OL}$	P.U.T.
V_{OH1}	Output Voltage High	4.03	4.22	4.135	4.37	3.88	4.12	V	9, 10	[1]9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 2)
V_{OH2}	Output Voltage High	2.70	4.22	3.00	4.37	2.40	4.12	V			5	4	6	8		7 I_{OH}	7
V_{OL1}	Output Voltage Low	3.11	3.44	3.14	3.515	3.04	3.405	V	9, 10	9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 2)
V_{OL2}	Output Voltage Low	0.10	0.80	0.10	0.66	0.10	1.00	V			4	5	6	8		7 I_{OL}	7
V_{OHA}	Output Voltage High	4.01	4.22	4.115	4.37	3.86	4.12	V		9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 3)
V_{OLA}	Output Voltage Low	3.11	3.46	3.14	3.535	3.04	3.425	V		9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 3)
V_{BB1}	Reference Bias Supply Voltage	3.67	3.87					V					1, 16	8		14	14
I_{OS}	Output Short Circuit Current	- 65	- 20	- 65	- 20	- 65	- 20	mA		7	5	5	6	8			7
I_{CC1}	Power Supply Current	- 80	- 10	- 80	- 10	- 88	- 10	mA					1, 16	8			8
I_{CC2}	Power Supply Current	0.5	5.2	0.5	5.2	0.5	5.2	mA			4	4	6	8			6

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.
2. See sequence table 1.
3. See sequence table 2.

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Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
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		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	P.U.T.
I_{INH1}	Input Current High		250		400		400	µA		9, 10	11 - 13, 15		1, 16	8	11, 12, 13, 15
I_{INH2}	Input Current High	2.0	6.0	2.0	6.4	1.7	6.0	mA			4, 5	4, 5	6	8	4, 5
I_{INH3}	Input Current High	1.0	3.0	1.0	3.6	0.7	3.0	mA			5	5	6	8	5
I_{INH4}	Input Current High		100		100		100	µA	9, 10				1, 16	8	9, 10
I_{INI1}	Input Current Low	- 10		- 10		- 10		µA					1, 16	8, 15, 11 - 13	11, 12, 13, 15
I_{INI1}	Input Current Low	- 1.6		- 1.6		- 1.6		mA		9, 10			1, 16	8	9, 10

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.

* **ELECTRICAL CHARACTERISTICS**: This device is designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 Ω resistor to + 3.0 V.

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T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
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		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
t_{PLH}	Propagation Delay	4.8	8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	1, 16	8	2, 3
t_{PHL}	Propagation Delay	4.8	7.5		8.7		7.5	ns	9, 10	11 - 13	15	2, 3	1, 16	8	2, 3
t_{PLH}	Propagation Delay	3.4	8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	1, 16	8	7
t_{PHL}	Propagation Delay	3.0	6.5		7.6		6.5	ns	9, 10	11 - 13	15	2, 3	1, 16	8	7
		Min	Typ	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
$t_{Setup\ 1}$	Setup Time MECL	5.0	2.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Setup\ 2}$	Setup Time MTTL	5.0	3.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Rel\ 1}$	Release Time MECL	5.0	2.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Rel\ 2}$	Release Time MTTL	5.0	3.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
		Min	Typ	Min	Typ	Min	Typ		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
$f_{max} + 6$	Toggle Frequency	480	520	420	440	420	500	MHz			15	2	1, 6, 16	8 - 13	2