

## General Description

The MIC4467/8/9 family of 4-output CMOS buffer/drivers is an expansion from the earlier single- and dual-output drivers, to which they are functionally closely related. Because package pin count permitted it, each driver has been equipped with a 2-input logic gate for added flexibility. Placing four high-power drivers in a single package also improves system reliability and reduces total system cost. In some applications, one of these drivers can replace not only two packages of single-input drivers, but some of the associated logic as well.

Although primarily intended for driving power MOSFETs, and similar highly capacitive loads, these drivers are equally well suited to driving any other load (capacitive, resistive, or inductive), which requires a high-efficiency, low-impedance driver capable of high peak currents, rail-to-rail voltage swings, and fast switching times. For example, heavily loaded clock lines, coaxial cables, and piezoelectric transducers can all be

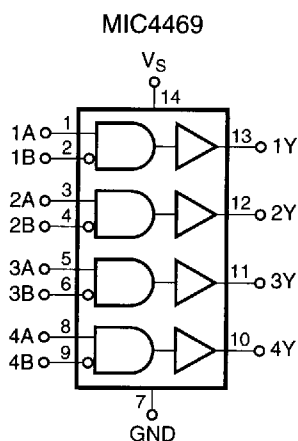
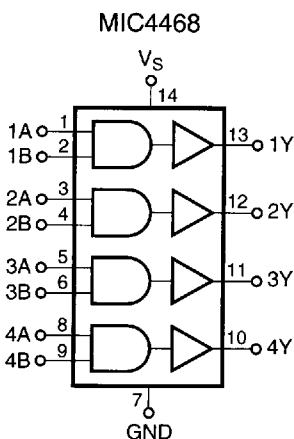
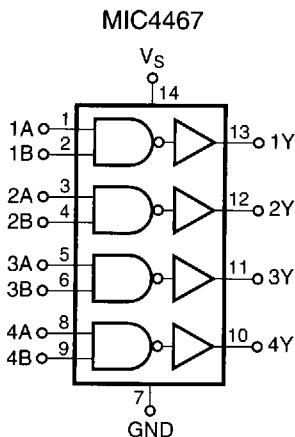
## Features

- Built using reliable, low power CMOS processes
- Latchproof. Withstands 500mA Inductive Kickback
- 3 Input Logic Choices
- Symmetrical Rise and Fall Times ..... 25ns
- Short, Equal Delay Times ..... 75ns
- High Peak Output Current ..... 1.2A
- Wide Operating Range ..... 4.5 to 18V
- Low Equivalent Input Capacitance (typ) ..... 6pF
- Inputs = Logic 1 for Any Input From 2.4V to  $V_S$
- ESD Protected

## Applications

- General-Purpose CMOS Logic Buffer
- Driving All 4 MOSFETs in an H-Bridge
- Direct Small-Motor Driver
- Relay or Peripheral Drivers
- Dual Differential Output Power Drivers
- CCD Driver
- Pin-Switching Network Driver

## Logic Diagrams



driven easily with MIC446X series drivers. The only limitation on loading is that total power dissipation in the IC must be kept within the power dissipation limits of the package.

The MIC446X series drivers are built using a BCD process. They will not latch under any conditions within their power and

voltage ratings. They are not subject to damage when up to 5V of noise spiking (either polarity) occurs on the ground line. They can accept up to half an amp of inductive kickback current (either polarity) into their outputs without damage or logic upset.

## Ordering Information

| Part No.    | Package            | Temp. Range    |
|-------------|--------------------|----------------|
| MIC44**CN   | 14-Pin Plastic DIP | 0° to +70°C    |
| MIC44**CWM  | 16-Pin Wide SOIC   | 0° to +70°C    |
| MIC44**BN   | 14-Pin Plastic DIP | -40° to +85°C  |
| MIC44**BWM  | 16-Pin Wide SOIC   | -40° to +85°C  |
| MIC44**BJ   | 14-Pin CerDIP      | -40° to +85°C  |
| MIC44**AJB* | 14-Pin CerDIP      | -55° to +125°C |
| MIC44**AL   | 20-Pin LCC         | -55° to +125°C |
| MIC44**CY   | Die                | 0° to +70°C    |

\* AJB indicates units screened to MIL-STD 883, Method 5004, condition B, and burned-in for 1-week.

\*\*Two digits must be added in this position to define the device logic:

67 — NAND

68 — AND

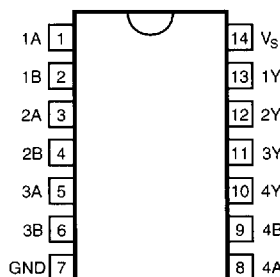
69 — AND with one inverting input

## Truth Table

| Part No.                 | Inputs |   | Output Y |
|--------------------------|--------|---|----------|
|                          | A      | B |          |
| MIC4467<br>(Each Driver) | L      | X | H        |
|                          | X      | L | H        |
|                          | H      | H | L        |
| MIC4468<br>(Each Driver) | H      | H | H        |
|                          | L      | X | L        |
|                          | X      | L | L        |
| MIC4469<br>(Each Driver) | L      | X | L        |
|                          | X      | H | L        |
|                          | H      | L | H        |

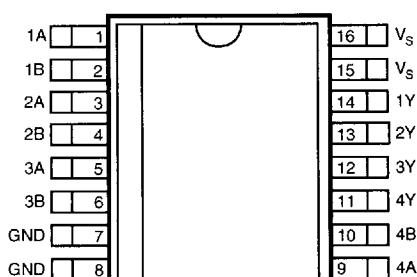
## Pin Configurations

14-Pin Dual-In-Line Package - N, J



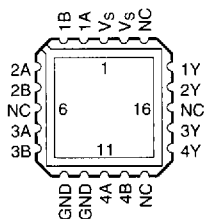
TOP VIEW

16-Pin Wide SOIC - WM

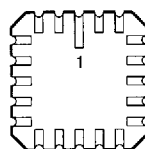


TOP VIEW

20-Pin LCC - L



TOP VIEW



BOTTOM VIEW

**Absolute Maximum Ratings (Notes 1 and 2)**

|                                                  |                |                                                |         |
|--------------------------------------------------|----------------|------------------------------------------------|---------|
| Supply Voltage                                   | 22V            | Power Dissipation                              |         |
| Input Voltage (GND – 5V) to ( $V_S + 0.3V$ )     |                | P Package (14-Pin Plastic DIP)                 | 1.5W    |
| Maximum Chip Temperature                         |                | WM Package (16-Pin Wide SOIC)                  | 1W      |
| Operating                                        | 150°C          | J Package (14-Pin CerDIP)                      | 1.25W   |
| Storage                                          | –65° to +150°C | L Package (20-Pin LCC)                         | 1W      |
| Maximum Load Temperature (10 sec, for soldering) | 300°C          | Package Thermal Resistance                     |         |
| Operating Ambient Temperature                    |                | P Package (14-Pin Plastic DIP) $R_{\theta JA}$ | 80°C/W  |
| C Version                                        | 0° to +70°C    | WM Package (16-Pin Wide SOIC) $R_{\theta JA}$  | 120°C/W |
| B Version                                        | –40° to +85°C  | J Package (14-Pin CerDIP) $R_{\theta JA}$      | 100°C/W |
| A Version                                        | –55° to +125°C | L Package (20-Pin LCC) $R_{\theta JA}$         | 120°C/W |

**Electrical Characteristics:** Measured at  $T_A = 25^\circ\text{C}$  with  $4.5V \leq V_S \leq 18V$  unless otherwise specified.

| Symbol                | Parameter                                        | Conditions                            | Min          | Typ | Max  | Units         |
|-----------------------|--------------------------------------------------|---------------------------------------|--------------|-----|------|---------------|
| <b>INPUT</b>          |                                                  |                                       |              |     |      |               |
| $V_{IH}$              | Logic 1 Input Voltage                            |                                       | 2.4          | 1.3 |      | V             |
| $V_{IL}$              | Logic 0 Input Voltage                            |                                       |              | 1.2 | 0.8  | V             |
| $I_{IN}$              | Input Current                                    | $0 \leq V_{IN} \leq V_S$              | –1           |     | 1    | $\mu\text{A}$ |
| <b>OUTPUT</b>         |                                                  |                                       |              |     |      |               |
| $V_{OH}$              | High Output Voltage                              | $I_{LOAD} = 10\text{mA}$              | $V_S - 0.15$ |     |      | V             |
| $V_{OL}$              | Low Output Voltage                               | $I_{LOAD} = 10\text{mA}$              |              |     | 0.15 | V             |
| $R_O$                 | Output Resistance                                | $I_{OUT} = 10\text{mA}$ , $V_S = 18V$ |              | 5   | 15   | $\Omega$      |
| $I_{PK}$              | Peak Output Current                              |                                       |              | 1.2 |      | A             |
| I                     | Latch-Up Protection<br>Withstand Reverse Current |                                       | >500         |     |      | mA            |
| <b>SWITCHING TIME</b> |                                                  |                                       |              |     |      |               |
| $t_R$                 | Rise Time                                        | Test Figure 1                         |              | 14  | 25   | ns            |
| $t_F$                 | Fall Time                                        | Test Figure 1                         |              | 13  | 25   | ns            |
| $t_{D1}$              | Delay Time                                       | Test Figure 1                         |              | 30  | 75   | ns            |
| $t_{D2}$              | Delay Time                                       | Test Figure 1                         |              | 45  | 75   | ns            |
| <b>POWER SUPPLY</b>   |                                                  |                                       |              |     |      |               |
| $I_S$                 | Power Supply Current<br>Supply                   |                                       |              | 0.2 | 4    | mA            |

**Electrical Characteristics:**

Measured over operating temperature range with  $4.5V \leq V_S \leq 18V$  unless otherwise specified.

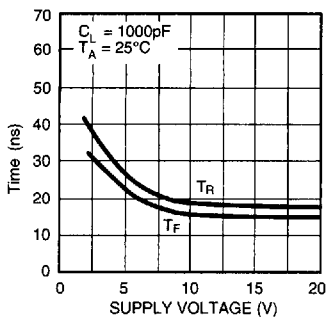
| Symbol                | Parameter                                        | Conditions                             | Min         | Typ | Max | Units    |
|-----------------------|--------------------------------------------------|----------------------------------------|-------------|-----|-----|----------|
| <b>INPUT</b>          |                                                  |                                        |             |     |     |          |
| $V_{IH}$              | Logic 1 Input Voltage                            |                                        | 2.4         | 1.4 |     | V        |
| $V_{IL}$              | Logic 0 Input Voltage                            |                                        |             | 1.0 | 0.8 | V        |
| $I_{IN}$              | Input Current                                    | $0 \leq V_{IN} \leq V_S$               | -1          |     | 1   | $\mu A$  |
| <b>OUTPUT</b>         |                                                  |                                        |             |     |     |          |
| $V_{OH}$              | High Output Voltage                              | $I_{LOAD} = 10\text{ mA}$              | $V_S - 0.3$ |     |     | V        |
| $V_{OL}$              | Low Output Voltage                               | $I_{LOAD} = 10\text{ mA}$              |             |     | 0.3 | V        |
| $R_O$                 | Output Resistance                                | $I_{OUT} = 10\text{ mA}$ , $V_S = 18V$ |             | 7   | 30  | $\Omega$ |
| $I_{PK}$              | Peak Output Current                              |                                        |             | 1.2 |     | A        |
| $I$                   | Latch-Up Protection<br>Withstand Reverse Current |                                        | 500         |     |     | mA       |
| <b>SWITCHING TIME</b> |                                                  |                                        |             |     |     |          |
| $t_R$                 | Rise Time                                        | Test Figure 1                          |             | 17  | 50  | ns       |
| $t_F$                 | Fall Time                                        | Test Figure 1                          |             | 16  | 50  | ns       |
| $t_{D1}$              | Delay Time                                       | Test Figure 1                          |             | 35  | 100 | ns       |
| $t_{D2}$              | Delay Time                                       | Test Figure 1                          |             | 55  | 100 | ns       |
| <b>POWER SUPPLY</b>   |                                                  |                                        |             |     |     |          |
| $I_S$                 | Power Supply Current<br>Supply                   |                                        |             | 0.4 | 8   | mA       |

**NOTE 1:** Functional operation above the absolute maximum stress ratings is not implied.

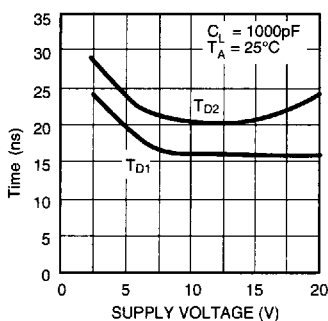
**NOTE 2:** Static sensitive device. Store only in conductive containers. Handling personnel and equipment should be grounded to prevent static damage.

# Typical Characteristics

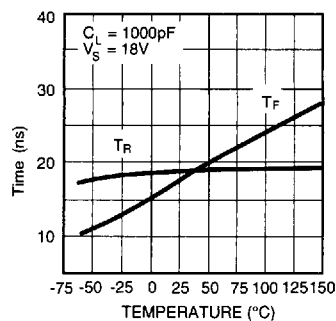
**Rise and Fall Time vs. Supply Voltage**



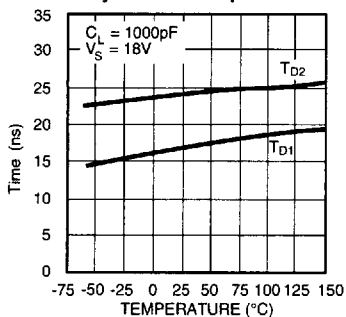
**Delay Time vs. Supply Voltage**



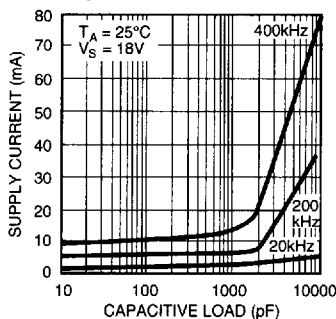
**Rise and Fall Time vs. Temperature**



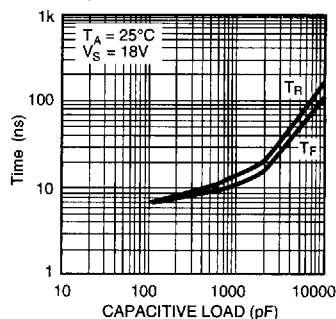
**Delay Time vs. Temperature**



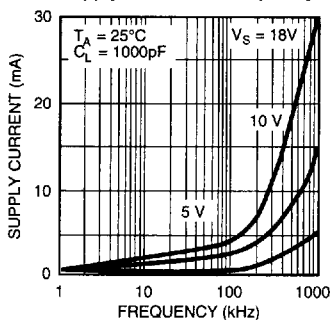
**Supply Current vs. Capacitive Load**



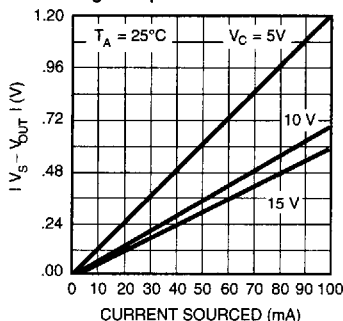
**Rise and Fall Time vs. Capacitive Load**



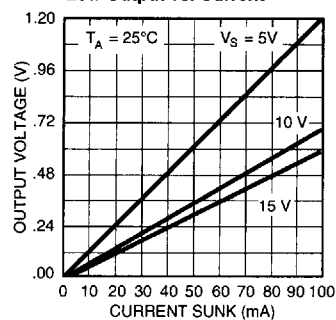
**Supply Current vs. Frequency**

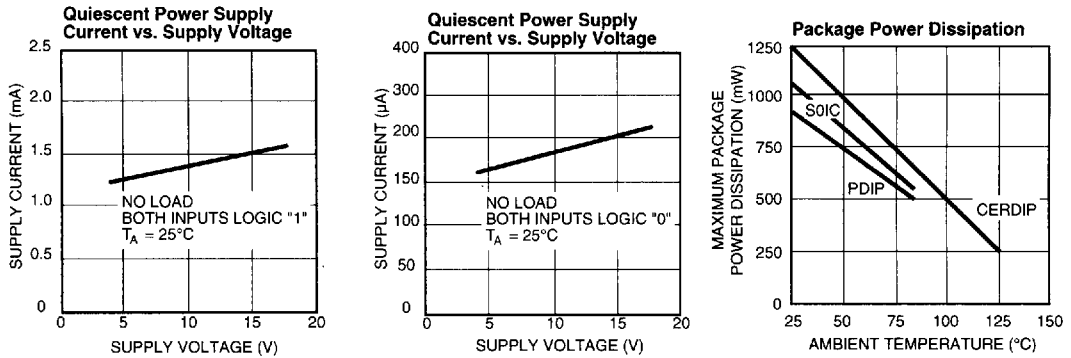


**High Output vs. Current**

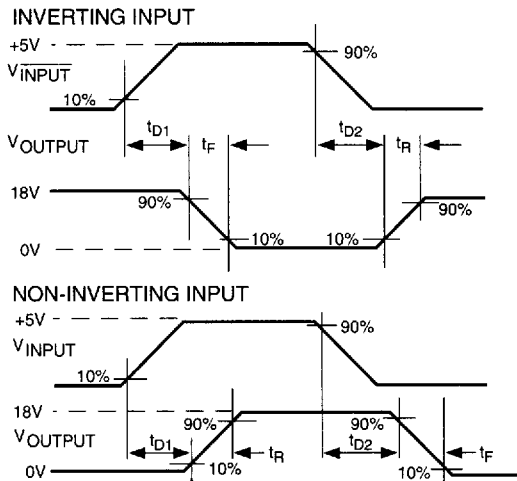
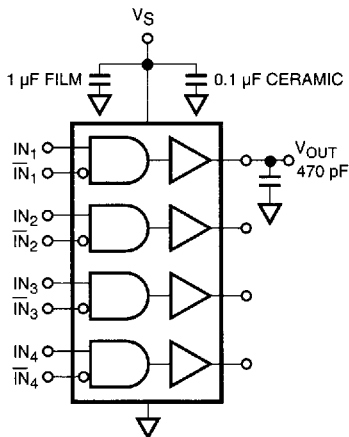


**Low Output vs. Current**



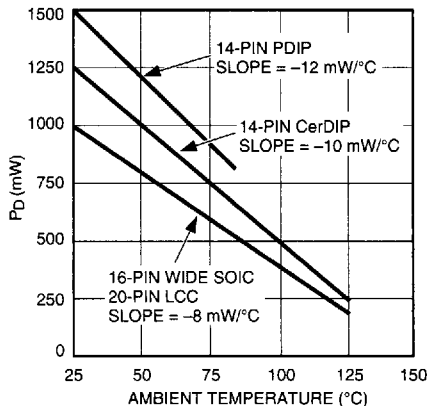


Test Figure 1



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## Package Power Dissipation



## Quad Driver Drives H Bridge to Control Motor Speed and Direction

