Preliminary Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU2X54FT
QUAD-FET (Fast Ethernet Transceiver) for 100Base-TX/FX Repeaters

Features

100 Mbits/s TX Transceiver

- Compatible with *IEEE** 802.3u MII (clause 22), PCS (clause 23), PMA (clause 24), and PMD (clauses 25 and 26) specifications
- Scrambler/descrambler bypass
- Encoder/decoder bypass
- 3-statable MII interface
- Selectable carrier sense signal generation (CRS) asserted during either transmission or reception in half duplex
- Selectable MII or 5-bit code group interface
- Half-duplex operation only
- Optional carrier integrity monitor (CIM)
- On-chip filtering and adaptive equalization that eliminates the need for external filter

100 Mbits/s FX Transceiver

- Compatible with *IEEE* 802.3U 100Base-FX standard
- Reuses existing twisted-pair I/O pins for compatible fiber-optic transceiver pseudo-ECL (PECL) data:
  - — No additional data pins required
  - — Reuses existing LU2X54FT pins for fiber-optic signal detect (FOSD) inputs
- Fiber mode automatically configures port:
  - — Enables 100Base-FX remote fault signaling
  - — Disables MLT-3 encoder/decoder
  - — Disables scrambler/descrambler
- FX mode enable is pin- or register-selectable on an individual per-port basis

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

General

- Independent MII mode: separate MII signals for each port, except MDIO and MDC which are common to all four channels
- Bused MII mode:
  - — Shared MII signals: TXD[3:0], RXD[3:0], TX_CLK25, RX_DV[3:0], RX_ER[3:0], RX_CLK25, MDIO, and MDC
  - — Separate TX_EN, RX_EN, CRS, and COL pins for each port
  - — Drivers on bused signal can drive up to eight LU2X54FTs (32 ports)
- Supports the station management protocol and frame format (clause 22):
  - — Basic and extended registers
  - — Supports next page function
  - — Operates up to 12.5 MHz
  - — Accepts preamble suppression
  - — Maskable status interrupts
- Supports the following management functions via pins if station management is unavailable:
  - — Carrier integrity enable
  - — Encoder/decoder bypass
  - — Scrambler/descrambler bypass
  - — Carrier sense select
  - — FX mode select
  - — No link pulse mode
- Single 25 MHz crystal input or 25 MHz clock input
- Provides four status signals: receive activity, transmit activity, collision, and link integrity
- Optional LED pulse stretching
- Per-channel powerdown mode
- Loopback mode
- Internal pull-up or pull-down resistors to set default powerup mode
- 0.35 µm, low-power CMOS technology
- 208-pin SQFP
- Single 5 V power supply

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Description

Configuration

The LU2X54FT is a four-channel, single-chip complete transceiver designed specifically for 100Base-TX/FX repeaters.

Each channel implements:

- Physical coding sublayer (PCS) of *IEEE* 802.3u.
- Physical medium attachment (PMA) of *IEEE* 802.3u.
- MII management of *IEEE* 802.3u.
- Physical medium dependent (PMD) of *IEEE* 802.3

The LU2X54FT supports operations over two pairs of category 5 cable (100Base-TX), or over fiber-optic cable (100 Base-FX).

Figure 1 gives a functional overview of the LU2X54FT while Figure 2 details its single-channel functions.

Figure 3 shows an application drawing of how the LU2X54FT single channel interfaces to the twisted pair (TP). A typical fiber-optic interface is shown in Figure 4.

Bused MII Mode

The LU2X54FT has been designed for operation in two basic system interface modes of operation:

- Separate MII ports. The separate mode provides four independent RJ-45 to MII ports and is similar to having four independent transceivers.
- Bused mode. This mode is designed specifically for repeater applications to save pins. In bused mode, data from all of the ports will be internally bused to a single MII interface port.

The bused mode is used when the LU2X54FT is communicating with a 100 Mbit/s repeater IC, and allows the use of the optional security feature. Figure 5 shows a block diagram of the bused mode of operation. In this mode, separate pins are used for RX_EN, TX_EN, CRS, and COL.

The individual MII signals are routed to the single MII port (TX_CLK25, TXD[3:0], TX_ER, RX_CLK25, RXD[3:0], RX_DV, and RX_ER).

The bused interface allows each of the four transceivers to be connected to a single system interface.

Clocking

The LU2X54FT requires an internal 25 MHz clock.

This clock can be supplied as:

- 25 MHz clock input
- The 25 MHz clock can also be internally generated by an on-chip oscillator if an external crystal is supplied.

The LU2X54FT will automatically detect if a 25 MHz clock is supplied, or if a crystal is being used to generate the 25 MHz clock.

The crystal specifications are listed in Table 1, and the crystal circuit is shown in Figure 3 and Figure 4.

Table 1. Crystal Specifications

Parameter	Requirement
Type	Quartz Fundamental Mode
Frequency	25 MHz
Stability	±25 ppm, 0 °C—70 °C
Shunt Capacitor	7 pF
Load Capacitor	20 pF
Series Resistance	<30 Ω

FX Mode

Each individual port of the LU2X54FT can be operated in 100Base-FX mode by selecting it through the pin program option (RXLED[D:A]/FX_MODE_EN[D:A]), or through the register bit (register 29, bit 0).

When operating in FX mode, the twisted-pair I/O pins are reused as the fiber-optic transceiver I/O data pins, and the fiber-optic signal detect (FOSD) inputs are enabled.

Figure 4 shows a typical FX port interface. Note that no additional external components, excluding those needed by the fiber transceiver, are required.

When a port is placed in FX mode, it will automatically configure the port for 100Base-FX operation (and the register bit control will be ignored) such that:

- The far-end fault signaling option will be enabled.
- The MLT-3 encoding/decoding will be disabled.
- Scrambler/descrambler will be disabled.
- The signal detect inputs will be activated.

Description (continued)

Functional Block Diagrams

Device Overview

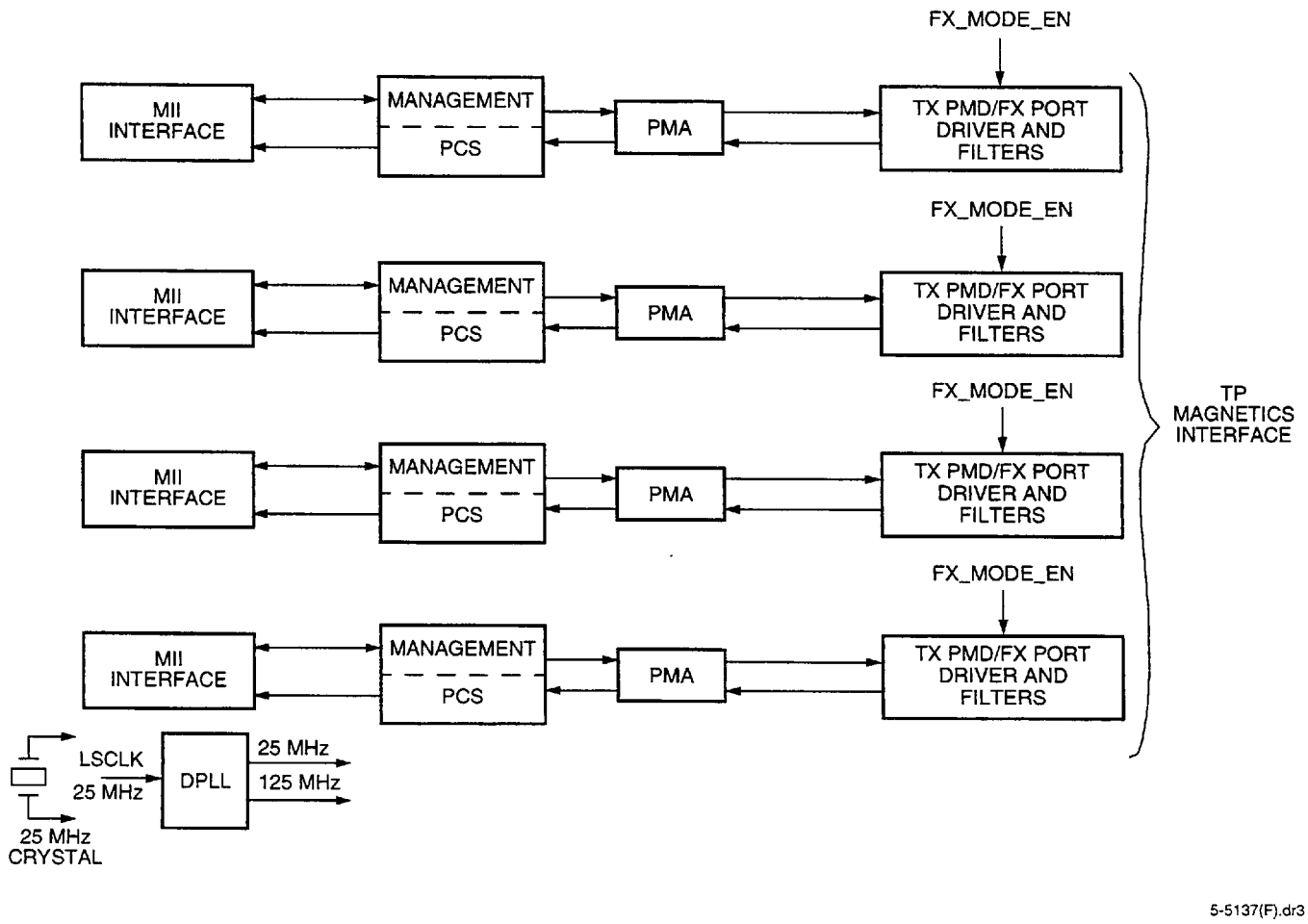

Figure 1. LU2X54FT Device Overview

Description (continued)

Functional Block Diagrams (continued)

Single-Channel Functions

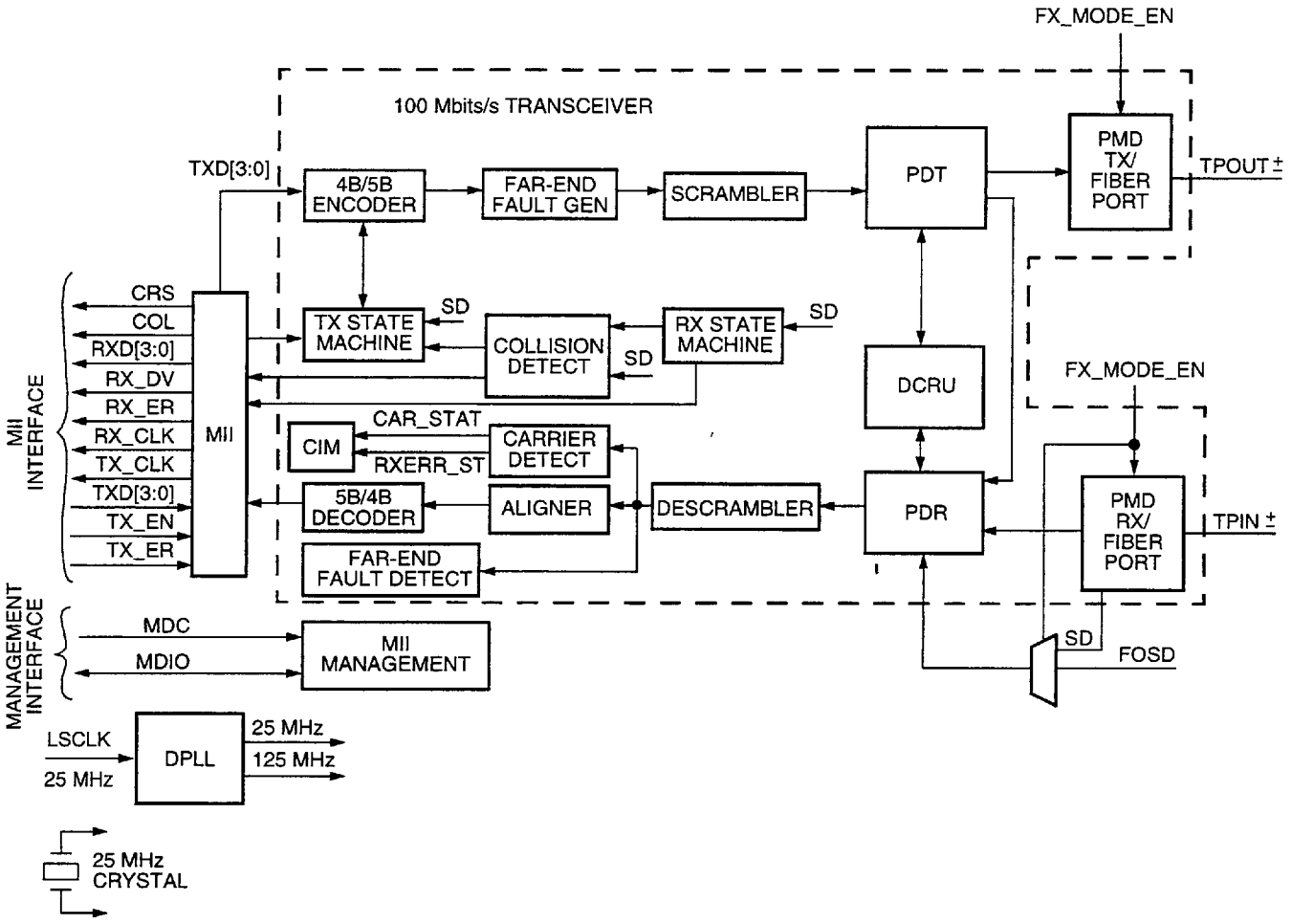

Figure 2. LU2X54FT Single-Channel Detail Block Diagram

Description (continued)

Application Diagrams

Twisted-Pair Interface

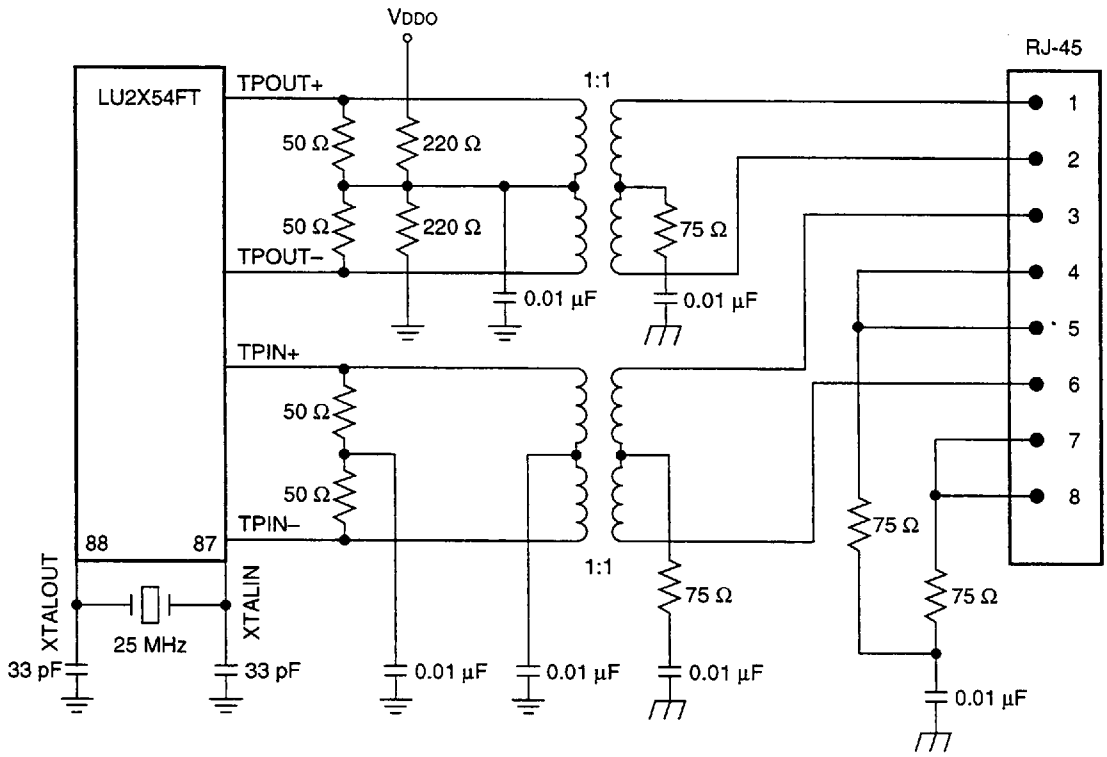

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Figure 3. Typical Single-Channel Twisted-Pair (TP) Interface

Description (continued)

Application Diagrams (continued)

Fiber-Optic Interface

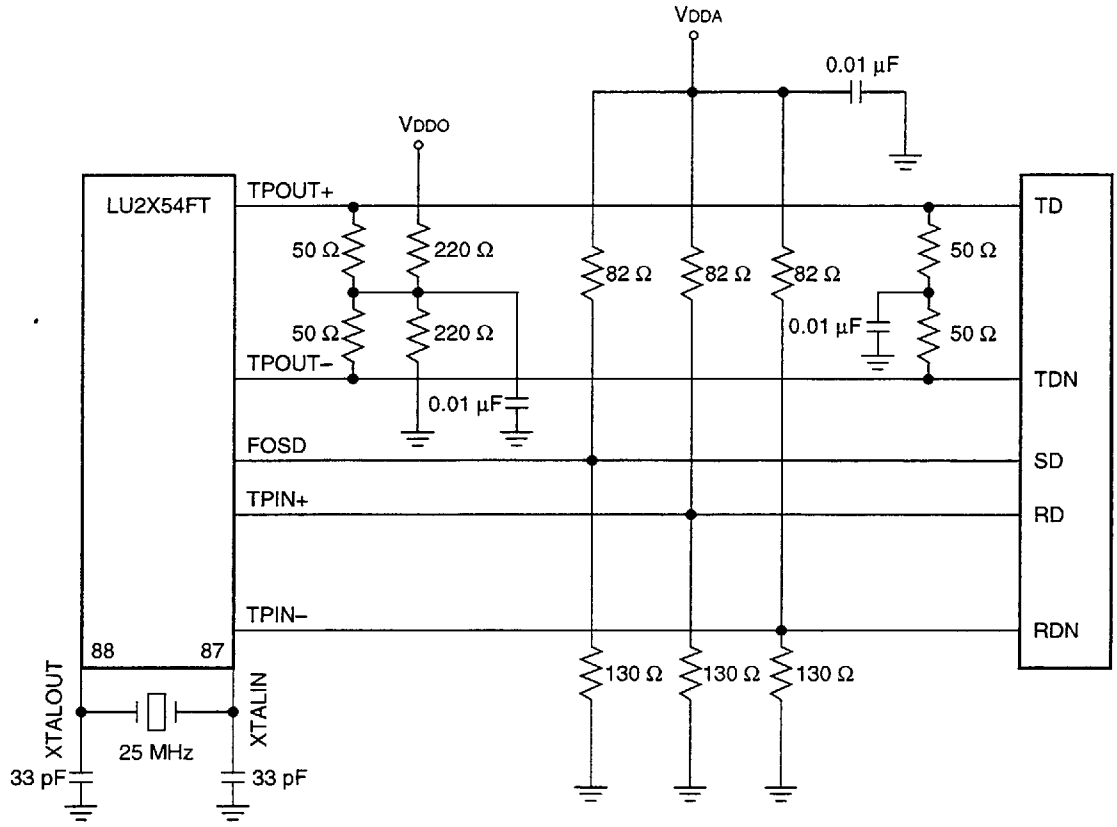


Figure 4. Typical Single-Channel Fiber-Optic Interface

Description (continued)

Bused Mode Block Diagram

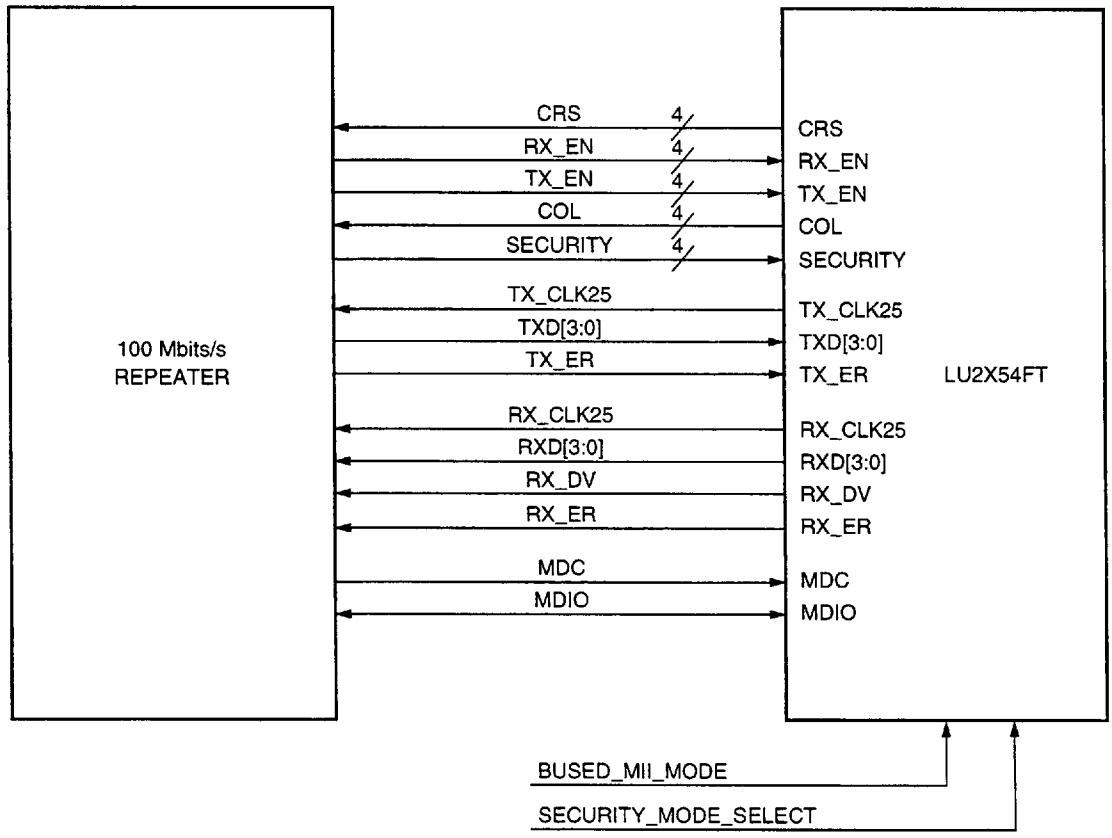


Figure 5. LU2X54FT in Bused MII Mode

Pin Information

Pin Diagram for Normal MII Mode

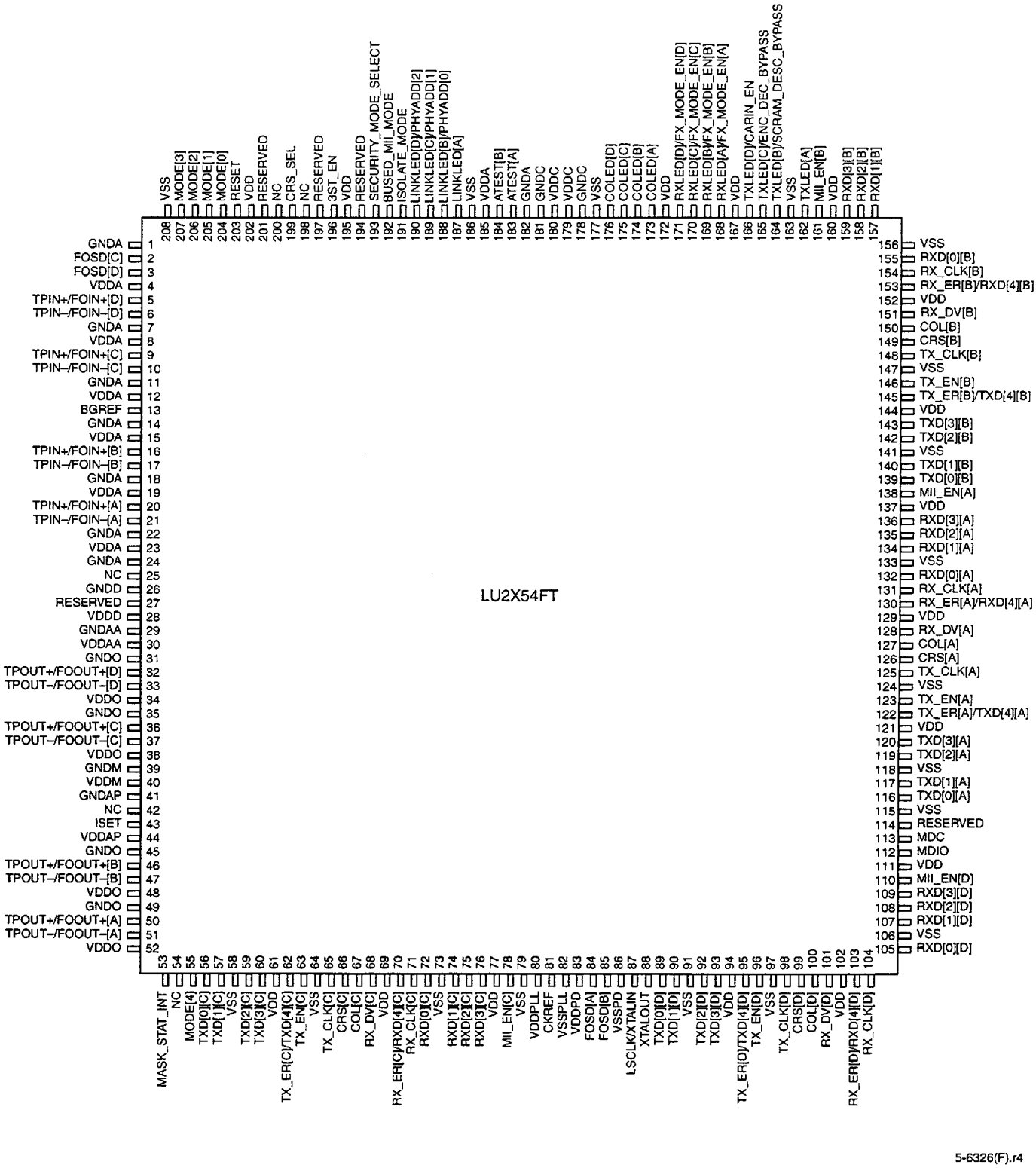


Figure 6. Preliminary Pinout for Normal MII Mode

Pin Information (continued)

Pin Diagram for Bused MII Mode

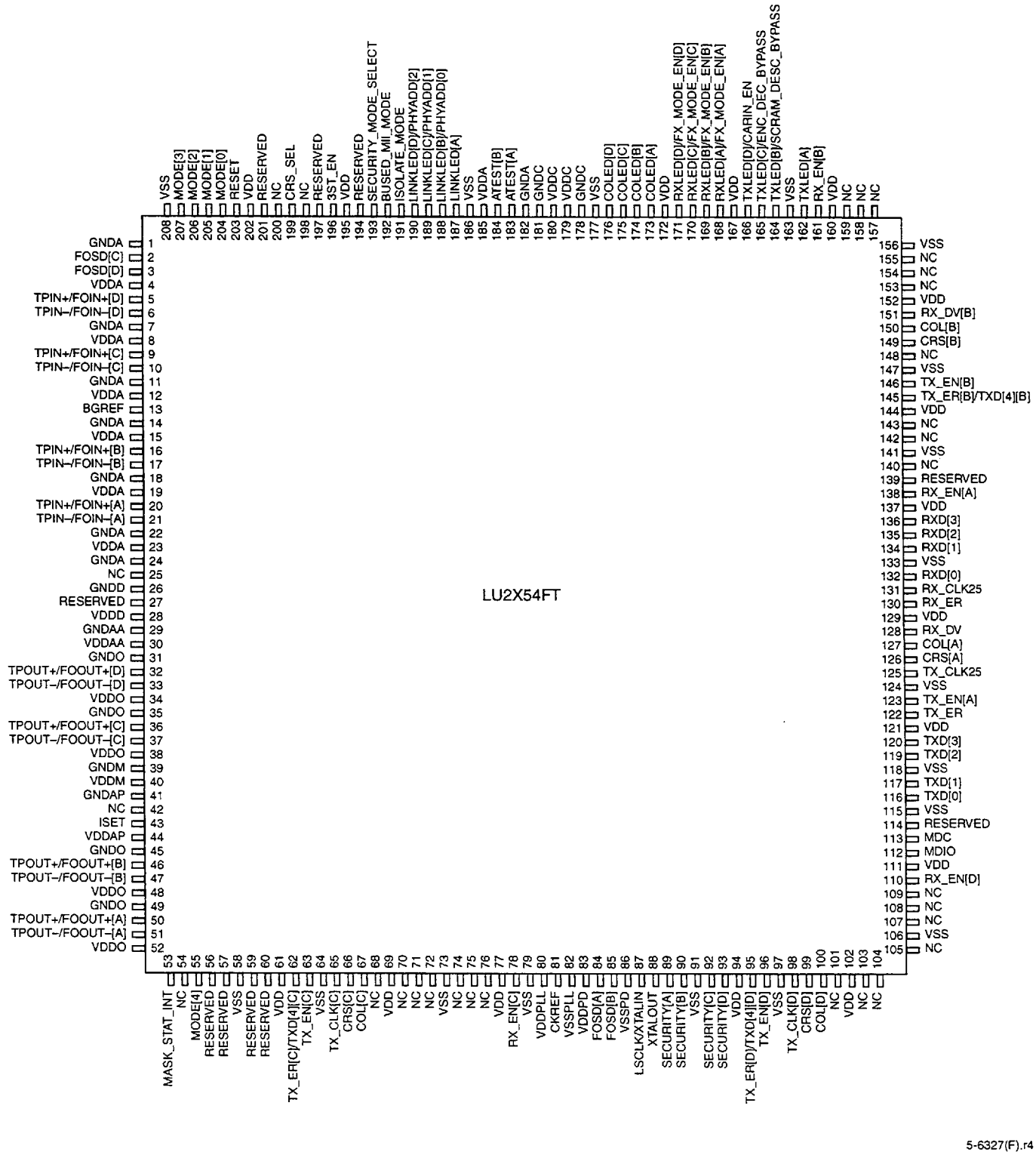


Figure 7. Preliminary Pinout for Bused MII Mode

Pin Information (continued)

Pin Maps

Table 2. LU2X54FT Pin Maps

Normal Mode Pins	Bused Mode Pin Functions
RXD[3:0][D]	Not used
CRS[D:A]	CRS[D:A]
TXD[3:0][C]	Not used
MII_EN[D:A]	RX_EN[D:A]
TXD[3:0][D]	SECURITY
TX_EN[D:A]	TX_EN[D:A]
RXD[3:0][C]	Not used
COL[D:A]	COL[D:A]
SECURITY_MODE_SELECT	SECURITY_MODE_SELECT
BUSED_MII_MODE	BUSED_MII_MODE
TX_CLK[A]	TX_CLK25
TX_CLK[B]	Not used
RX_CLK[B]	Not used
RX_CLK[A]	RX_CLK25
RXD[0][B]	Not used
RXD[3:0][A]	RXD[3:0]
RX_DV[A]	RX_DV
RX_ER[A]/RXD[4][A]	RX_ER
TXD[0][B]	Not used
TXD[3:0][A]	TXD[3:0]
TX_ER[A]/TXD[4][A]	TX_ER

Pin Information (continued)

Pin Descriptions

This section describes the LU2X54FT signal pins. Note that any register bit referenced includes the register number and bit position. For example, register bit [29.8] is register 29, bit 8.

Table 3. MII Interface Pins in Normal MII Mode (Four Separate MII Ports)

Pin	Signal	Type	Description
100 67 150 127	COL[D:A]	O	**Collision Detect.** This signal signifies that a collision has occurred on the network. COL is asserted high whenever there is transmit and receive activity on the UTP media. COL is the logical AND of TX_EN and receive activity, and is an asynchronous output.
99 66 149 126	CRS[D:A]	O	**Carrier Sense.** When CRS_SEL is low, this signal is asserted high when either the transmit or receive medium is nonidle. This signal remains asserted throughout a collision condition. When CRS_SEL is high, CRS is asserted on receive activity only. CRS_SEL is set via the MII management interface or the CRS_SEL pin.
104 71 154 131	RX_CLK[D:A]	O	**Receive Clock.** 25 MHz clock output. RX_CLK has a worst-case 45/55 duty cycle. RX_CLK provides the timing reference for the transfer of RX_DV, RXD, and RX_ER signals.
109 76 159 136 108 75 158 135 107 74 157 134 105 72 155 132	RXD[3:0][D:A]	O	**Receive Data.** 4-bit parallel data outputs that are synchronous to RX_CLK. When RX_ER[D:A] is asserted high, an error code will be presented on RXD[3:0][D:A] where appropriate. The codes are as follows: ■ Packet errors: ERROR_CODES = 2h. ■ Link errors: ERROR_CODES = 3h. (Packet and link error codes will only be repeated if registers [29.9] and [29.8] are enabled.) ■ Premature end errors: ERROR_CODES = 4h. ■ Code errors: ERROR_CODES = 5h.
101 68 151 128	RX_DV[D:A]	O	**Receive Data Valid.** When this pin is high, it indicates the LU2X54FT is recovering and decoding valid nibbles on RXD[3:0], and the data is synchronous with RX_CLK. RX_DV is synchronous with RX_CLK.
103 70 153 130	RX_ER[D:A]/ RXD[4][D:A]	O	**Receive Error.** When high, RX_ER indicates the LU2X54FT has detected a coding error in the frame presently being transferred. RX_ER is synchronous with RX_CLK.
			Receive Data[4]. When encoder/decoder bypass (ENC_DEC_BYPASS) is selected through the MII management interface, this output serves as the RXD[4] output.

Pin Information (continued)

Pin Descriptions (continued)

Table 3. MII Interface Pins in Normal MII Mode (Four Separate MII Ports) (continued)

Pin	Signal	Type	Description
98 65 148 125	TX_CLK[D:A]	O	**Transmit Clock.** 25 MHz clock output. TX_CLK provides timing reference for the transfer of the TX_EN, TXD, and TX_ER signals sampled on the rising edge of TX_CLK.
93, 60, 143, 120, 92, 59, 142, 119, 90, 57, 140, 117, 89, 56, 139, 116	TXD[3:0][D:A]	I	**Transmit Data.** 4-bit parallel input synchronous with TX_CLK.
96 63 146 123	TX_EN[D:A]	I	**Transmit Enable.** When driven high, this signal indicates there is valid data on TXD[3:0]. TX_EN is synchronous with TX_CLK.
95 62 145 122	TX_ER[D:A]/ TXD[4][D:A]	I	**Transmit Coding Error.** When driven high, this signal causes the encoder to intentionally corrupt the byte being transmitted across the MII (00100 will be transmitted). When the encoder/decoder bypass bit is set, this input serves as the TXD[4] input.
110 78 161 138	MII_EN[D:A]	I	**MII Enable.** For normal MII mode of operation (nonbused mode), MII_EN for each channel must be tied high to enable each individual port being used.

Pin Information (continued)

Pin Descriptions (continued)

Table 4. MII Interface Pins in Bused MII Mode

Pin	Signal	Type	Description
125	TX_CLK25	O	**Shared Transmit Clock.** 25 MHz clock output. TX_CLK25 provides timing reference for the transfer of the TX_EN, TXD, and TX_ER signals that are sampled on the rising edge of TX_CLK25.
99 66 149 126	CRS[D:A]	O	**Carrier Sense.** When CRS_SEL is low, this signal is asserted high when either the transmit or receive medium is nonidle. This signal remains asserted throughout a collision condition. When CRS_SEL is high, CRS is asserted on receive activity only. CRS_SEL is set via the MII management interface or the CRS_SEL pin.
131	RX_CLK25	O	**Shared Receive Clock.** 25 MHz clock output. RX_CLK25 has a worst-case 45/55 duty cycle. RX_CLK25 provides the timing reference for the transfer of RX_DV, RXD, and RX_ER signals. These signals are sampled on the rising edge of RX_CLK25.
136 135 134 132	RXD[3:0]	O	**Shared Receive Data.** Four-bit parallel data outputs that are synchronous to the falling edge of RX_CLK25. When RX_ER is asserted high, an error code will be presented on RXD[3:0] where appropriate. The codes are as follows: ■ Packet errors, ERROR_CODES = 2h. ■ Link errors, ERROR_CODES = 3h (packet and link error codes will only be repeated if registers [29.9] and [29.8] are enabled). ■ Premature end errors, ERROR_CODES = 4h. ■ Code errors, ERROR_CODES = 5h.
60 59 57 56	RESERVED	I	**Reserved.** Tie to ground.
110 78 161 138	RX_EN[D:A]	I	**Receive Enable.** When RX_EN is driven high, its channel's data, clock, and receive data valid signals (RXD, RX_ER, RX_DV, and RX_CLK25) are driven onto the shared bus. **Note:** Care should be taken that no more than one RX_EN is asserted at a time.
128	RX_DV	O	**Shared Receive Data Valid.** When this pin is driven high, it indicates that the LU2X54FT is recovering and decoding valid nibbles on RXD[3:0] and that the data is synchronous with RX_CLK25. RX_DV is synchronous with RX_CLK25.
130	RX_ER	O	**Shared Receive Error.** When asserted high, it indicates that the LU2X54FT has detected a coding error in the frame presently being transferred. RX_ER is synchronous with RX_CLK25.
139	RESERVED	I	**Reserved.** Tie to ground.
120 119 117 116	TXD[3:0]	I	**Shared Transmit Data.** Four-bit parallel input synchronous with TX_CLK25.

Pin Information (continued)

Pin Descriptions (continued)

Table 4. MII Interface Pins in Bused MII Mode (continued)

Pin	Signal	Type	Description
93 92 90 89	SECURITY[D:A]	I	**Security.** When security is activated, the LU2X54FT will ignore the transmit data, and a fixed pattern is transmitted (alternating 1, 0). Security should not be asserted until after the entire preamble has been transmitted. **Note:** SECURITY is only activated when SECURITY_MODE_SELECT is high.
96 63 146 123	TX_EN[D:A]	I	**Transmit Enable.** When TX_EN is driven high, it indicates that its channel's input data is valid.
122	TX_ER	I	**Shared Transmit Coding Error.** When asserted high, it causes the encoder to intentionally corrupt the byte being transmitted across the MII (00100 will be transmitted).
100 67 150 127	COL[D:A]	O	**Collision Detect.** This signal signifies that a collision has occurred on the network. COL is asserted high whenever there is transmit and receive activity on the UTP media. COL is the logical AND of TX_EN and receive activity, and it is an asynchronous output.
68, 70, 71, 72, 74, 75, 76, 101, 103, 104, 105, 107, 108, 109, 153, 154, 155, 157, 158, 159	NC	O	**No Connect.** Do not connect these pins.

Pin Information (continued)

Pin Descriptions (continued)

Table 5. MII Management Pins

Pin	Signal	Type	Description
113	MDC	I	**Management Data Clock.** This is the timing reference for the transfer of data on the MDIO signal. This signal may be asynchronous to RX_CLK and TX_CLK. The maximum clock rate is 12.5 MHz. When running MDC above 6.25 MHz, MDC must be synchronous with LSCLK and have a setup time of 15 ns and a hold time of 5 ns with respect to LSCLK. When using an external crystal instead of an LSCLK input, the maximum MDC rate is 6.25 MHz.
112	MDIO	I/O	**Management Data Input/Output.** This I/O is used to transfer control and status information between the LU2X54FT and the station management. Control information is driven by the station management synchronous with MDC. Status information is driven by the LU2X54FT synchronous with MDC. This pin requires a 1.5 kΩ pull-up resistor.
53	MASK_STAT_INT	O	**Maskable Status Interrupt.** This pin will go high whenever there is a change in status as defined in Table 16.

Table 6. Twisted-Pair (TP) Interface Pins

Pin	Signal	Type	Description
5 9 16 20	TPIN+/FOIN+[D:A]	I	**Received Data.** Positive differential received 125 Mbaud MLT3 from magnetics, or 125 Mbaud pseudo-ECL from fiber transmitter.
6 10 17 21	TPIN–/FOIN–[D:A]	I	**Received Data.** Negative differential received 125 Mbaud MLT3 from magnetics, or 125 Mbaud pseudo-ECL from fiber transmitter.
32 36 46 50	TPOUT+/FOOUT+[D:A]	O	**Transmit Data.** Positive differential transmit 125 Mbaud MLT3 from magnetics, or 125 Mbaud pseudo-ECL to fiber transmitter.
33 37 47 51	TPOUT–/FOOUT–[D:A]	O	**Transmit Data.** Negative differential transmit 125 Mbaud MLT3 to magnetics, or 125 Mbaud pseudo-ECL to fiber transmitter.
3 2 85 84	FOSD[D:A]	I	**Fiber-Optic Signal Detect.** Pseudo-ECL input signal which indicates whether or not the fiber-optic receive pairs (FOIN±) are receiving valid signal levels.

Pin Information (continued)

Pin Descriptions (continued)

Table 7. Miscellaneous Pins

Pin	Signal	Type	Description
81	CKREF	I	**Clock Reference.** Connect this pin to a 1 nF ± 10% capacitor to ground.
184 183	ATEST[B:A]	O	**Reserved.** For normal operation, leave these pins unconnected.
197	RESERVED	I	**Reserved.** Tie to ground.
1, 7, 11, 14, 18, 22, 24, 26, 29, 31, 35, 39, 41, 45, 49, 58, 64, 73, 79, 82, 86, 91, 97, 106, 115, 118, 124, 133, 141, 147, 156, 163, 177, 178, 181, 182, 186, 208	GND/Vss	PWR	**Ground.** (38 pins.)
4, 8, 12, 15, 19, 23, 28, 30, 34, 38, 40, 44, 48, 52, 61, 69, 77, 80, 83, 94, 102, 111, 121, 129, 137, 144, 152, 160, 167, 172, 179, 180, 185, 195, 202	VDD	PWR	**VDD.** Single 5.0 V ± 5% power supply. (35 pins.)
196	3ST_EN	I	**3-State Enable.** When this pin is high, all digital outputs will be 3-stated. For normal operating conditions, pull this pin low.
13	BGREF	I	**Band-Gap Reference.** Connect this pin to a 24.9 kΩ ± 1% resistor to ground. The parasitic load capacitance should be less than 15 pF.
43	ISET	I	**Current.** An external resistor (nominally 24.9 kΩ) is placed from this pin to ground to set the TP driver transmit output level.
114 27	RESERVED	I	**Reserved.** Tie to ground.
166	TXLED[D]/ CARIN_EN	I/O	**Transmit LED[D].** This pin indicates transmit activity on port D. External buffers are necessary to drive the LEDs.
			Carrier Integrity Enable. At powerup or reset, if this pin is pulled high through a 4.7 kΩ resistor, it will enable the carrier integrity function of register 29, bit 3, if station management is unavailable. This pin has an internal 50 kΩ pull-down resistor for normal operation (CARIN_EN is disabled). This input and register bits [29:3] are ORed together.

Pin Information (continued)

Pin Descriptions (continued)

Table 7. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
165	TXLED[C]/ ENC_DEC_BYPASS	I/O	**Transmit LED[C].** This pin indicates transmit activity on port C. External buffers are necessary to drive the LEDs.
			Encoder/Decoder Bypass. At powerup or reset, if this pin is pulled high through a 4.7 kΩ resistor, it will enable the ENC_DEC_BYPASS function of register 29, bit 6, if station management is unavailable. This pin has an internal 50 kΩ pull-down resistor for normal operation (encoder/decoder ON). This input and the register bit [29.6] are ORed together enabling the encoder/decoder bypass function for all four channels.
164	TXLED[B]/ SCRAM_DESC_BYPASS	I/O	**Transmit LED[B].** This pin indicates transmit activity on port B. External buffers are necessary to drive the LEDs.
			Scrambler/Descrambler Bypass. At powerup or reset, this pin may be used to enable the SCRAM_DESC_BYPASS function by pulling this pin high through a 4.7 kΩ resistor, if station management is unavailable. This is the same function as register 29, bit 4. This pin has an internal 50 kΩ pull-down resistor for normal operation (scrambler/descrambler ON). This input and the register bit (29.4) are ORed together during powerup and reset.
162	TXLED[A]	O	**Transmit LED[A].** This pin indicates transmit activity on port A. External buffers are necessary to drive the LEDs.
171 170 169 168	RXLED[D:A]/ FX_MODE_EN[D:A]	O/I	**Receive LED[D:A].** This pin indicates receive activity. External buffers are necessary to drive the LEDs. These pins have internal 50 kΩ pull-down resistors.
			FX Mode Enable. At powerup or reset, when driven high through a 4.7 kΩ resistor, this pin will enable the FX mode (100Base-TX disabled), and when driven low, it will enable 100Base-TX mode (100Base-FX mode disabled).
176 175 174 173	COLED[D:A]	O	**Collision LED.** This pin indicates collision occurrence. External buffers are necessary to drive the LEDs. Channels A and B have internal 50 kΩ pull-down resistors but not channels C and D.
190	LINKLED[D]/ PHYADD[2]	O/I	**Link LED[D].** This pin indicates good link status on port D. External buffers are necessary to drive the LEDs.
			PHY Address 2. At powerup or reset, this pin is used to set the PHY address bit 2. If this pin is pulled high through a 50 kΩ resistor, it will set PHYADD[2] to a 1. If this pin is pulled low through a 50 kΩ resistor, it will set PHYADD[2] to a 0.
189	LINKLED[C]/ PHYADD[1]	I/O	**Link LED[C].** This pin indicates good link status on port C. External buffers are necessary to drive the LEDs.
			PHY Address 1. At powerup or reset, this pin is used to set the PHY address bit 1. If this pin is pulled high through a 50 kΩ resistor, it will set PHYADD[1] to a 1. If this pin is pulled low through a 50 kΩ resistor, it will set PHYADD[1] to a 0.

Pin Information (continued)

Pin Descriptions (continued)

Table 7. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
188	LINKLED[B]/ PHYADD[0]	I/O	**Link LED[B].** This pin indicates good link status on port B. External buffers are necessary to drive the LEDs.
			PHY Address 0. At powerup or reset, this pin may be used to set the PHY address bit 0. If this pin is pulled high through a 50 kΩ resistor, it will set PHYADD[0] to a 1. If this pin is pulled low through a 50 kΩ resistor, it will set PHYADD[0] to a 0.
187	LINKLED[A]	O	**Link LED[A].** This pin indicates good link status on port A. External buffers are necessary to drive the LEDs.
194	RESERVED		**Reserved.** Do not connect this pin. **Note:** This pin is an unused LED output driven high except during powerup and reset.
193	SECURITY_MODE_SELECT	I	**Security Mode Select.** At powerup or reset, if this pin is pulled high through a 4.7 kΩ resistor, this mode enables the use of the security feature. When security is activated high, the LU2X54FT will transmit a jam signal instead of data.This pin has an internal 50 kΩ pull-down resistor to set the default to the separate MII mode of operation when bused mode has been selected. If bused mode is not being used, pull this pin low or leave floating. **Note:** This pin is an unused LED output driven high except during powerup and reset.
192	BUSED_MII_MODE	I	**Bused MII Mode Select.** At powerup or reset, if this pin is pulled high through a 4.7 kΩ resistor, data streams from each port will appear on the single port A. In addition, control signals TX_EN, RX_EN, and CRS become active. This pin has an internal 50 kΩ pull-down resistor to set the default to the normal MII mode of operation. **Note:** This pin is an unused LED output driven high except during powerup and reset.
191	ISOLATE_MODE	I	**Isolate Mode.** As an input, this pin can be used at powerup or reset to select the isolate operation mode. If this pin is pulled high through a 4.7 kΩ resistor, the LU2X54FT will powerup or reset to the isolate mode. (MII outputs to high-impedance state.) This pin is internally pulled low through a 50 kΩ resistor. The default state is for the LU2X54FT to powerup or reset in a nonisolate mode. This pin and register bit [10.0] are ORed together during powerup and reset. **Note:** This pin is an unused LED output driven high except during powerup and reset.
201	RESERVED	I	**Reserved.** Tie low through a 4.7 kΩ resistor. **Note:** This pin is an unused LED output driven high except during powerup and reset.
87	LSCLK/XTALIN	I	**CMOS Local Symbol Clock.** A 25 MHz clock, ±100 ppm, 40%—60% duty cycle.
			Crystal Oscillator Input. A 25 MHz crystal ±25 ppm can be connected across XTALIN and XTALOUT.

Pin Information (continued)

Pin Descriptions (continued)

Table 7. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
88	XTALOUT	I	**Crystal Oscillator Output.** A 25 MHz crystal ±25 ppm can be connected across XTALIN and XTALOUT. If a single-ended external clock (LSCLK) is connected to XTALIN, the crystal output pin should be left floating.
55 207 206 205 204	MODE[4:0]	I	**Test Mode Select.** Reserved for manufacturing testing. These pins should be tied low for normal operation.
203	RESET	I	**Full Chip Reset.** Reset must be asserted high for at least five LSCLK cycles. The LU2X54FT will come out of reset after 400 µs. LSCLK must remain running during reset. **Note:** This pin is an unused LED output driven high except during powerup and reset.
199	CRS_SEL	I	**Carrier Sense Select.** At powerup, this pin may be used to select the mode of CRS operation. When this pin is pulled high through a 4.7 kΩ resistor, CRS will be asserted on receive activity only. This is the same function as register 29, bit 10. This pin has an internal 50 kΩ pull-down resistor for normal mode operation (default: CRS asserted on transmit or receive activity). This input and the register bit [29.10] are ORed together during powerup and reset. **Note:** This pin is an unused LED output driven high except during powerup and reset.
25 42 54	NC	—	**No Connect.** Do not connect these pins.
198 200	NC	—	**No Connect.** Do not connect these pins. **Note:** This pin is an unused LED output driven high except during powerup and reset.

MII Station Management

Basic Operations

The primary function of station management is to transfer control and status information about the LU2X54FT to a management entity. This function is accomplished by the MDC clock input, which has a maximum frequency of 12.5 MHz, along with the MDIO pin. The MDIO pin (112) requires an external 1.5 kΩ pull-up resistor.

The management interface (MII) uses MDC and MDIO to physically transport information between the PHY and the station management entity.

A specific set of registers and their contents (described in Table 8) defines the nature of the information transferred across this interface. Frames transmitted on the MII management interface will have the frame structure shown in Table 8. The order of bit transmission is from left to right. Note that reading and writing of the management register must be completed without interruption.

Since the LU2X54FT is a four-channel device, each of the management registers is duplicated four times as depicted in the functional block diagram shown in Figure 1. To select a particular channel [D:A], write to that channel's unique PHY address as described in Table 9.

MII Management Frames

The fields and format for management frames are described in the following tables.

Table 8. MII Management Frame Format

Read/Write (R/W)	Pre	ST	OP	PHYADD	REGAD	TA	DATA	Idle
R	1 . . . 1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
W	1 . . . 1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 9. MII Management Frames—Field Descriptions

Field	Description
Pre	**Preamble.** The preamble is a series of 32 ones. The LU2X54FT will accept frames with no preamble. This is indicated by a 1 in register 1, bit 6.
ST	**Start of Frame.** The start of frame is indicated by a 01 pattern.
OP	**Operation Code.** The operation code for a read transaction is 10. The operation code for a write transaction is 01.
PHYADD	**PHY Address.** The PHY address is 5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB of the address. A station management entity, which is attached to multiple PHY entities, must have prior knowledge of the appropriate PHY address for each entity. The address 00000 is the broadcast address. This address will produce a match regardless of the local address. The LU2X54FT maps the PHYADD[2:0] to the most significant 3 bits, while the least significant 2 bits address the channel within the LU2X54FT as follows: 00: Channel A. 01: Channel B. 10: Channel C. 11: Channel D.
REGAD	**Register Address.** The register address is 5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	**Turnaround.** The turnaround time is a 2-bit time spacing between the register address field and the data field of a frame to avoid drive contention on MDIO during a read transaction. During a write to the LU2X54FT, these bits are driven to a 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the LU2X54FT during the second bit time.
DATA	**Data.** The data field is 16 bits. The first bit transmitted and received is bit 15 of the register being addressed.

MII Station Management (continued)

Management Registers (MR)

Register Overview

The MII management 16-bit register (MR) set is implemented as described in the table below.

CAUTION: Reserved registers may be used for manufacturing testing. Do not write to any reserved registers.

Table 10. MII Management Registers (MR)

Register Address	Symbol	Name	Default (Hex Code)
0	MR0	Control Register	3000
1	MR1	Status Register	7849
2	MR 2	PHY Identifier Register 1	0180
3	MR 3	PHY Identifier Register 2	7641
4—27, 30	MR8—MR27	Reserved	0000
28	MR28	Device-specific Register 1	—
29	MR29	Device-specific Register 2	2080
31	MR31	Device-specific Register 3 (quick status)	—

MII Station Management (continued)

Management Registers (MR) (continued)

This section discusses each management register and its bit definitions.

Table 11. MR0—Control Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
0.15 (SW_RESET)	R/W	**Reset.** Setting this bit to a 1 will reset the LU2X54FT. All registers will be set to their default state. This bit is self-clearing. The default is 0.
0.14 (LOOPBACK)	R/W	**Loopback.** When this bit is set to 1, no data transmission will take place on the media. Any receive data will be ignored. The loopback signal path will contain all circuitry up to, but not including, the PMD. The default value is a 0.
0.13 (RESERVED)	NA	**Reserved.** This bit should always be set to a 1.
0.12 (RESERVED)	NA	**Reserved.** This bit should always be set to a 0.
0.11 (PWRDN)	R/W	**Powerdown.** The LU2X54FT may be placed in a low-power state by setting this bit to a 1, the 100 Mbits/s transceiver will be powered down. While in the powerdown state, the LU2X54FT will respond to management transactions. The default state is a 0.
0.10(ISOLATE)	R/W	**Isolate Mode.** When this bit is set to a 1, the MII outputs will be brought to the high-impedance state. The default state is a 0. This bit is ORed with the ISOLATE_MODE pin during powerup and reset.
0.9:8 (RESERVED)	NA	**Reserved.** These bits should always be set to a 0.
0.7 (COLTST)	R/W	**Collision Test.** When this bit is set to a 1, the LU2X54FT will assert the COL signal in response to TX_EN. This bit should only be set when in loopback mode.
0.6:0 (RESERVED)	NA	**Reserved.** All bits will read 0.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write, NA = not applicable.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 12. MR1—Status Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
1.15 (RESERVED)	R	**Reserved.** This bit will always read as 0.
1.14:11 (RESERVED)	R	**Reserved.** These bits will always read as 1.
1.10:7 (RESERVED)	R	**Reserved.** These bits will read as a 0.
1.6 (NO_PA_OK)	R	**Suppress Preamble.** This bit is set to a 1 indicating that the LU2X54FT accepts management frames with the preamble suppressed.
1.5 (RESERVED)	R	**Reserved.** These bits should always read as 0.
1.4 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. The default is a 0.
1.3 (RESERVED)	R	**Reserved.** These bits should always read as 1.
1.2 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
1.1 (RESERVED)	R	**Reserved.** This bit will always read as 1.
1.0 (EXT_ABLE)	R	**Extended Capability.** This bit indicates that the LU2X54FT supports the extended register set (MR2 and beyond). It will always read a 1.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 13. MR2, 3—PHY Identifier Registers (1 and 2) Bit Descriptions

Register/Bit[1]	Type[2]	Description
2.15:0 (OUI[3:18])	R	**Organizationally Unique Identifier.** The third through the twenty-fourth bit of the OUI assigned to the PHY manufacturer by the *IEEE* are to be placed in register bits [2.15:0] and [3.15:10]. The value for bits [15:0] is 0180h.
3.15:10 (OUI[19:24])	R	**Organizationally Unique Identifier.** The remaining 6 bits of the OUI. The value for bits [15:10] is 1Dh.
3.9:4 (MODEL(5:0)]	R	**Model Number.** 6-bit model number of the device. The model number is 54 dec.
3.3:0 (VERSION[3:0])	R	**Revision Number.** The value of the present revision number. The value is 01h for the first version.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

Table 14. MR28—Device-Specific Register 1 (Status Register) Bit Descriptions

Register/Bit[1]	Type[2]	Description
28.15:6 (R28[15:6])	R	**Unused.** Read as 0.
28.5 (DISCON)	R/LH	**Disconnect.** If this bit is a 1, it indicates a disconnect. This bit will latch high until read. This bit defaults to 0.
28.4 (UNLOCKED)	R/LH	**Unlocked.** Indicates that the TX scrambler lost lock. This bit will latch high until read. This bit defaults to 0.
28.3 (RXERR_ST)	R/LH	**RX Error Status.** Indicates a false carrier. This bit will latch high until read. This bit defaults to 0.
28.2 (FRC_JAM)	R/LH	**Force Jam.** This bit will latch high until read. This bit defaults to 0.
28.1 (LNKUP)	R	**Link Up.** This bit, when set to a 1, indicates a transceiver is up and operational. This bit defaults to 0.
28.0 (RESERVED)	R	**Reserved.** These bits should always read as 0.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, LH = latched high.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 15. MR29—Device-Specific Register 2 Bit Descriptions

Register/Bit[1]	Type[2]	Description
29.15 (LOCALRST)	R/W	**Local Management Reset.** This is the local management reset bit. Writing a logic 1 to this bit will cause the lower 16 registers and registers 28 and 29 to be reset to their default values. This bit is self-clearing. Default state is 0.
29.14 (RST1)	R/W	**Generic Reset 1.** This register is used for manufacture test only. Default state is 0.
29.13 (RST2)	R/W	**Generic Reset 2.** This register is used for manufacture test only. Default state is 0.
29.12 (TMTROFF)	R/W	**Transmitter Off.** When this bit is set to 0, it forces TPIN+[D:A] low and TPIN–[D:A] high. This bit defaults to 1.
29.11 (RESERVED)	R/W	**Reserved.** Program to zero.
29.10 (CRS_SEL)	R/W	**Carrier Sense Select.** CRS will be asserted on receive only when this bit is set to a 1. If this bit is set to logic 0, CRS will by asserted on receive or transmit. This bit is ORed with the CRS_SEL pin during powerup and reset. Default state is 0.
29.9 (LINK_ERR)	R/W	**Link Error Indication.** When this bit is a 1, a link error code will be reported on RXD[3:0] of the LU2X54FT when RX_ER is asserted on the MII. The specific error codes are listed in the RXD pin description. If it is 0, it will disable this function. Default state is 0.
29.8 (PKT_ERR)	R/W	**Packet Error Indication Enable.** When this bit is a 1, a packet error code, which indicates that the scrambler is not locked, will be reported on RXD[3:0] of the LU2X54FT when RX_ER is asserted on the MII. When this bit is 0, it will disable this function. Default state is 0.
29.7 (PULSE_STR)	R/W	**Pulse Stretching.** When this bit is set to 1, the COLED[D:A], TXLED[D:A], and RXLED[D:A] output signal will be stretched between approximately 42 ms—84 ms. If this bit is set to 0, it will disable this feature. Default state is 1.
29.6 (ENC_DEC_BYPASS)	R/W	**Encoder/Decoder Bypass.** When this bit is set to 1, the 4B/5B encoder and 5B/4B decoder function will be disabled. This bit is ORed with the TXLED[C] pin during powerup and reset. Default state is 0.
29.5 (SAB)	R/W	**Symbol Aligner Bypass.** When this bit is set to 1, the aligner function will be disabled. Default state is 0.
29.4 (SCRAM_DESC_BYPASS)	R/W	**Scrambler/Descrambler Bypass.** When this bit is set to 1, the scrambling/descrambling functions will be disabled. This bit is ORed with the TXLED[B] pin during powerup and reset. Default state is 0.
29.3 (CARIN_EN)	R/W	**Carrier Integrity Enable.** When this bit is set to a 1, carrier integrity is enabled. This bit is ORed with the TXLED[D] pin during powerup and reset. Default state is 0.
29.2 (JAM_COL)	R/W	**Jam Enable.** When this bit is a 1, it enables JAM associated with carrier integrity to be ORed with COL. Default state is 0.
29.1 (FEF_EN)	R/W	**Far-End Fault Enable.** This bit is used to enable the far-end fault detection and transmission capability. This capability may only be used if autonegotiation is disabled. This capability is to be used only with media that does not support autonegotiation. Setting this bit to 1 enables far-end fault detection and generation. Logic 0 will disable the function. Default state is 0.
29.0 (FX_MODE_EN)	R/W	**FX Mode Enable.** When set high, this bit will enable the FX mode (100Base-TX disabled). When low, it will enable 100Base-TX mode (100Base-FX mode disabled). This bit defaults to zero. It is ORed with the FX mode enable pin.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 16. MR31—Device-Specific Register 4 (Quick Status) Bit Descriptions

Register/Bit[1]	Type[2]	Description
31.15 (ERROR)	R	**Receiver Error.** When this bit is a 1, it indicates that a receive error has been detected. This bit will remain set until cleared by reading the register. Default is a 0.
31.14 (RXERR_ST)/ (LINK_STAT_CHANGE)	R	**False Carrier.** When bit [31.7] is set to 0 and this bit is a 1, it indicates that the carrier detect state machine has found a false carrier. This bit will remain set until cleared by reading the register. Default is 0.
		Link Status Change. When bit [31.7] is set to a 1, this bit is redefined to become the LINK_STAT_CHANGE bit and goes high whenever there is a change in link status (bit [31.11] changes state).
31.13 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. Default is a 0.
31.12 (UNLOCKED)	R	**Unlocked.** If this bit is set, it indicates that the TX descrambler has lost lock. This bit will remain set until cleared by reading the register.
31.11 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching low function: a link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
31.10 (RESERVED)	R	**Reserved.** This bit will read as 0.
31.9 (RESERVED)	R	**Reserved.** These bits should always read as 1.
31.8 (RESERVED)	R	**Reserved.** These bits should always read as 0.
31.7 (INT_CONF)	R/W	**Interrupt Configuration.** When this bit is set to a 0, it defines bit [31.14] to be the RXERR_ST bit and the interrupt pin (MASK_STAT_INT) goes high whenever any of bits [31.15:12] go high or bit [31.11] goes low. When this bit is set high, it redefines bit [31.14] to become the LINK_STAT_CHANGE bit, and the interrupt pin (MASK_STAT_INT) goes high only when the link status changes (bit [31.14] goes high). This bit defaults to 0.
31.6 (MASK_STAT_INT)	R/W	**Interrupt Mask.** When set high, no interrupt is generated by this channel under any condition. When set low, interrupts are generated according to bit [31.7].
31.5:0 (RESERVED)	R	**Reserved.** Ignore these bits.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2 R = read; W = write.

MII Station Management (continued)

Unmanaged Operations

The LU2X54FT allows the user to set some of the station management functions during powerup or reset by strapping outputs high or low through weak resistors (50 kΩ). Table 17 shows the functions and their associated output pin. For detailed information on the function of these output pins, refer to the section on management registers described earlier in this data sheet. Also, information on how these output pins should be strapped is discussed in the Pin Descriptions section (Table 3 through Table 7).

Table 17. Output Pins for Normal MII Mode

Function (Register/Bit)	Pin	Internal Pull-Up/Pull-Down
PHYADD[2:0]	LINKLED[D:B]	None
RESERVED	LINKLED[A]	50 kΩ down
CARIN_EN	TXLED[D]	50 kΩ down
ENC_DEC_BYPASS	TXLED[C]	50 kΩ down
SCRAM_DESC_BYPASS	TXLED[B]	50 kΩ down
RESERVED	TXLED[A]	50 kΩ down
CRS_SEL	CRS_SEL	50 kΩ down
BUSED_MII_MODE	BUSED_MII_MODE	50 kΩ down
SECURITY_MODE_SELECT	SECURITY_MODE_SELECT	50 kΩ down
ISOLATE_MODE	ISOLATE_MODE	50 kΩ down
FX_MODE_ENABLE	RXLED[D:A]	50 kΩ down
RESERVED	COLED[B:A]	50 kΩ down
RESERVED	Not Used (198)	50 kΩ down
RESERVED	Not Used (200)	50 kΩ down
RESERVED	RESERVED (201)	50 kΩ down

Mode Select

Table 18. LU2X54FT Modes

MODE[4:0]	Description
00000	Normal operation
00001—11111	Reserved

Absolute Maximum Ratings (T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 19. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	125	°C
Voltage on Any Pin with Respect to Ground	—	–0.5	V_{DD} + 0.5	V
Maximum Supply Voltage	—	—	5.5	V

Table 20. Operating Conditions

Parameter	Symbol	Min	Type*	Max	Unit
Operating Supply Voltage	—	4.75	5.0	5.25	V
Power Dissipation:					
All Ports 100 Mbits/s	P_D	—	3.0	—	W
All Ports 100 Mbits/s FX	P_D	—	2.2	—	W
All Ports Autonegotiating	P_D	—	1.5	—	W

* Typical power dissipations are specified at 5.0 V and 25 °C. This is the power dissipated by the LU2X54FT. An additional 0.2 W of power is required for the external twisted-pair driver termination resistors.

Electrical Characteristics

The following specifications apply for V_{DD} = 5 V ± 5%.

Table 21. dc Characteristics

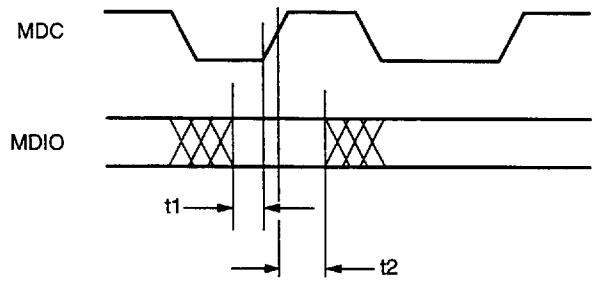
Parameter	Symbol	Min	Typ	Max	Unit
TTL Inputs:					
Input High Voltage	V_{IH}	2.0	—	—	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Current	I_{IH}	—	—	50	µA
Input Low Current	I_{IL}	—	—	–400	µA
Input Leakage Current	I_L	—	—	50	µA
TTL Outputs:					
Output High Voltage	V_{OH}	2.4	—	—	V
Output Low Voltage	V_{OL}	—	—	0.45	V
Output Short-circuit Current	I_{SC}	–15	—	–85	mA
100 Mbits/s Twisted Pair (TP):					
Input Voltage	V_{DIFF}	—	—	1.5	V
100 Mbits/s Twisted Pair (TP):					
Output Current	V_{DIFF}	19	20	21	mA

Timing Characteristics (Preliminary)

Table 22. MII Management Interface Timing (25 pF Load)

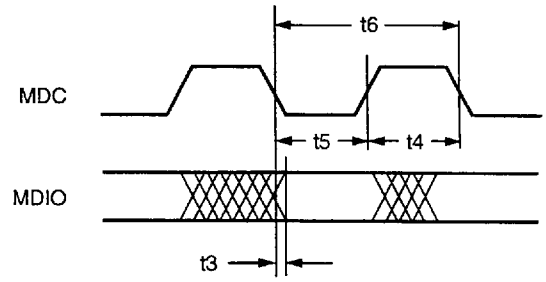
Name	Parameter	Min	Typ	Max	Unit
t1	MDIO Valid to Rising Edge of MDC (setup)	10	—	—	ns
t2	Rising Edge of MDC to MDIO Invalid (hold)	10	—	—	ns
t3	MDC Falling Edge to MDIO Valid (prop. delay)	0	—	40	ns
t4	MDC High*	—	200	—	ns
t5	MDC Low*	40	200	—	ns
t6	MDC Period*	80	400	—	ns

* When operating MDC above 6.25 MHz, MDC must be synchronous with LSCLK and have a setup time of 15 ns and a hold time of 5 ns, with respect to LSCLK.



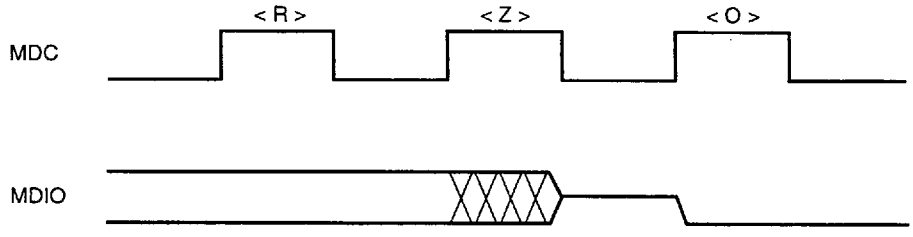
5-4959(F).r1

Figure 8. MDIO Input Timing



5-4960(F).c

Figure 9. MDIO Output Timing



5-5312(F).r1

Note: MDIO turnaround (TA) time is a 2-bit time spacing between the register address field and the data field of a frame to avoid drive contention on MDIO during a read transaction. During a write to the LU2X54FT, these bits are driven to a 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the LU2X54FT during the second bit time.

Figure 10. MDIO During TA (Turnaround) of a Read Transaction

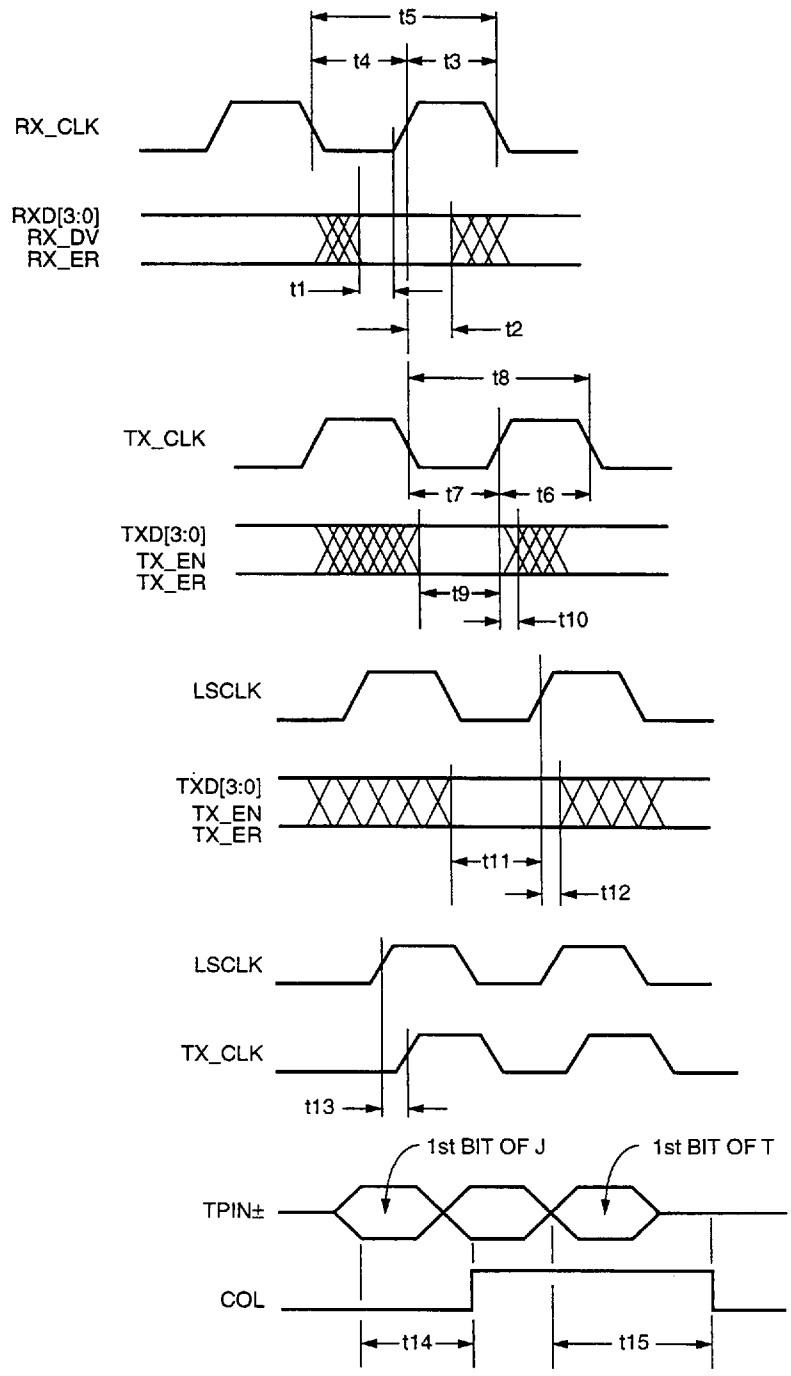
Timing Characteristics (Preliminary) (continued)

Table 23. MII Data Timing (25 pF Load)

Name	Parameter	Min	Typ	Max	Unit
t1	RXD[3:0], RX_ER, RX_DV Valid to RX_CLK High	10	—	—	ns
t2	RX_CLK High to RXD[3:0], RX_DV, RX_ER Invalid	10	—	—	ns
t3	RX_CLK High	14	—	26	ns
t4	RX_CLK Low	14	—	26	ns
t5	RX_CLK Period	—	40	—	ns
t6	TX_CLK High	14	—	26	ns
t7	TX_CLK Low	14	—	26	ns
t8	TX_CLK Period	—	40	—	ns
t9	TXD[3:0], TX_EN, TX_ER, Setup to TX_CLK	15	—	—	ns
t10	TXD[3:0], TX_EN, TX_ER, Hold to TX_CLK	0	—	—	ns
t11	TXD[3:0], TX_ER, TX_EN, Setup to LSCLK*	10	—	—	ns
t12	TXD[3:0], TX_EN, TX_ER, Hold to LSCLK*	0	—	—	ns
t13	TX_CLK Skew from LSCLK	TBD	—	TBD	ns
t14	First Bit of J on TPIN± While Transmitting Data to COL Assert (half-duplex mode)	—	—	170	ns
t15	First Bit of T Received on TPIN± While Transmitting to COL Deasserted (half-duplex mode)	—	—	210	ns

* 100 Mbits/s only.

Timing Characteristics (Preliminary) (continued)



5-5432(F).r3

Figure 11. MII Timing Requirements for LU2X54FT

Timing Characteristics (Preliminary) (continued)

Table 24. 100 Mbits/s MII Transmit Timing

Name	Parameter	Min	Max	Unit
t41	Rising Edge of TX_CLK Following TX_EN Assertion to CRS Assertion	—	40	ns
t42	Rising Edge of TX_CLK Following TX_EN Assertion to TPOUT±	—	60	ns
t43	Rising Edge of TX_CLK Following TX_EN Deassertion to CRS Deassertion	—	40	ns

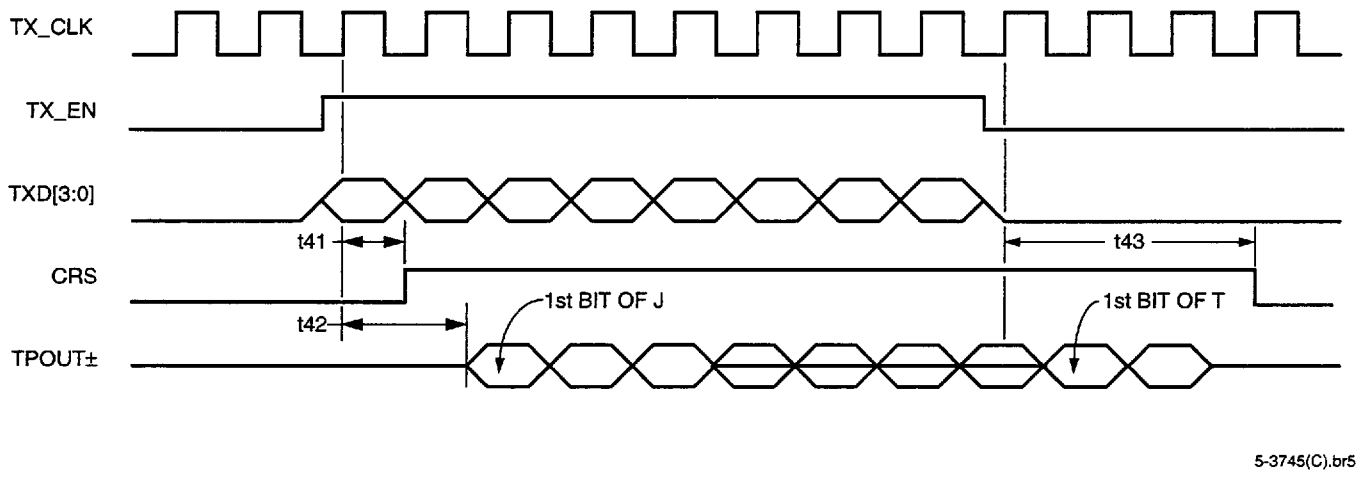


Figure 12. 100 Mbits/s MII Transmit Timing

Timing Characteristics (Preliminary) (continued)

Table 25. 100 Mbits/s MII Receive Timing

Name	Parameter	Min	Max	Unit
t44	TPIN± 1st Bit of J Receive Activity to CRS Asserted	—	170	ns
t45	TPIN± Receive Activity to Receive Data Valid	—	210	ns
t46	TPIN± Receive Activity Cease (1st bit of T) to CRS Deasserted	—	210	ns
t47	TPIN± Receive Activity Cease (1st bit of T) to Receive Data Not Valid	—	210	ns

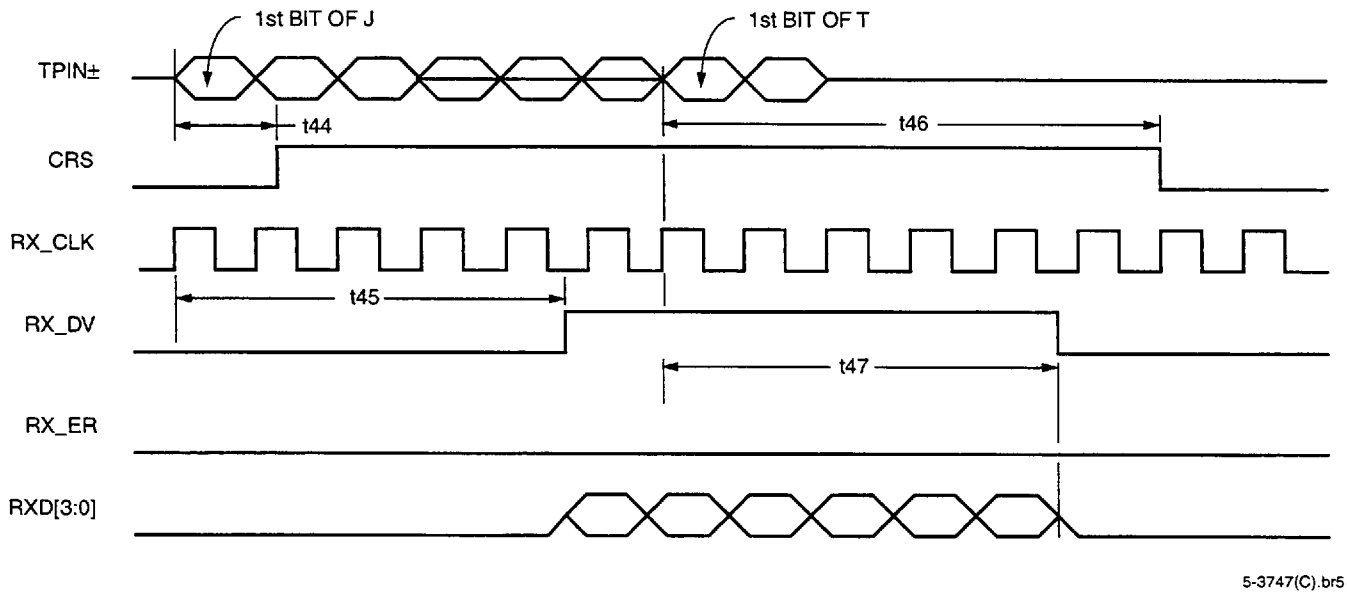
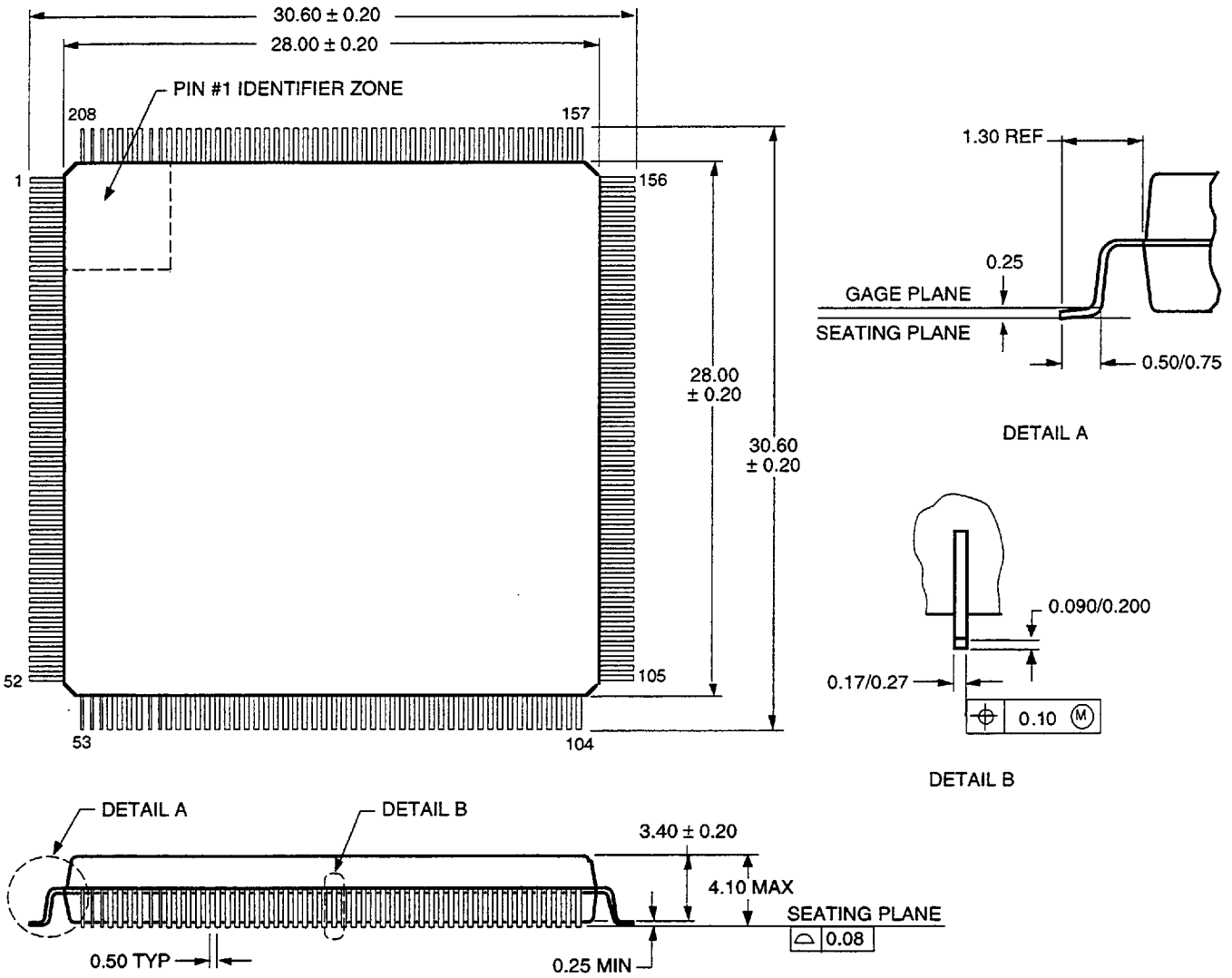


Figure 13. 100 Mbits/s MII Receive Timing

Outline Diagram

208-Pin SQFP

Dimensions are in millimeters.



5-5196(C).r13

Ordering Information

Device Code	Package	Temperature
LU2X54FT	208-Pin SQFP	0 °C to 70 °C