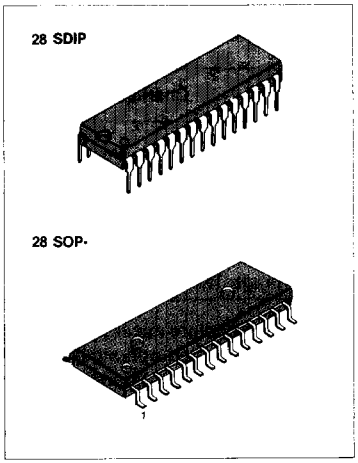
HIGH SPEED TRIPLE D/A CONVERTER 6-BIT TRIPLE, 20 MSPS



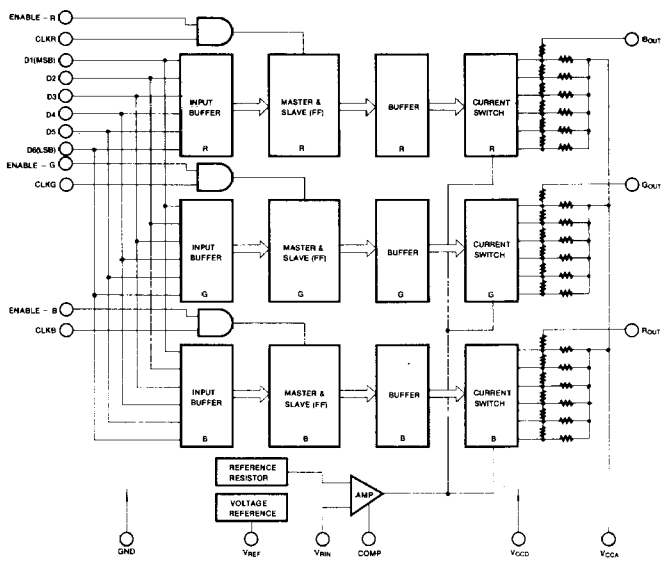
The KDA0406 is a monolithic 6-bit tripple DAC which applies a 2μm bipolar process. The Decoding method and R-2R collector split method are combined to create the device. In the device operating on a single +5V, signal transformation up to 20MSPS (Mega Samples Per Second) is possible. This DAC is designed for video application and has an output dynamic range of 4 to 5V. In order to have less input data lines and package pins, six pins provide input data to three DACs if a clock is enabled. Where the clock is unenabled, its internal registor holds the input data of the previous condition so the analog output in the previous condition is maintained.

All the data input and input signals of the clock and control are controlled by the TTL CMOS level, since there is a built-in registor, the input data can be used by transforming it into an analog signal, after being synchronized into a clock signal, without an additional deglitch circuit. Moreover, the built-in generating circuit for reference voltage provides an easy application of the device.

FEATURES

- **Resolution: 6 Bit**
- **Linearity error: less than ± 1/2 LSB**
- **Maximum conversion rate: 20 MSPS**
- **Analog output dynamic range: 4 – 5V**
- **Data, clock enable input: TTL, CMOS level compatible**
- **Single power supply: 5 ± 0.25V**
- **Low power dissipation: 300 mW (typ.)**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CCA}, V_{CCD}	−0.5 to 6.0	V
Supply Difference	$V_{CCA} - V_{CCD}$	−0.5 to 0.5	V
Digital Input Voltage	V_{DIN}	−0.5 to 6.0	V
Reference Voltage Input	V_{RIN}	3.0 to 6.0	V
Analog Output Voltage	V_{OUT}	3.0 to 6.0	V
Ambient Operating Temperature Range	T_a	−25 ~95	°C
Storage Temperature Range	T_{stg}	−55 ~125	°C

Notes: 1. Absolute maximum ratings are limiting values applied individually, while all other parameters are within specified operating conditions.
2. Functional operation under any of these conditions is not implied.
3. The applied voltage must be current limited to a specified range.
4. The current is specified as positive when flowing into the device.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CCA}, V_{CCD}	4.75	5.00	5.25	V
Supply Difference	$V_{CCA} - V_{CCD}$	−0.05	0	0.05	V
Clock High Time	t_{PWH}	25			ns
Clock Low Time	t_{PWL}	25			ns
Input Data Set-up Time	t_S	15			ns
Input Data Hold Time	t_H	15			ns
Digital Input Voltage, Low	V_{IL}			0.8	V
Digital Input Voltage, High	V_{IH}		2.0		V
Reference Voltage Input	V_{RIN}	3.8	4.0	4.2	V
Compensation Capacitor	C_{COMP}	1			μF
Ambient Operating Temperature Range	T_a	0		70	°C

D.C. ELECTRICAL CHARACTERISTICS WITHIN SPECIFIED CONDITIONS

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	$I_{CCD} + I_{CCA}$	V_{CC} = Max		60	80	mA
Reference Output Voltage	V_{ROUT}	V_{CC} = Typ	3.8	4.0	4.2	V
Reference Output Voltage Variation	V_{ROT}	0°C ~ 70°C			28	mV
Reference Input Current	I_{RIN}	V_{CC} = Max			10	μA
Digital Input Current, Low	I_{IL}	V_{CC} = Max, V_I = 0.4V			− 400	μA
Digital Input Current, High	I_{IH}	V_{CC} = Max, V_I = 2.4V			200	μA
Output Resistance	R_{OUT}	V_{CCA} to A_{OUT}	190	240	290	ohm

A.C. ELECTRICAL CHARACTERISTICS WITHIN SPECIFIED CONDITIONS

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Conversion Rate	f_C	V_{CC} = Min			20	MSPS
Analog Output Delay	t_D	V_{CC} = Min			20	ns
Settling Time	t_{SET}	V_{CC} = Min			40	ns
Rise Time (10%→90%)	t_r	V_{CC} = Typ			10	ns

PERFORMANCE CHARACTERISTICS WITHIN SPECIFIED CONDITIONS

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Integral Linearity Error	E_{LI}	V_{CC} = Typ			±0.8	%
Differential Linearity Error	E_{LD}	V_{CC} = Typ			±0.8	%
Zero-scale Output Voltage	V_{OZS}	V_{CC} = Typ, V_{RIN} = 4.0V	3.9	4.0	4.1	V
Full-scale Output Voltage	V_{OFS}	V_{CC} = Max	V_{CC} − 15	V_{CC}	V_{CC} + 15	mV
Zero-scale Channel Variation	$\triangle V_{CH}$	V_{CC} = Typ, V_{RIN} = 4.0V			30	mV
Differential Phase	DP	f_C = 4 fsc			2	°C
Differential Gain	DG	f_C = 4 fsc			2	%

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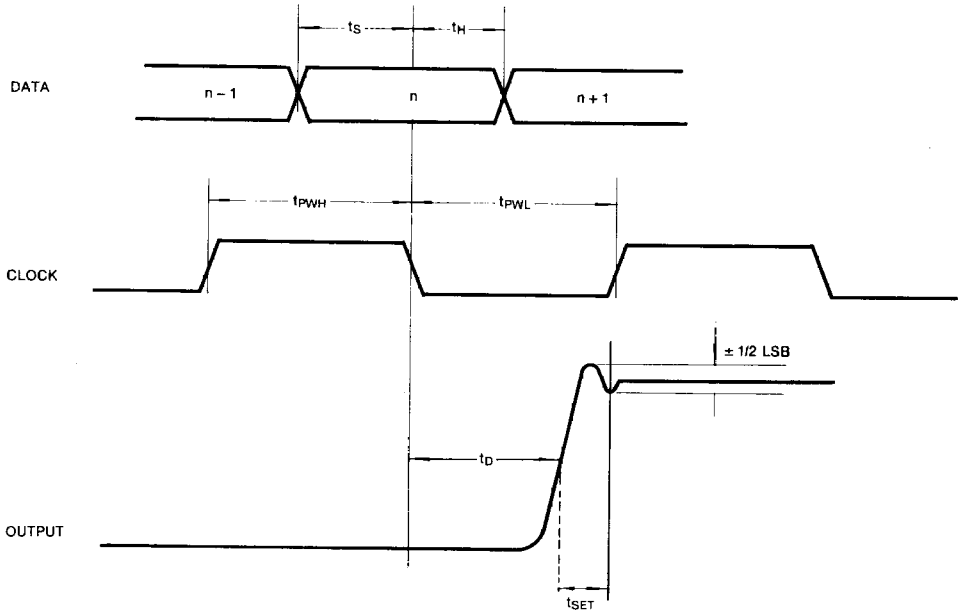
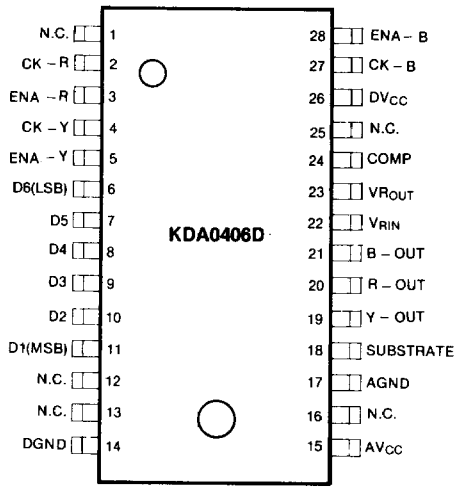
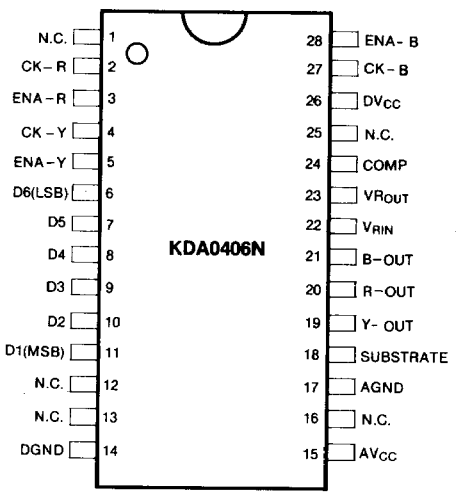
TIMING DIAGRAM



PIN CONFIGURATIONS

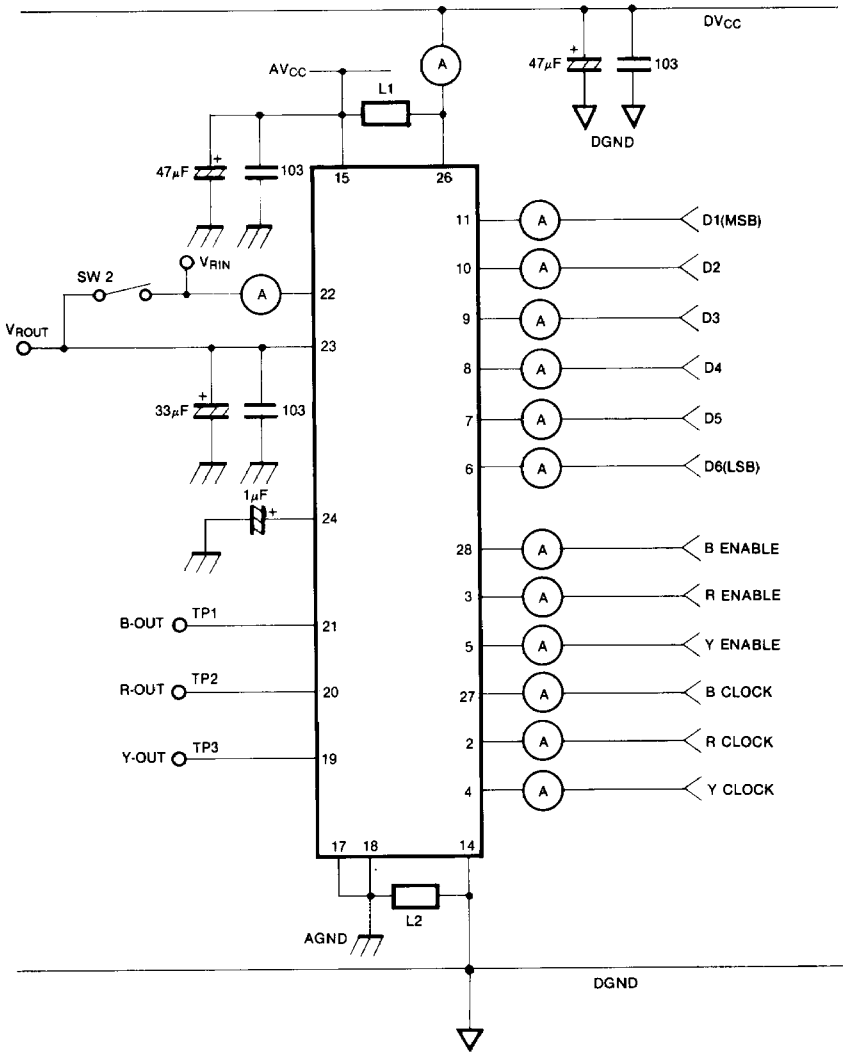


(TOP VIEW)



(TOP VIEW)

KDA0406 D.C. TEST CIRCUIT



KDA0406 A.C. TEST CIRCUIT