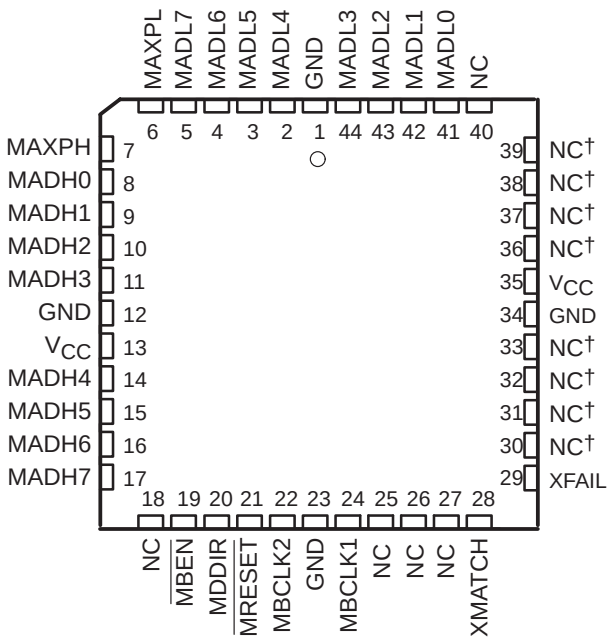
SPWS006 – NOVEMBER 1991

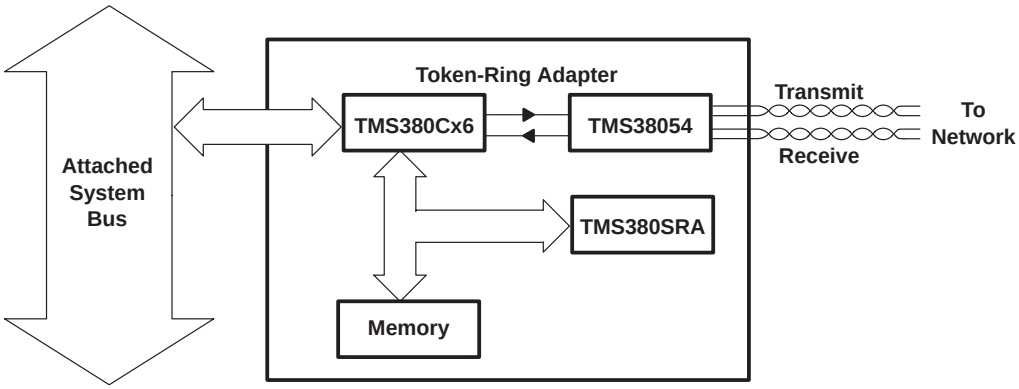
- **Source-Routing Bridge Accelerator for 16-Mbps and 4-Mbps Token-Ring Bridges**
- **Compatible With the IBM Token-Ring Network Architecture**
- **Interfaces Directly to the TMS380Cx6 Second-Generation Network Commprocessor**
- **Provides Automatic Recognition of Source-Routing Field in Token-Ring Frame for Hardware-Accelerated-Frame Copying and High-Performance Bridging**
- **Utilizes TI-Patented Enhanced-Address Copy Option (EACO) Interface of the TMS380Cx6**
- **High-Performance, 1-μm EPIC™ CMOS Technology**
- **44-Pin JEDEC PLCC Surface-Mount Package**

FN PACKAGE
(TOP VIEW)



† These pins must be left externally unconnected.
NC – No internal connection

Token-Ring LAN SRA Applications Diagram



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description

The TMS380SRA source-routing accelerator (SRA) device provides the hardware for direct recognition and parsing of the source-routing field in a token-ring frame. The TMS380SRA is designed to interface directly to the TMS380Cx6. The TMS380SRA searches the received frame for frames that need to be forwarded to the adjacent ring by examining the source-routing field. If a frame is to be forwarded, the frame is copied by the adapter and transferred to the attached system through the system interface of the TMS380Cx6. A second adapter with the TMS380SRA can also be included in the attached system (thus forming a bridge) to provide an identical function for the second ring. Transfer of data between the two rings (bridging) occurs under attached system-software control.

A block diagram of the TMS380SRA is shown in Figure 1. The internal registers fall into two categories: registers that can be set by the host software for the specific bridge parameters for this adapter, and dynamic registers that are loaded with the received frames-routing information as read from the adapter bus transfer. The routing information is compared to the specified bridge parameters, which determines the value to be placed on the XMATCH and XFAIL pins. The memory-interface (MIF) address output during memory cycles is shown in Table 1. Status information is provided on the MADH0–MADH7 signals in the second quarter of the memory cycle (shaded area). MADH6 and MADH7 are the bits that can be used by an EACO device. The information provided in these bits during the second quarter of the memory cycle can be decoded as follows:

MADH6	H	=	The TMS380Cx6 PH RX DMA machine is transferring a word of received frame data to memory.
	L	=	At all other times
MADH7	H	=	The TMS380Cx6s PH RX DMA machine is transferring the first word of a new received frame to memory. In a token-ring frame, the first word contains the AC and FC fields.
	L	=	At all other times

The decode of the rest of the status information is shown in Table 2 and Table 3.

The TMS380SRA is available in a 44-lead plastic chip-carrier package (FN suffix) and is characterized for operation from 0°C to 70°C (L suffix). The electrostatic-discharge protection of the TMS380SRA is rated at 500 V human-body model (HBM).

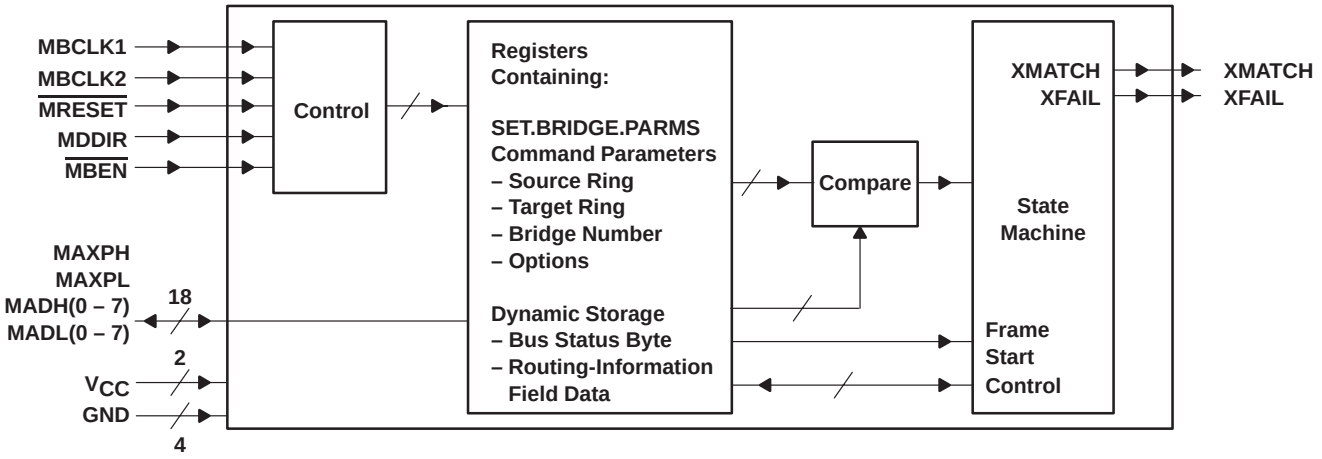

Figure 1. TMS380SRA Block Diagram

Table 1. TMS380Cx6 Address Output During Memory Cycle

PIN	FIRST QUARTER	SECOND QUARTER	REST OF CYCLE
MAX0†	AX0	A12	A12
MAXPH	AX1	AX0	Parity
MAX2†	AX2	A14	A14
MAXPL	AX3	AX2	Parity
MADH0	AX4	Status	Data
MADH1	A0	Status	Data
MADH2	A1	Status	Data
MADH3	A2	Status	Data
MADH4	A3	Status	Data
MADH5	A4	Status	Data
MADH6	A5	Status	Data
MADH7	A6	Status	Data
MADL0	A7	AX4	Data
MADL1	A8	A0	Data
MADL2	A9	A1	Data
MADL3	A10	A2	Data
MADL4	A11	A3	Data
MADL5	A12	A4	Data
MADL6	A13	A5	Data
MADL7	A14	A6	Data
MROMEN†	ROMEN	A13	A13

† These signals do not attach to the TMS380SRA; therefore, there are no corresponding pins.

Table 2. Status Information on MADH0 – MADH7

SECOND-QUARTER MEMORY CYCLE	FUNCTION
MADH0	Code/$\overline{\text{data}}$‡
MADH1	Indicates which internal module of the TMS380Cx6 has ownership of the adapter memory bus (see Table 3)‡.
MADH2	
MADH3	
MADH4	
MADH5	SIF DMA active
MADH6	PH RX DMA cycle
MADH7	New RX frame

‡ To the TMS380SRA, these bits are don't care.

Table 3. Decode of Status Information on MADH1 – MADH4

MADH1	MADH2	MADH3	MADH4	REPRESENTATION
0	0	0	0	DRAM controller
0	0	0	1	Not assigned
0	0	1	0	PH TX DMA machine
0	0	1	1	PH RX DMA machine
0	1	0	0	PH TX buffer manager
0	1	0	1	PH RX buffer manager
0	1	1	0	SIF DIO machine
0	1	1	1	SIF DMA machine
1	0	0	0	CP (uses bus)
1	0	0	1	CP (does not use bus)
1	0	1	0	Not assigned
1	0	1	1	Not assigned
1	1	0	0	Not assigned
1	1	0	1	Not assigned
1	1	1	0	Program debug controller
1	1	1	1	No memory access

† To the TMS380SRA, these bits are don't care.

Pin Functions

PIN NAME	NO.	I/O/Z‡	DESCRIPTION
MADHO MADH1 MADH2 MADH3 MADH4 MADH5 MADH6 MADH7	8 9 10 11 14 15 16 17	I/O	Adapter-memory address, data and status bus – high byte. For the first quarter of the adapter-memory cycle, these bus lines carry address bits AX4 and A0 to A6; for the second quarter, they carry status bits; and for the third and fourth quarters, they carry data bits 0 to 7. The most significant bit is MADH0 and the least significant bit is MADH7. Memory Cycle Signal: 1Q AX4, A0 – A6; 2Q Status; 3Q D0 – D7; 4Q D0 – D7
MADLO MADL1 MADL2 MADL3 MADL4 MADL5 MADL6 MADL7	41 42 43 44 2 3 4 5	I/O	Adapter-memory address, data and status bus – low byte. For the first quarter of the adapter-memory cycle these bus lines carry address bits A7 to A14; for the second quarter, they carry address bits AX4 and A0 to A6; and for the third and fourth quarters, they carry data bits 8 to 15. The most significant bit is MADL0 and the least significant bit is MADL7. Memory Cycle Signal: 1Q AX7 – A14; 2Q AX4, A0 – A6; 3Q D8 – D15; 4Q D8 – D15
MAXPH	7	I/O	Adapter-memory-extended address and parity – high byte. For the first quarter of a memory cycle, carries the extended address bit (AX1); for the second quarter of a memory cycle, it carries the extended address bit (AX)); and for the last half of the memory cycle, it carries the parity bit for the high data byte. Memory Cycle Signal: 1Q AX1; 2Q AX0; 3Q Parity; 4Q Parity
MAXPL	6	I/O	Adapter-memory-extended address parity – low byte. For the first quarter of the adapter memory cycle, MAXPL carries the extended address bit (AX3), for the second quarter of a memory cycle, it carries extended address bit (AX2); and for the last half of the memory cycle, it carries the parity bit for the low data byte. Memory Cycle Signal: 1Q AX3; 2Q AX2; 3Q Parity; 4Q Parity

‡ Denotes input/output/high-impedance state

Pin Functions (Continued)

PIN NAME	NO.	I/O/Z†	DESCRIPTION
MBCLK1 MBCLK2	24 22	I	Adapter-bus clock 1 and adapter-bus clock 2. MBCLK1 and MBCLK2 are references for all adapter-bus transfers. MBCLK2 lags MBCLK1 by a quarter of a cycle. These clocks operate at 8 MHz for a 64-MHz OSCIN (on the TMS380Cx6) and 6 MHz for a 48-MHz OSCIN (on the TMS380Cx6), which is twice the memory cycle rate. The MBCLK signals are always a divide-by-8 of the OSCIN (on the TMS380Cx6) frequency.
$\overline{\text{MBEN}}$	19	I (see Note 1)	Buffer enable. $\overline{\text{MBEN}}$ enables the bidirectional buffer outputs on the MADH, MAXPH, MAXPL, and MADL buses during the data phase. $\overline{\text{MBEN}}$ is used in conjunction with MDDIR, which selects the buffer output direction. H = Buffer output disabled L = Buffer output enabled
MDDIR	20	I	Data direction. MDDIR is used as a direction control for the bidirectional bus drivers from the TMS380Cx6. MDDIR becomes valid before $\overline{\text{MBEN}}$ becomes active. H = TMS380Cx6 memory-bus write L = TMS380Cx6 memory-bus read
$\overline{\text{MRESET}}$	21	I (see Note 1)	Memory bus reset. $\overline{\text{MRESET}}$ is a reset signal generated when either the ARESET bit in the SIFACL register is set or the $\overline{\text{SRESET}}$ is asserted. This signal is used for resetting external adapter bus glue logic and the TMS380SRA. H = External logic not reset L = External logic reset
XFAIL	29	O	External fail-to-match. The TMS380SRA device uses XFAIL to indicate to the TMS380Cx6 that it should not copy the data frame nor set the ARI/FCI bits due to an external address match. The ARI/FCI bits may still be set by the TMS380Cx6 due to an internal address match (see table in XMATCH description). H = No address match by TMS380SRA L = TMS380SRA armed state
XMATCH	28	O	External match. The TMS380SRA device uses XMATCH to indicate to the TMS380Cx6 to copy the data frame and set the ARI/FCI bits. H = Address match recognized by TMS380SRA L = TMS380SRA armed state XMATCH / XFAIL / Function 0 / 0 / Armed (processing frame data) 0 / 1 / Do *not* externally match the frame 1 / 0 / Copy the frame 1 / 1 / Do *not* externally match the frame Hi-Z / Hi-Z / Reset state (TMS380SRA is in the reset state
V_{CC} (2 pins)	13,35	5-V supply voltage	
GND (4 pins)	1,12,23,34	Ground	
NC (13 pins)		These pins must be unconnected.	

† Denotes input/output/high-impedance state

NOTE 1: Pin has an internal pullup device to maintain a high voltage level when left unconnected (no etch or loads)

operation

The TMS380SRA is designed to be interfaced with the TMS380Cx6 on DRAM-based adapters operating at 4-MHz adapter-bus speed with no external glue logic required. In adapter designs utilizing EPROMs or other devices in addition to DRAMs and a BIA PROM, it may be necessary to buffer the DRAMs in order to reduce the total bus loading below the maximum output load capacitance (50 pF) of the TMS380SRA.

The TMS380SRA control registers are mapped into the TMS380Cx6 memory map at all times, and no external chip-select signal is used. The adapter software controls access to these registers through the SET.BRIDGE.PARMS command (>0010), as described in the TMS380 Second-Generation Token-Ring User's Guide (SPWS005).

operation (continued)

The TMS380SRA is reset by a low-level signal on $\overline{\text{MRESET}}$. The TMS380Cx6 forces a $\overline{\text{MRESET}}$ active during a hardware or software reset of the adapter. In the reset state of the TMS380SRA, XMATCH and XFAIL are in the high-impedance state.

The TMS380SRA is also reset by the SET.BRIDGE.PARMS command before loading the supplied values and conditions for the TMS380SRA to use. If the SET.BRIDGE.PARMS command is supplied with invalid values, the values are not loaded and the device remains in the reset state (disabled).

The TMS380SRA should be placed such that the length of the signal lines between it and the TMS380Cx6 does not exceed 7 cm in length. Figure 2 illustrates the TMS380Cx6 to TMS380SRA interface.

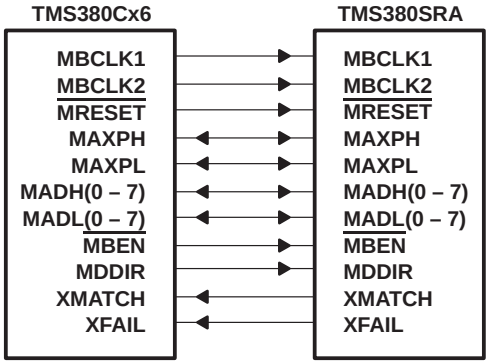

Figure 2. TMS380Cx6 to TMS380SRA Interface

bridging

Bridging is the process of passing information from one physical ring to another and is achieved by having a token-ring adapter attached to each ring but sharing a common attached-system processor. Each adapter monitors frames received on its ring for frames to be forwarded via its colleague to the other ring. When such a frame is detected, the transfer takes place via the attached-system processor. Each of these bridge adapters has a designator composed of its own ring number and its individual bridge number, and each also knows the ring number and bridge number of its colleague. This principle of the bridge is illustrated in Figure 3. Bridge #3 on ring 1 looks for frames to be forwarded to ring 2, and similarly bridge #3 on ring 2 looks for frames to forward to ring 1.

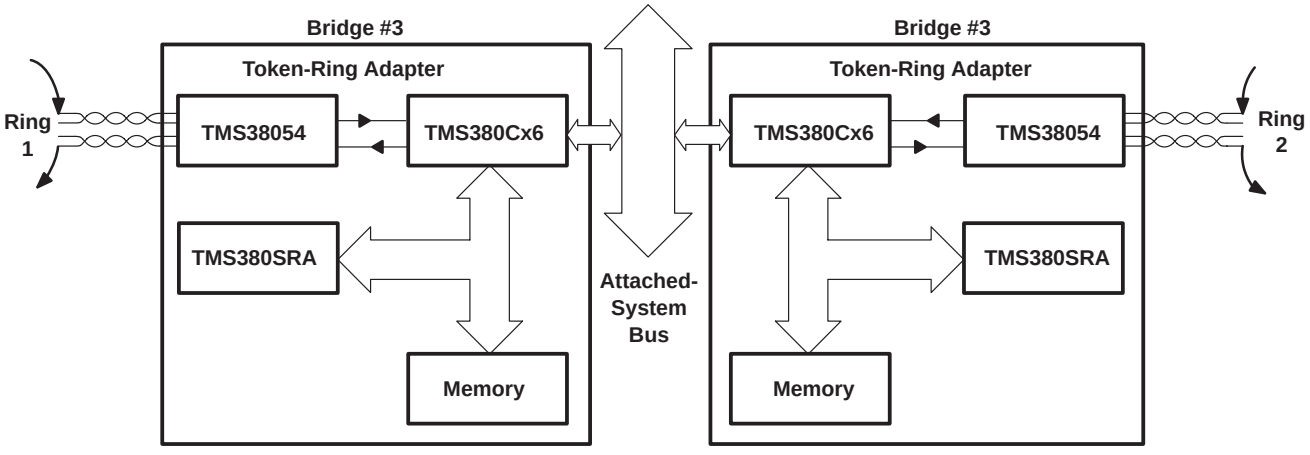

Figure 3. SRA Bridge

bridging (continued)

The TMS380SRA source-routing accelerator provides for high-speed frame copying and forwarding to the attached system. The SRA monitors incoming frames and asserts either XMATCH and XFAIL for each frame to indicate whether the frame should be bridged. Asserting XMATCH enables the TMS380Cx6 commprocessor to copy the frame, set the address recognize indicator (ARI) bits in the frame status (FS) byte, and set frame copied indicator (FCI) bits in the FS if the frame is copied. The attached system provides the appropriate frame building and forwarding services as well as the bridge-control functions described in the IBM token-ring network architecture reference.

The frame format containing the routing information is shown in Figure 4. The most significant bit of the source-address field is transmitted as a one, indicating that the frame contains routing information. If this bit is zero, the TMS380SRA does not copy the frame. The routing-information field immediately follows the source address and contains a 2-byte routing-control field and additional 2-byte route designators. The TMS380SRA supports up to fifteen route designators (see Note). The frame data, CRC field, end deliminator, and frame status follow the routing-information field.

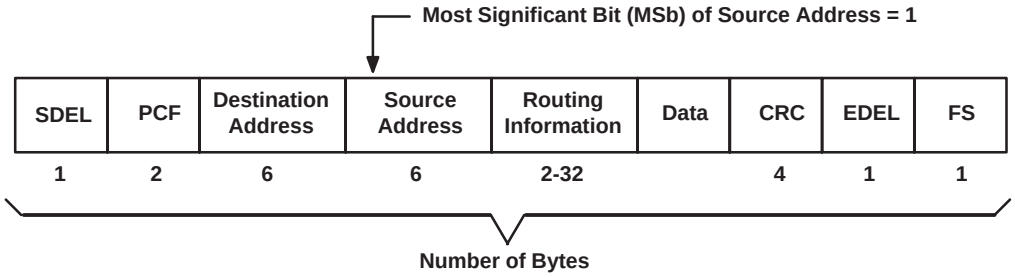

Figure 4. Frame Format Containing Routine Information

NOTE: IBM's current token-ring source-routing architecture supports only an 18-byte routing-information field. Texas Instruments Release 1.00, 2.00 and 2.10 second-generation adapter software will not transmit frames with routing-information fields longer than 18 bytes.

The routing-information field is expanded in Figure 5. If the frame is routed via a particular sequence of bridges (i.e., nonbroadcast), all the required route designators are provided by the token-ring node sourcing the frame. If the frame is a broadcast and meets requirements for forwarding (as determined by the routing-control field), the TMS380SRA copies the frame and the attached system adds the route designator of the next ring to the end of the routing-information field and transmits the frame through the colleague adapter.

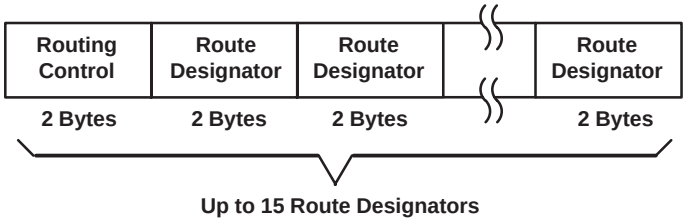

Figure 5. Routing-Information Field

bridging (continued)

The routing-control field contains two bytes of information as shown in Figure 6. Bits 0–2 indicate if the frame is a broadcast, and if so, what type. Bits 3–7 are the length field and indicate the length of the routing-information field, including the routing-control field. Bit 8 is a direction bit that, for nonbroadcast frames, indicates the order in which route designators should be interpreted by bridges routing the frame. Bits 9–11 are the largest frame-indicator bits, which can be modified by the attached system to indicate the maximum frame size that can travel via that bridge. The TMS380SRA ignores bit 2 in the broadcast-indicator field, bits 9–11 in the largest frame size field, and bits 12–15 in the reserved field.

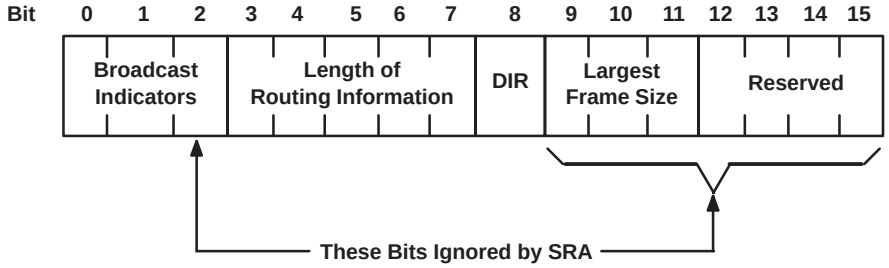

Figure 6. Routing-Control Field

Each ring in a multiple-ring network is assigned a unique ring number, and each bridge is assigned a bridge number, which may or may not be unique. Together the ring and bridge number form a route designator as shown in Figure 7. The two bytes of the route designator are divided into two parts. The least significant K-bits are the individual bridge number, and the most significant K-bits are the ring number. The individual bridge-number portion allows parallel bridges to exist to share traffic between two particular rings. The value of K is set using the PARTITION_LENGTH parameter of the SET.BRIDGE.PARMS command.

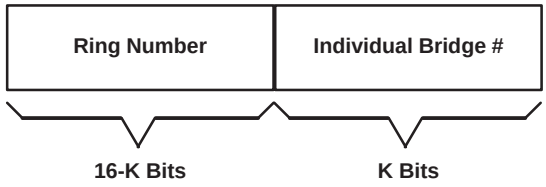

Figure 7. Route-Designator Field

frame-copying algorithm

Frame copying by the TMS380SRA is controlled by register-bit settings in the TMS380SRA and the incoming-frame routing-information field. If a frame is to be copied, the TMS380SRA asserts XMATCH, otherwise XFAIL is asserted. The TMS380SRA copies only frames with the source-routing-indicator bit set in the source address. The major parsing function is controlled by the broadcast bit settings of the incoming frame in the routing-control field [the broadcast indicator bits of the routing-control field (bits 0–2)]. The frame-copy algorithms are as follows:

0xx — Indicates that the routing-information field contains a specific route for the frame to travel through the network (nonbroadcast routing). For direction bit equal zero, the TMS380SRA examines the route designators for two adjacent designators containing its own adapter ring number and bridge number, and its colleague adapter's ring number. For direction bit equal one, the TMS380SRA examines the route designators for two adjacent designators containing its own adapter ring number, and its colleague adapter's ring number and bridge number. If these combinations are detected, the frame is copied. If no such match is found, the TMS380SRA does not enable frame coying. The TMS380SRA uses the direction bit to determine the required

order in which the routing information should be interpreted. This allows a frame to be returned to the sender without having to reorder the designators by changing the direction bit. If the direction bit is zero, the designators are read from left to right; if the direction bit is one, from right to left.

The TMS380SRA does not check that the same ring number appears more than once in the routing information. If rings 1, 2, and 3 are bridged together as a triangle, and a frame contains a sequence of designators 1, 2, 3, 1, it circulates indefinitely. Attached system software should check for this condition before forwarding the frame.

10x — Indicates that the frame is an all-routes broadcast. Every bridge forwards the frame to the next ring if it has not already circulated on that ring or has not already traversed the maximum number of bridges permitted by the protocol. (IBM token-ring network architecture reference limits this count to seven.) If the network is configured so that there are several routes to the destination adapter, then as many copies are received by that adapter as there are routes. The ring number in the final route designator of a broadcast should be the same as the ring number of the token-ring adapter bridge that receives it for forwarding. the TMS380SRA does not copy an all-routes broadcast frame with an incorrect final-route designator.

With broadcast frames, the value in the length field grows as the frame traverses the network. The first bridge to forward a frame adds 4 to the value and appends its designator (ring number and bridge number) and its colleague's ring number to the routing-information field, leaving its colleague's bridge number as all zeros. Subsequent bridges forwarding the frame add 2 to the value of the length field, add their bridge number into the all zeros bridge number part of the received final designator, and append their colleague's designator to the routing-information field, again leaving the colleague's bridge number portion as all zeros.

11x — Indicates that the frame is a single-route broadcast. Only bridges that are set up to transfer single-route broadcast frames consider the frame for forwarding. The TMS380SRA can be configured to copy single-route broadcast frames using the SET.BRIDGE.PARMS command. Frames are copied by the TMS380SRA under the same conditions as for all-route broadcasts. There is nothing inherent in the frame to limit its propagation to just one route. The network manager must select which bridges forward single-route broadcast frames and inform the bridges appropriately.

length-field requirements

The five length bits in the routing-control field indicate, in bytes, the length of the routing-information field. The minimum value is 2, which is how all bridge-broadcast frames originate, and the maximum value supported by the TMS380SRA is 30. All odd values, 0, 4, and values greater than 30 result in frames not being copied by the TMS380SRA. A value of 4 is illegal since this would mean there was only one route designator present. A value of 2 is not copied by the TMS380SRA for nonbroadcast frames.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . –0.5 V to 7 V
Input voltage range . . . . . –0.5 V to 7 V
Output voltage range . . . . . –0.5 V to 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: Voltage values are with respect to GND.

recommended operating conditions

The TMS380SRA is designed to interface directly to the TMS380Cx6 token-ring commprocessor, Refer to the *TMS380 Second-Generation Token Ring User's Guide* (SPWS005) for details on TMS380Cx6 operation.

All inputs to the TMS380SRA have TTL compatible levels. All outputs are CMOS compatible; therefore, like-named pins on the TMS380SRA and TMS380Cx6 should be connected together.

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{CC}	Supply voltage, GND (see Note 3)		0	0	0	V
I_{OH}	High-level output current	Except XMATCH and XFAIL			8	mA
		XMATCH and XFAIL			2	
I_{OL}	Low-level output current (see Note 4)	Except XMATCH and XFAIL			–8	mA
		XMATCH and XFAIL			–2	
T_A	Operating free-air temperature		0		70	°C
C_L	Output load capacitance	MADH, MADL, MAXPH, MAXPL			50	pF
		XFAIL, XMATCH			20	

NOTES: 3. All GND pins should be routed to minimize inductance to system ground.
4. The algebraic convention, where the more negative (less positive) limit is designated as a minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS (see Note 5)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 5.5 V	2			V
V_{IL}	Low-level input voltage, TTL-level signal	V_{CC} = 4.5 V			0.8	V
V_{OH}	High-level output voltage, TTL-level signal	V_{CC} = MIN, I_{OL} = MAX	3.7			V
V_{OL}	Low-level output voltage, TTL-level signal	V_{CC} = MIN, I_{OL} = MAX			0.5	V
I_{CC}	Supply current	V_{CC} = MAX		60	160	mA
C_i	Input capacitance, any input				15	pF
C_o	Output capacitance, any output or input/output				15	pF

NOTE 5: For conditions shown as MIN or MAX, use the appropriate value specified under the recommended operating conditions.

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