JEIDA Ver. 3 STATIC RAM

VARIATION

Part Number	Memory Size	Description
AWB129JS10	128K Bytes	64K × 16 bits JEIDA Ver.3 MIX CMOS SRAM CARD
AWB257JS10	256K Bytes	128K × 16 bits JEIDA Ver.3 MIX CMOS SRAM CARD
AWB513JS10	512K Bytes	256K × 16 bits JEIDA Ver.3 MIX CMOS SRAM CARD

OUTLINE OF FUNCTIONS AND FEATURES

(1) This memory card conforms to JEIDA Ver.3.
(2) Size of the card
    Width : 54.0 mm
    Length : 85.6 mm
    Thickness : 3.3 mm
(3) Includes exclusive IC's for the control of I/O and power functions.
(4) Digital output for the condition of the battery.
(5) A write protect switch for protection from accidental overwriting.
(6) Locking mechanism for battery holder.
(7) Replaceable battery. (replace only when power is supplied.)
(8) Card Type: 68-pin Two-piece Type.

MAXIMUM RATING

Symbol	Description	Note	Min	Max	Unit
V_{CC}	Supply voltage		–0.5	7.0	V
V_{IN}	Input signal voltage	1	–0.5	V_{CC} + 0.5	V
V_{OUT}	Output signal voltage		–0.5	V_{CC}	V
T_{OPR}	Operating temperature		0	60	°C
T_{STR}	Storage temperature	2	–20	60	°C
HUM	Humidity	3	10	90	%
P_D	Power dissipation			2	W
V_{BAT}	Battery voltage		–0.5	7.0	V

Notes: 1. Under 7.0 V
2. Without data back-up
3. No dew condition

CAPACITANCE (Ta = 25°C, V_{IN}/V_{OUT} = 0 V, f = 1 MHz)

Symbol	Description	Min	Typ	Max	Unit
C1	Input capacitance		10	14	pF
C2	Input/output capacitance		10	14	pF

Note: The above figures are for reference only

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Description	Min	Typ	Max	Unit
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{BAT}	Battery voltage	2.5	—	—	V
V_{IH}	High level input voltage	2.2	—	V_{CC} + 0.3	V
V_{IL}	Low level input voltage	–0.3	—	0.6	V

DC CHARACTERISTICS (V_{CC} = 5 V, Ta = 25°C)

Symbol	Description	Object	Condition	Min	Typ	Max	Unit
I_{LI}	Low level input current	1,3	V_{IN} = 0 V	–2	—	2	µA
		2		–0.53	—	–0.48	mA
I_{HI}	High level input current	1, 2, 3	V_{IN} = 5 V	10	—	100	µA
V_{OH}	High level output voltage	3, 4, 5	I_{OH} = –2.0 mA	4.0 V_{CC} –0.6	—	—	V
V_{OL}	Low level output voltage	3, 4, 5	I_{OL} = 6.0 mA	—	—	V_{SS} +0.4	V
I_{OZ}	Off-state leakage current	4, 5		–1	—	1	µA

Object :
1. A0 to A18, OE
2. CE1, CE2, REG, WE
3. D0 to D15
4. V_{BAT}
5. WP

CURRENT CONSUMPTION AND BATTERY VOLTAGE DETECT
(Ta = 25°C, V_{CC} = 5 V, V_{BAT} = 3 V)

Symbol	Description	Condition		Min	Typ	Max	Unit
I_{STBY}	Standby current	CE = V_{IH}, Other = V_{IL}/V_{IH}		1.0	2.50	3.20	mA
I_{ACT}	Active current	CE = V_{IL}, I_{OUT} = 0 mA, Other = V_{IL}/V_{IH}	f = 1 MHz	—	40	50	mA
			f = Max	—	—	145	mA
I_{BAT1}	Back-up current 1 Ta = 25°C	V_{CC} = 0 V, V_{BAT} = 3 V	128KB	—	1.0	2.5	µA
			256KB	—	1.8	5.0	µA
			512KB	—	3.5	10.0	µA
I_{BAT2}	Back-up current 2 Ta = 0 to 60°C	V_{CC} = 0 V, V_{BAT} = 3 V	128KB	—	—	40	µA
			256KB	—	—	80	µA
			512KB	—	—	160	µA
V_{INL}	Input detect voltage	V_{IN} V_{CC} –> 0 V		4.05	4.20	4.35	V
V_{INH}		V_{IN} 0 V –> V_{CC}		4.15	4.30	4.45	V
DV_{IN}	Hysteresis width	V_{INH} – V_{INL}		50	100	200	mV
V_{BATL}	Battery detect voltage	V_{BAT} V_{CC} –> 0 V		2.60	2.70	2.80	V
V_{BATH}		V_{BAT} 0 V –> V_{CC}		2.65	2.75	2.85	V
DV_{BAT}	Hysteresis width	V_{BATH} – V_{BATL}		—	50	100	mV

OPERATING MODES

Mode	A0	CE1	CE2	OE	WE	D0 to D7	D8 to D15
Standby	*	VIH	VIH	*	*	HZ	HZ
Even data read	VIL	VIL	VIH	VIL	VIH	OUTPUT	HZ
Odd data read	VIH	VIL	VIH	VIL	VIH	OUTPUT	HZ
Even data write	VIL	VIL	VIH	VIH	VIL	INPUT	HZ
Odd data write	VIH	VIL	VIH	VIH	VIL	INPUT	HZ
Word read	*	VIL	VIL	VIL	VIH	OUTPUT	OUTPUT
Word write	*	VIL	VIL	VIH	VIL	INPUT	INPUT

Notes : HZ = High impedance
* = Input is VIL or VIH

REGISTER OPERATION/CARD INFORMATION

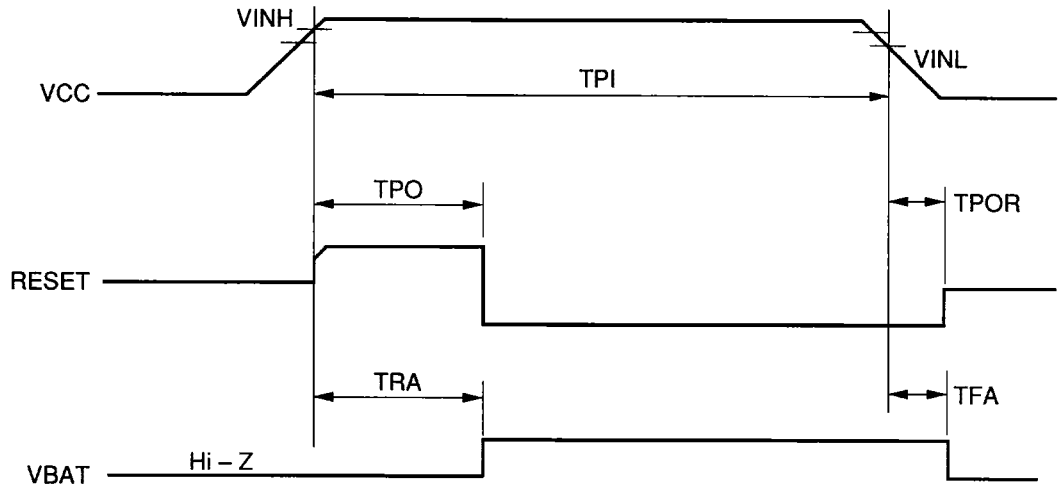
Mode	A0	A1 to A7	CE1	CE2	OE	REG	D0 to D7	D8 to D15
Even data read	VIL	VIL	VIL	VIH	VIL	VIL	OUTPUT	Hi - Z
Odd data read	VIH	VIL	VIL	VIH	VIL	VIL	OUTPUT	Hi - Z
Word data read	*	VIL	VIL	VIL	VIL	VIL	OUTPUT	OUTPUT

Notes : * = Input is VIL or VIH

Part Number	Even Register Data	Odd Register Data
AWB129JS10	58H	0CH
AWB257JS10	68H	0CH
AWB513JS10	78H	0CH

CHARACTERISTICS OF POWER CONTROL (Ta = 25°C, VCC = 5 V)

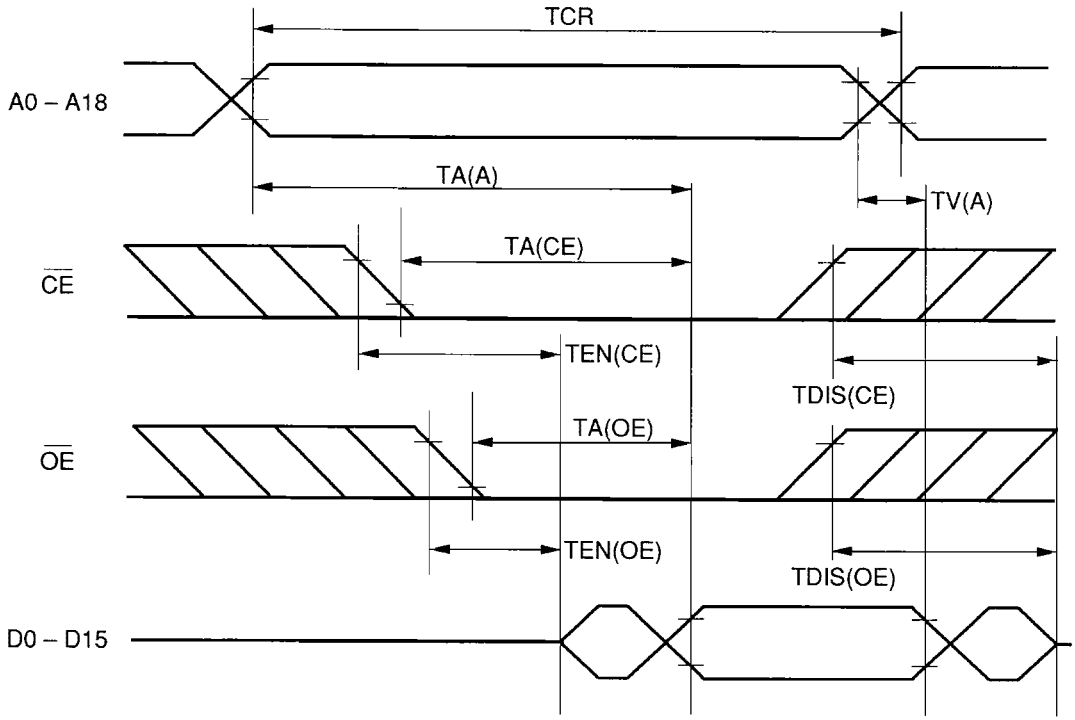
Symbol	Parameter	Condition	Min	Typ	Max	Unit
TPO	Delay time after power on	VCC = 4.20 - >4.75 V	5	10	15	ms
TPDR	Delay time after power off	VCC = 4.75 - >4.10 V	—	2.0	10	µs
TPI	Input pulse width	—	1	—	—	ms
TRA	Rising time of VBAT output	—	5	10	15	ms
TFA	Falling time of VBAT output	—	—	0.1	0.5	µs



AC CHARACTERISTICS AT READ

Symbol	Parameter	Min	Max	Unit
TCR	Read cycle time	250	—	ns
TA (A)	Address access time	—	250	ns
TA (CE)	Card enable access time	—	250	ns
TA (OE)	Output enable access time	—	125	ns
TDIS (CE)	Output disable time from card enable	—	100	ns
TDIS (OE)	Output disable time from output enable	—	100	ns
TEN (CE)	Output enable time from card enable	10	—	ns
TEN (OE)	Output enable time from output enable	10	—	ns
TV (A)	Valid data hold time from address invalid	10	—	ns

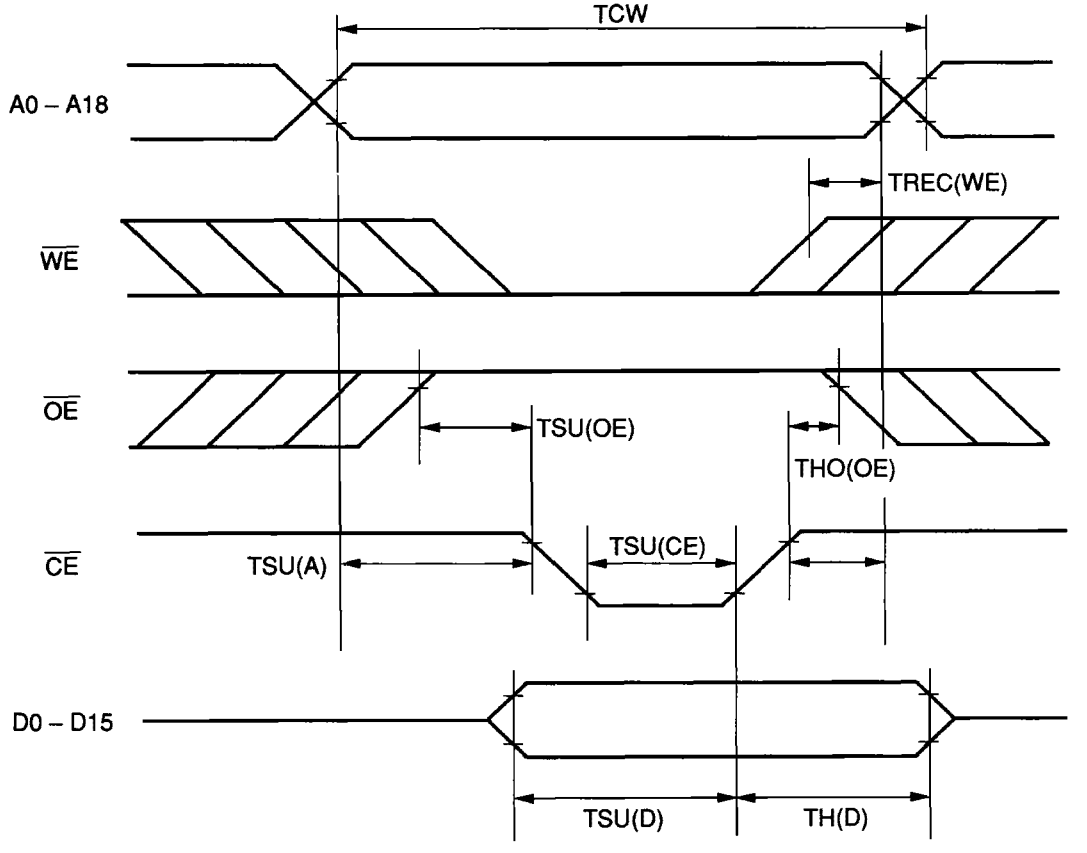
READ TIMING



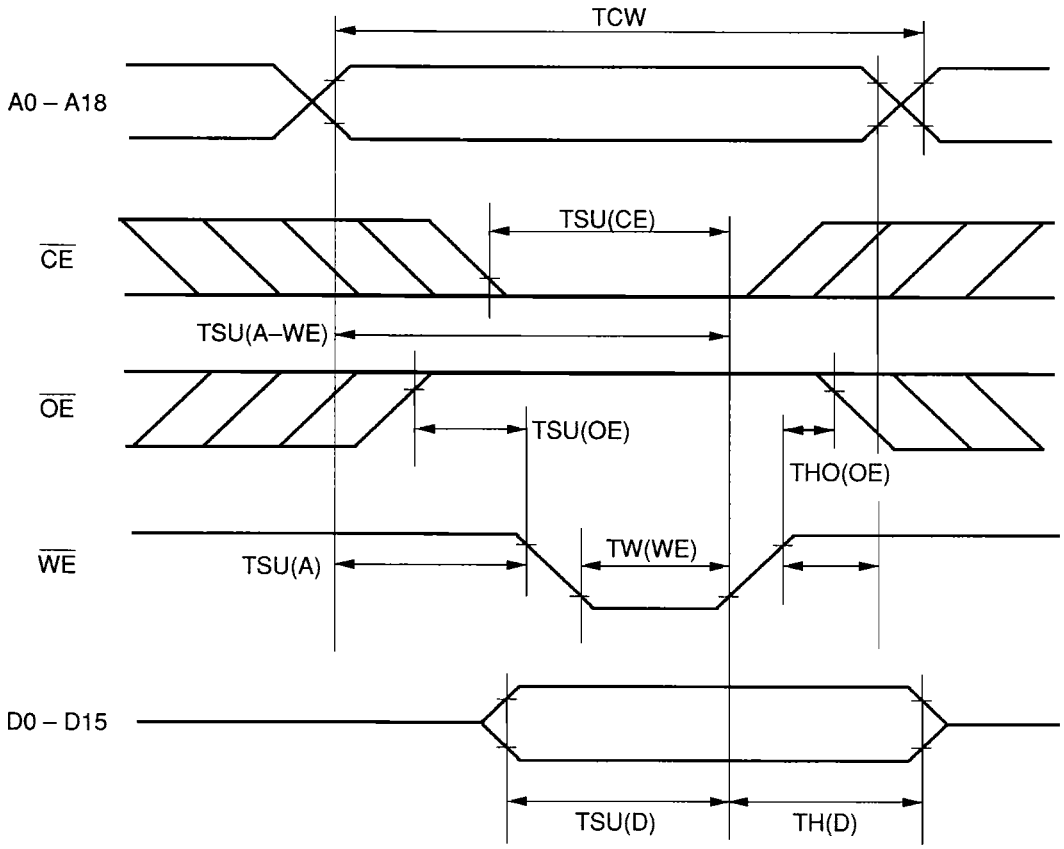
AC CHARACTERISTICS AT WRITE

Symbol	Parameter	Min	Max	Unit
TCW	Write cycle time	250	—	ns
TW(WE)	Write pulse width	150	—	ns
TSU(A)	Address setup time	30	—	ns
TSU(A-WEH)	Address setup time to end write	180	—	ns
TSU(CE)	Card enable setup time	180	—	ns
TSU(D)	Data setup time	80	—	ns
TH(D)	Data hold time	30	—	ns
TREC(WE)	Write recovery time	30	—	ns
TSU(OE)	Output enable setup time	10	—	ns
THO(OE)	Output enable hold time	0	—	ns

WRITE TIMING (CE CONTROLLED WRITE)



WRITE TIMING (WE CONTROLLED WRITE)



PIN ASSIGNMENT

Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	GND	23	A6	46	A17
2	D3	24	A5	47	A18
3	D4	25	A4	48	NC
4	D5	26	A3	49	NC
5	D6	27	A2	50	NC
6	D7	28	A1	51	VCC
7	$\overline{CE1}$	29	A0	52	VCC
8	A10	30	D0	53	NC
9	$\overline{OE}$	31	D1	54	NC
10	A11	32	D2	55	NC
11	A9	33	WP	56	NC
12	A8	34	GND	57	NC
13	A13	35	GND	58	NC
14	A14	36	$\overline{CD1}$	59	NC
15	$\overline{WE}$	37	D11	60	NC
16	NC	38	D12	61	$\overline{REG}$
17	VCC	39	D13	62	NC
18	VCC	40	D14	63	VBAT
19	A16	41	D15	64	D8
20	A15	42	$\overline{CE2}$	65	D9
21	A12	43	NC	66	D10
22	A7	44	NC	67	$\overline{CD2}$
		45	NC	68	GND

Notes: NC = No connect
A16 : AWB129, AWB257, AWB513
A17 : AWB257, AWB513
A18 : AWB513