

# MM54HC4511/MM74HC4511

## BCD-to-7 Segment Latch/Decoder/Driver

### General Description

This high speed latch/decoder/driver utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ( $\overline{LT}$ ), blanking ( $\overline{BI}$ ), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

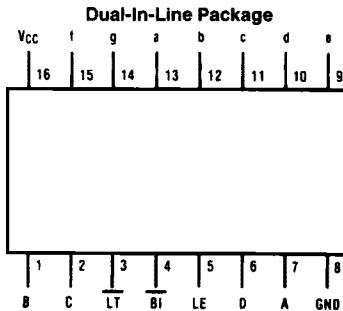
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to  $V_{CC}$  and ground.

### Features

- Latch storage of input data
- Blanking input
- Lamp test input
- Low power consumption characteristics of CMOS devices
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1  $\mu A$  maximum
- Low quiescent current: 80  $\mu A$  maximum over full temperature range (74 Series)

### Connection Diagram



TOP VIEW

TLF/5373-1

**Order Number MM54HC4511\* or MM74HC4511\***

\*Please look into Section 8, Appendix D for availability of various package types.

### Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
x	x	L	x	x	x	x	H	H	H	H	H	H	H	8
x	L	H	x	x	x	x	L	L	L	L	L	L	L	0
L	H	H	L	L	L	L	H	H	H	H	H	H	H	1
L	H	H	L	L	L	H	L	H	H	L	L	L	L	2
L	H	H	L	L	H	H	H	H	H	L	L	L	L	3
L	H	H	L	H	L	L	L	H	L	H	L	L	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	H	H	H	L	L	L	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	L	L	L	H	H	9
L	H	H	H	L	L	L	L	L	L	L	L	L	L	
L	H	H	H	L	L	H	L	L	L	L	L	L	L	
L	H	H	H	L	L	L	L	L	L	L	L	L	L	
L	H	H	H	L	L	H	L	L	L	L	L	L	L	
L	H	H	H	L	L	H	L	L	L	L	L	L	L	
L	H	H	H	L	L	H	L	L	L	L	L	L	L	
L	H	H	H	L	L	H	L	L	L	L	L	L	L	
H	H	H	x	x	x	x					*			*

x = Don't care

\* = Depends upon the BCD code applied during the 0 to 1 transition of LE.

**Absolute Maximum Ratings** (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC}$ + 1.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC}$ + 0.5V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_{OUT}$ )	±25 mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±50 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. ( $T_L$ ) (Soldering 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HC	-40	+85	°C
MM54HC	-55	+125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$		$T_A = -55$ to $125^\circ C$		Units
				Typ	Guaranteed Limits					
$V_{IH}$	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15	V		
			6.0V		4.2	4.2	4.2	V		
$V_{IL}$	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35	V		
			6.0V		1.8	1.8	1.8	V		
$V_{OH}$	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V		
			4.5V	4.5	4.4	4.4	4.4	V		
			6.0V	6.0	5.9	5.9	5.9	V		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 6.0$ mA $ I_{OUT}  \leq 7.8$ mA	4.5V	4.2	3.98	3.84	3.7	V		
			6.0V	5.7	5.48	5.34	5.2	V		
$V_{OL}$	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V		
			4.5V	0	0.1	0.1	0.1	V		
			6.0V	0	0.1	0.1	0.1	V		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V		
			6.0V	0.2	0.26	0.33	0.4	V		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA		
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	μA		

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ( $V_{OH}$  and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

\*\* $V_{IL}$  limits are currently tested at 20% of  $V_{CC}$ . The above  $V_{IL}$  specification (30% of  $V_{CC}$ ) will be implemented no later than Q1, CY'89.

**AC Electrical Characteristics**  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$ 

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from Inputs A thru D to any Output		60	120	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from $\overline{BI}$ to any Output		60	120	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from $\overline{LT}$ to any Output		60	120	ns
$t_S$	Minimum Setup Time Inputs A thru D to LE		10	20	ns
$t_H$	Minimum Hold Time Inputs A thru D to LE		--3	0	ns
$t_W$	Minimum Pulse Width for LE			16	ns

**AC Electrical Characteristics**  $C_L = 50 \text{ pF}$ ,  $t_r = t_f = 6 \text{ ns}$  (unless otherwise specified)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		74HC	54HC	Units
						$T_A = -40 \text{ to } 85^\circ C$	$T_A = -55 \text{ to } 125^\circ C$	
				Typ	Guaranteed Limits			
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from Inputs A thru D to any Output	$LE = 0V$ $\overline{LT} = V_{CC}$ $\overline{BI} = V_{CC}$	2.0V	300	600	756	894	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from $\overline{BI}$ to any Output	$\overline{LT} = V_{CC}$	2.0V	300	600	756	894	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay from $\overline{LT}$ to any Output	$\overline{BI} = 0V$	2.0V	300	600	756	894	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
$t_S$	Minimum Setup Time Inputs A thru D to LE		2.0V		100	126	149	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
$t_H$	Minimum Hold Time Inputs A thru D to LE		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
$t_W$	Minimum Pulse Width for LE		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
$t_r$ , $t_f$	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)							pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**INPUTS**

**A, B, C, D (Pins 7, 1, 2, 6)**—BCD data inputs. A (pin 7) is the least-significant data bit and D (pin 6) is the most significant bit. Hexadecimal data A–F at these inputs will cause the outputs to assume a logic low, offering an alternate method of blanking the display.

**OUTPUTS**

**a–g**—Decoded, buffered outputs. These outputs, unlike the 4511, have CMOS drivers, which will produce typical CMOS output voltage levels.

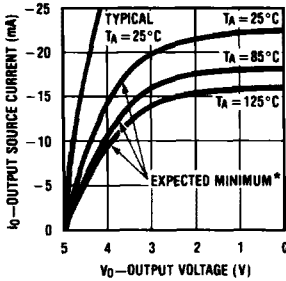
**CONTROLS**

**BI (Pin 4)**—Active-low display blanking input. A logic low on this input will cause all outputs to be held at a logic low, thereby blanking the display. LT is the only input that will override the BI input.

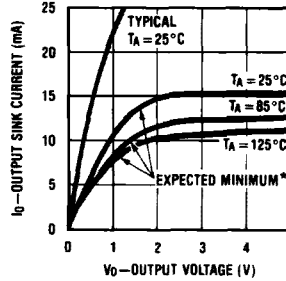
**LT (Pin 3)**—Active-low lamp test. A low logic level on this input causes all outputs to assume a logic high. This input allows the user to test all segments of a display, with a single control input. This input is independent of all other inputs.

**LE (Pin 5)**—Latch enable input. This input controls the 4-bit transparent latch. A logic high on this input latches the data present at the A, B, C and D inputs; a logic low allows the data to be transmitted through the latch to the decoder.

**Output Characteristics (V<sub>CC</sub> = 5V)**



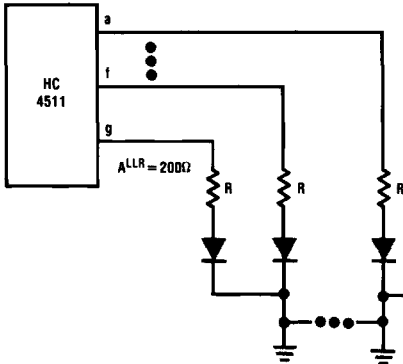
TL/F/5373-2



TL/F/5373-3

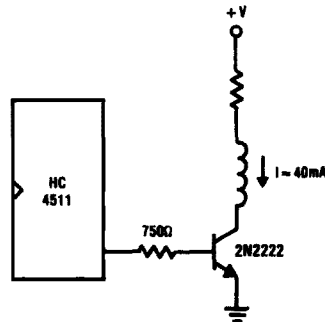
\*The expected minimum curves are not guarantees, but are design aids.

**Typical Applications**



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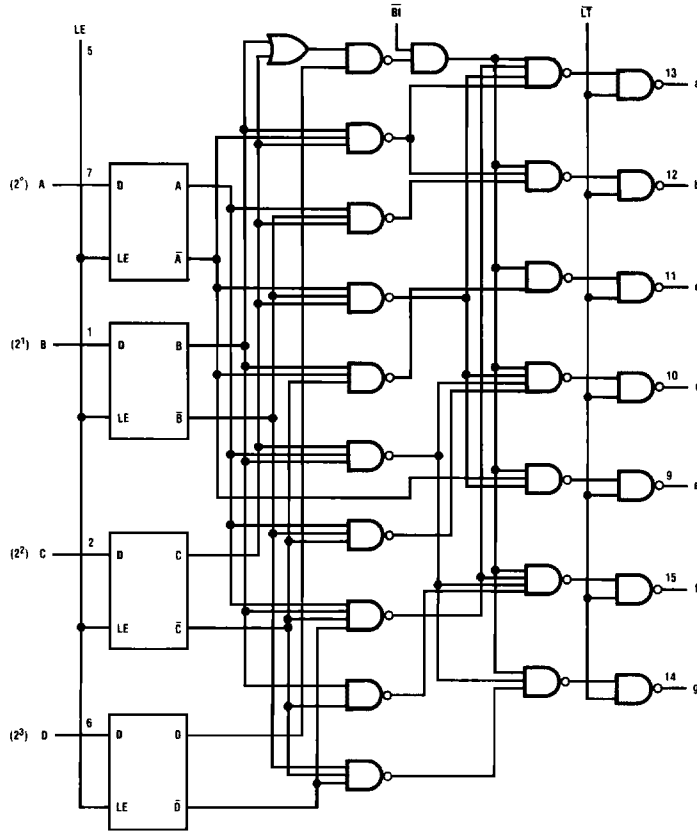
**Typical Common Cathode LED Connection**



TL/F/5373-5

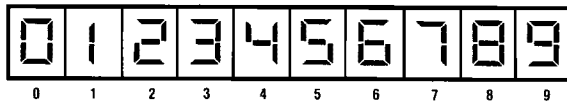
**Incandescent Bulb Driving Circuit**

# Logic Diagram



TL/F/5373-6

Display



TL/F/5373-7

Segment Identification



TL/F/5373-8