

**Target Specification**

November 1994

**DESCRIPTION**

The SSI 32C9210 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. This part supports headerless operation. The SSI 32C9210 has a four bit wide NRZ channel interface with disk transfers rates up to 120 megabits per second, an advanced ATA interface which supports host transfer rates up to 16.6 megabytes per second, and a sixteen bit wide data buffer interface capable of supporting concurrent full speed transfers on both disk and host interfaces. The circuitry of the SSI 32C9210 includes: a complete, highly automated ATA interface; an advanced, fully integrated buffer manager; a high performance disk formatter; and two fast Reed-Solomon ECC's, one for the header field and a second for the data field, both with on-the-fly hardware correction. The SSI 32C9210 maximizes performance while minimizing microcontroller intervention.

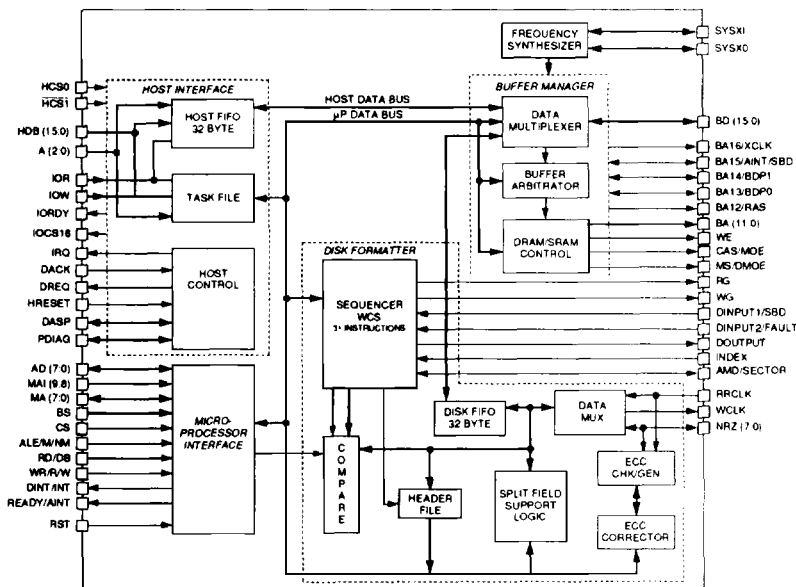
(continued)

**FEATURES**

- **ATA Interface**
  - Single chip PC AT controller (IDE)
  - Full ANSI ATA-1 and ATA-2 compliance
  - Direct PC bus connection with on-board 12 mA drivers
  - PC transfers to 16.6 megabytes per second
  - Supports PIO, DMA and Multiword DMA (EISA Class B Demand DMA)
  - Logic for daisy chaining 2 drives
  - Operates as master, slave or both
  - Automatic command decoding of write, write long, write multiple, write DMA, write buffer and format commands.

(continued)

**BLOCK DIAGRAM**



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# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

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#### DESCRIPTION (continued)

The SSI 32C9210 also supports dual bit NRZ interfaces. In dual bit mode, transfer rates up to 100 megabits per second on the disk interface are supported.

The highly automated Header ECC logic performs corrections on the header within one or two byte times, and data ECC is capable of performing corrections in real-time, allowing the SSI 32C9210 to read every sector on the disk in a single revolution even if every sector contained a correctable error.

The SSI 32C9210 is the latest in a line of sophisticated disk storage controllers. Other Silicon Systems' disk storage controllers include: the SSI 32C9800 (32C9810 headerless support) SCSI-3 controller, with host transfer rates up to 20 megabytes per second and disk data rates of up to 160 megabits per second. The SSI 32C9001, SSI 32C9301, SSI 32C9302 and SSI 32C9003 ATA controllers provide dual and serial NRZ data rates to 80 Megabits per second and ATA speeds to 13.3 megabytes per second. The SSI 32C9020, SSI 32C9022, SSI 32C9023 and SSI 32C9024 family members are SCSI disk controllers supporting fast, 8-bit wide SCSI interface, with disk data rates to 80 Megabits per second. The SSI 32C9340 disk controller completes the family providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9210 represents a major reduction in parts count. When the SSI 32C9210 ATA Controller is combined with the SSI 32R1510BR or SSI 32R2110R read/write device, the SSI 32P4782 read channel (1,7) or SSI 32P4910 PRML read channel (8/9), the 32H6826 servo/spindle controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

#### FEATURES (continued)

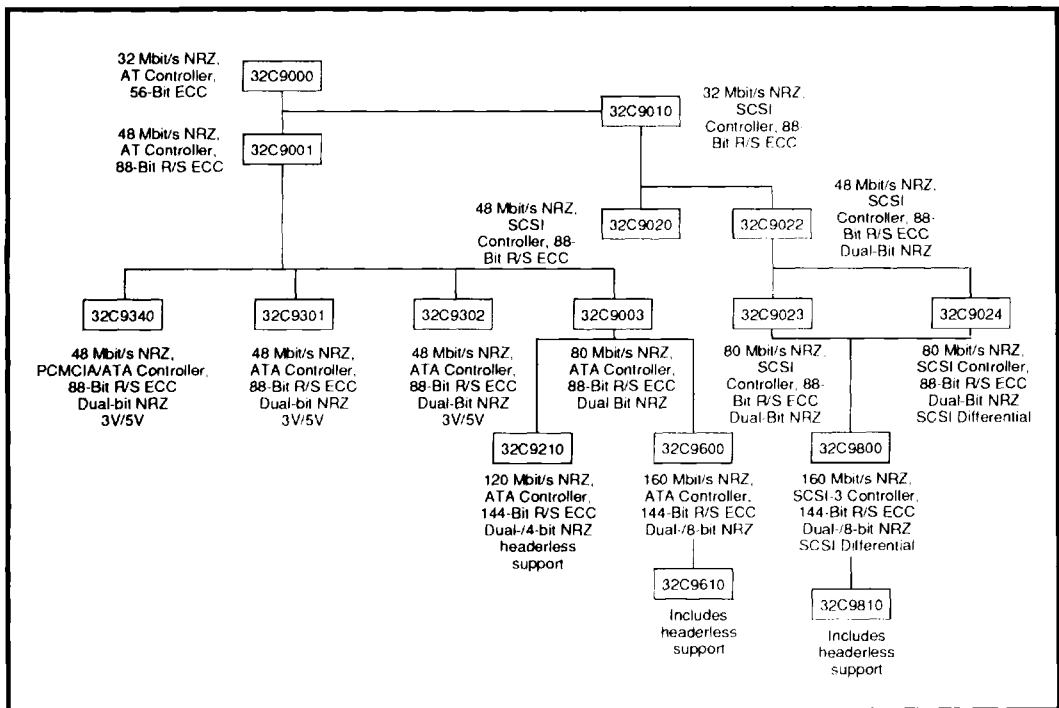
- Hardware support for read multiple and write multiple commands
- Hardware support for Cyl/Hd/Sec and LBA addressing modes, including automatic updates of the host task file registers in both modes
- Automatic Multi-sector data transfers without microprocessor intervention
- Automatic Host Interrupt and busy for multiple sector transfers
- 32 byte FIFO to improve performance
- Extensive power down modes
- Buffer manager
  - Direct support of SRAM
    - SRAM: up to 256k bytes of memory with throughput to 33.3 megabytes per second
  - Buffer CRC and/or buffer parity for increased data integrity
  - Programmable memory timing
  - Flexible buffer RAM segmentation
  - Dedicated host, disk and microprocessor address pointers
  - Buffer streaming with internal buffer protection circuit providing buffer integrity
- Disk formatter
  - Unique headerless operation
  - 4-Bit NRZ interface supporting data rates to 120 megabits per second, or
  - 2-Bit NRZ interface supporting data rates to 100 megabits per second
  - Automatic multi-sector transfers
  - Error tolerant sync detection
  - Header based split data field support
  - Advanced sequencer organized in 31 x 4 bytes
  - Timeouts for sync detection, sector or index pulse detection, and retry limiting

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# SSI 32C9210

## ATA-2 Storage Controller 120 Mbit/s, Headerless Support

- Disk formatter (continued)
  - 144-bit Reed Solomon ECC for the data field, with "on-the-fly" fast hardware correction circuitry
    - Capable of correcting up to six 8-bit symbols in error
    - Guaranteed to correct a single 41-bit error burst, or two 17-bit error bursts
    - Fast hardware on-the-fly correction assures continuous data transfers even if consecutive sectors are in error
  - 40-bit Reed Solomon ECC for the header field, with "on-the-fly" hardware correction circuitry which completes within 1 or 2 byte times
    - Guaranteed to correct a single 9-bit error burst
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate host and disk interrupts
  - 1024 byte buffer window with wait stated or polled access
- Other Features
  - Frequency synthesizers for buffer clock
  - Internal power down mode
  - Available in 120-pin TQFP



**FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy**

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# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

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#### FUNCTIONAL DESCRIPTION

The SSI 32C9210 contains the following four major functional blocks:

- Microprocessor Interface
- ATA Interface
- Disk Formatter
- Buffer Manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9210 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9210. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9210 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 12 mA drivers allowing for direct connection of the SSI 32C9210 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro-controller involvement. The ATA block interfaces directly with the buffer manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the buffer manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The disk formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 4 bytes (32 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities.

This allows the SSI 32C9210 to interface with many different read/write channels and allows the user of the SSI 32C9210 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9210 controller and the SSI 32P4910 PRML read channel (8/9), you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 40-bit Reed-Solomon ECC for headers and a 144-bit Reed-Solomon code for data. The header ECC circuitry performs correction of the header bytes within one or two byte times, minimizing delays. The data ECC correction circuitry performs data corrections rapidly. The data ECC circuitry guarantees that the correction logic will always be available to correct the next sector if necessary.

The disk formatter provides additional reliability by use of error tolerant sync detection. This feature allows the creation of a multi-byte sync field and the detection of data synchronization even in the event of errors within the sync field.

The 32C9210 provides headerless capabilities. Silicon Systems' unique approach supports operation with existing servo-subsystems. Minimal or no change to the servo-subsystem is required. Head position information from the servo-subsystem is validated in the controller. The controller requires basic servo wedge timing and on-track status. After power on and initialization, the controller constantly keeps track of head position both within and across zones. The controller provides hardware to support defect management.

The buffer manager manages the data buffer of the controller. The buffer manager supports SRAM, and creates all of the necessary timing and control signals for a wide range of speeds. Besides interfacing with the buffer memory, the buffer manager interfaces with the ATA Interface block, the disk formatter block, the ECC corrector and the microprocessor. If more than one of these blocks requires access to the buffer memory, the

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# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

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buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9210 can sustain ATA operations at the rate of 33.3 megabytes per second, disk formatter operations at 120 megabits per second and still has sufficient band-width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

Besides the ability to generate and check data parity, the ATA interface also includes a CRC generation and checking capability. During writes, a CRC can be generated on data received from the host and checked when the data is transferred to the disk formatter. The CRC is part of the data ECC and is always written by the disk formatter. If the ATA interface generates the CRC, then the disk formatter writes the CRC field that was generated by the ATA interface to the media, or the disk formatter generates the CRC itself. During reads the CRC is read from the media by the disk formatter. If buffer CRC is enabled, the disk formatter writes the CRC to the buffer and the CRC is re-checked by the ATA interface when the data is transferred to the host, or the disk formatter checks the CRC that is read from the media. The addition of CRC to the ATA interface adds a high degree of integrity, and detects most memory errors that may occur in the buffer memory.

# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

#### PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — HCS1.

#### GENERAL

NAME	TYPE	DESCRIPTION
VDD	-	POWER SUPPLY PIN
GND	-	GROUND

#### HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various host control, status, and data registers.
HCS1	I	HOST CHIP SELECT 1. This pin selects access to the control block task file registers.
HCS0	I	HOST CHIP SELECT 0. This pin selects access to the command block task file registers.
IOCS16	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
IRQ	O,Z	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O,Z	I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin will be tristated when a read or write is not in progress.
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller.
DACK	I	DMA ACKNOWLEDGE. This active low signal is used during DMA transfer between the host and the controller.
IOR	I	I/O READ. This active low pin is asserted by the Host during a Host read operation. When asserted with HCS0, HCS1, or DACK, data from the device is enabled onto the host data bus if the device is currently selected.
IOW	I	I/O WRITE. Asserted active low by the HOST during a HOST write operation. When asserted with HCS0, HCS1, or DACK, data from the host data bus is strobed into the device.

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# SSI 32C9210

## ATA-2 Storage Controller 120 Mbit/s, Headerless Support

### HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
HRESET	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
DASP	I,OD	DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present.
PDIAG	I,OD	PASSED DIAGNOSTICS. This signal is an output when configured as Drive 1 and an input when configured as Drive 0.

### DISK INTERFACE

INDEX	I	INDEX. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA16 pin, this pin can function as input or index.
DOOUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
DINPUT1/SBD	I	DISK SEQUENCER INPUT 1. This pin may be used to synchronize the sequencer to an external event.
DINPUT2/FAULT	I	DISK SEQUENCER INPUT 2. This pin may be used to synchronize the sequencer to an external event, or as a write fault signal.
AMD/SECTOR	I	ADDRESS MARK DETECT/SECTOR. In hard sector mode, this is the input for the sector pulse from the disk drive. In soft sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out.
NRZ (7:0)	I/O	NON RETURN TO ZERO. These signals are the read data input 0 through 7 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ7 is the most significant bit.

# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

#### PIN DESCRIPTION (continued)

##### MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{\text{RST}}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/NM	I	ADDRESS LATCH ENABLE/multiplexed or Non-multiplexed address select. If this input is constantly low, the microprocessor interface is configured with non-multiplexed address and data busses. If this input is ever high, the microprocessor interface is configured with a multiplexed address and data bus. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{\text{WR}}/\text{R}/\overline{\text{W}}$	I	WRITE STROBE/READ/WRITE. When the Intel bus control interface is selected, this signal acts as the $\overline{\text{WR}}$ signal. When the write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register.  When the Motorola bus control interface is selected, this signal acts as the R/W signal. A high on this input along with the $\overline{\text{RD}}/\overline{\text{DS}}$ signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{\text{RD}}/\overline{\text{DS}}$ signal asserted and the CS signal asserted high indicates a write operation.
$\overline{\text{RD}}/\overline{\text{DS}}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{\text{RD}}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals.  When the Motorola bus control interface is selected, this signal acts as the $\overline{\text{DS}}$ signal. A high on the R/W signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/W signal along with this signal asserted and the CS signal asserted high indicates a write operation.
$\overline{\text{DINT}}/\overline{\text{INT}}$	O, OD	DISK INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin READY/AINT is programmed as ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.

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# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

#### MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory.  When configured in the Non-multiplexed mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS. This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a multiplexed type microprocessor cycle. These signals are non-multiplexed address input when used with a Non-multiplexed microprocessor.
MAI (9:8)	I	MICROPROCESSOR ADDRESS INPUTS. These signals are address input lines for bits 9 and 8 of the address. They are inputs regardless of whether multiplexed or non-multiplexed data and address busses are used. In the multiplexed mode, these bits are latched internally with the ALE signal; in the non-multiplexed mode, they are not latched.
READY/AINT	O, OD	READY/HOST SIDE INTERRUPT. When programmed as the ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'ready' function.
BS	I	BUFFER WINDOW SELECT. This signal is asserted during microprocessor access of the buffer window.

#### BUFFER MANAGER INTERFACE

SYSXI	I	CRYSTAL INPUT/SYSTEM CLOCK. This is the crystal input to the buffer manager frequency synthesizer, or the clock input that is used to generate buffer memory access cycles when the frequency synthesizer is bypassed.
SYSXO	O	CRYSTAL OUTPUT.
CAS/SMOE	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE. This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
$\overline{WE}$	O	WRITE ENABLE. This signal is asserted low when a buffer memory write operation is active.
BD(15:0)	I/O	BUFFER MEMORY DATA BUS. These signals are bits 15-0 of the 16-bit parallel data lines to/from the buffer memory.

7

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# SSI 32C9210

## ATA-2 Storage Controller

### 120 Mbit/s, Headerless Support

#### BUFFER MANAGER INTERFACE (continued)

NAME	TYPE	DESCRIPTION
BA16/XCLK	O	BUFFER ADDRESS 16/SYNTHESIZER OUTPUT CLOCK. This signal is either the output of the frequency synthesizer, or buffer address 16. At reset, this signal is the equivalent of the signal at SYSXI (input clock to the frequency synthesizer.)
BA15/ $\overline{\text{AINT}}$ /SBD	I/O	BUFFER ADDRESS 15/AT INTERRUPT/SYNC BYTE DETECT. This signal may be used for addressing the buffer memory in SRAM mode, or as a separate local microprocessor interrupt for the host interface, or as a sync byte detect signal input for the disk formatter. After $\overline{\text{RST}}$ is asserted, this signal will be configured as SBD (i.e., as an input).
BA14/BDP1	I/O	BUFFER MEMORY ADDRESS 14/BUFFER DATA PARITY 1. This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD(15:8) in DRAM mode.
BA13/BDP0	I/O	BUFFER MEMORY ADDRESS 13/BUFFER DATA PARITY 0. This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD (7:0) in DRAM mode.
BA12/ $\overline{\text{RAS}}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE. This signal is used for addressing the buffer memory in SRAM mode, or as the row address strobe in DRAM mode. After $\overline{\text{RST}}$ is asserted, this signal will be high.
BA (11:0)	O	BUFFER MEMORY ADDRESS LINES. These are bits 11-0 for addressing the buffer memory.
MS/DMOE	O	MEMORY SELECT/DRAM MEMORY OUTPUT ENABLE. This pin is configured as memory select in SRAM mode, or as memory output enable in DRAM mode.

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