Electrical Specifications

ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Max	Units
P_D	Power Dissipation	–	1	W
V_{CC}	Supply Voltage	–0.5	7	V
V_I	Input Voltage	–0.5	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	85	°C
T_{STG}	Storage Temperature	–40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	4.75	5.25	V
T_A	Ambient Temperature	0	55	°C

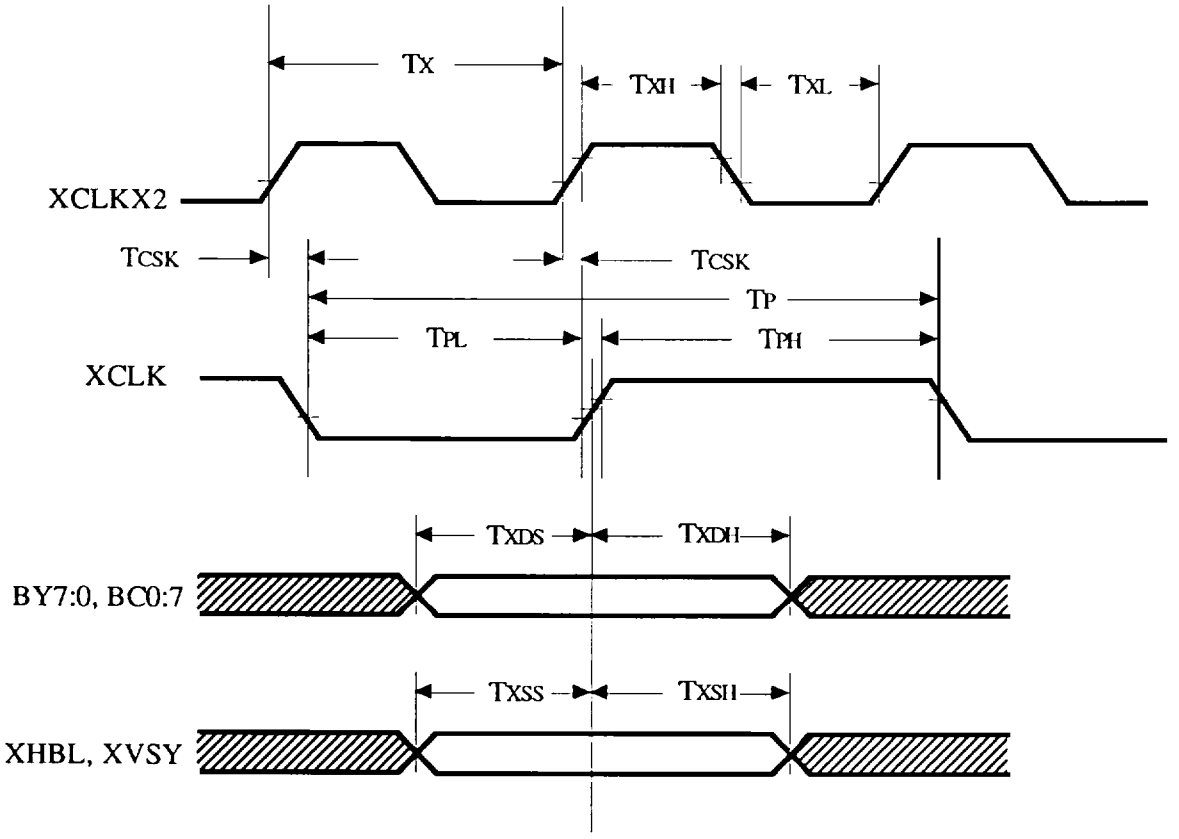
DC CHARACTERISTICS

(Under Normal Operation Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Max	Units
I_{CC1}	Power Supply Current	@27 MHz CLK, 0°C, 5.25V	–	100	mA
I_{IL}	Input Leakage Current		–10	+10	uA
I_{OZ}	Output Leakage Current	High Impedance	–10	+10	uA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC}	V
V_{OL}	Output Low Voltage	I_{OL}=18mA (RDY, MEMCS16/)	–	0.45	V
		I_{OL} = 13.5 mA (I2CK, I2CO)	–	0.45	V
		I_{OL} = 9 mA (all other signals)	–	0.45	V
V_{OH}	Output High Voltage	I_{OH}=10mA (RDY, MEMSC16/)	2.4	–	V
V_{OH}	Output High Voltage	I_{OH} = 5.0 mA (all other signals)	2.4	–	V

AC TIMING CHARACTERISTICS - INPUT VIDEO TIMING

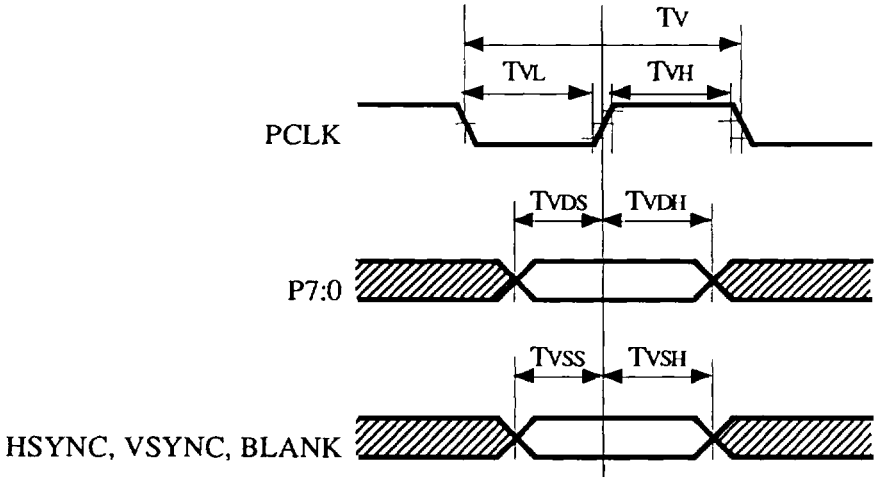
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_P	XCLK Period	13.5 MHz Typ	66	74	80	nS
T_{PH}	XCLK High Time		$0.45T_P$	–	$0.55T_P$	nS
T_{PL}	XCLK Low Time		$0.45T_P$	–	$0.55T_P$	nS
T_X	PCX2 Period	27.0 MHz Typ	T_P / 2	37	T_P / 2	nS
T_{XH}	PCX2 High Time		$0.45T_X$	–	$0.55T_X$	nS
T_{XL}	PCX2 Low Time		$0.45T_X$	–	$0.55T_X$	nS
T_{XSS}	XVSY, XHBL setup to XCLK rising edge		12	–	–	nS
T_{XSH}	XVSY, XHBL hold from XCLK rising edge		0	–	–	nS
T_{XDS}	BY 7:0, BC 7:0 setup to XCLK rising edge		10	–	–	nS
T_{XDH}	BY 7:0, BC 7:0 setup to XCLK rising edge		0	–	–	nS
T_{CSK}	PCX2 to XCLK skew required		0	–	10	nS
T_{RST}	Reset Pulse Width		$64T_X$	–	–	nS



PC Video Input Video Timing

AC TIMING CHARACTERISTICS - VGA INPUT TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_V	PCLK Period	–	–	45	Mhz
T_{VH}	PCLK High Time	$0.45T_V$	–	$0.55T_V$	nS
T_{VL}	PCLK Low Time	$0.45T_V$	–	$0.55T_V$	nS
T_{VSS}	HSYNC, VSYNC, BLANK setup to PCLK rising edge	2	–	–	nS
T_{VSH}	HSYNC, VSYNC, BLANK hold from PCLK rising edge	3	–	–	nS
T_{VDS}	P7:0 setup to PCLK rising edge	2	–	–	nS
T_{VDH}	P7:0 hold from PCLK rising edge	4	–	–	nS
F vhmax	Maximum VGA HYSNC rate for stable NTSC Source	–	–	48	kHz
F vhmax	Maximum VGA HSYNC rate for stable PAL Source	–	–	47	kHz

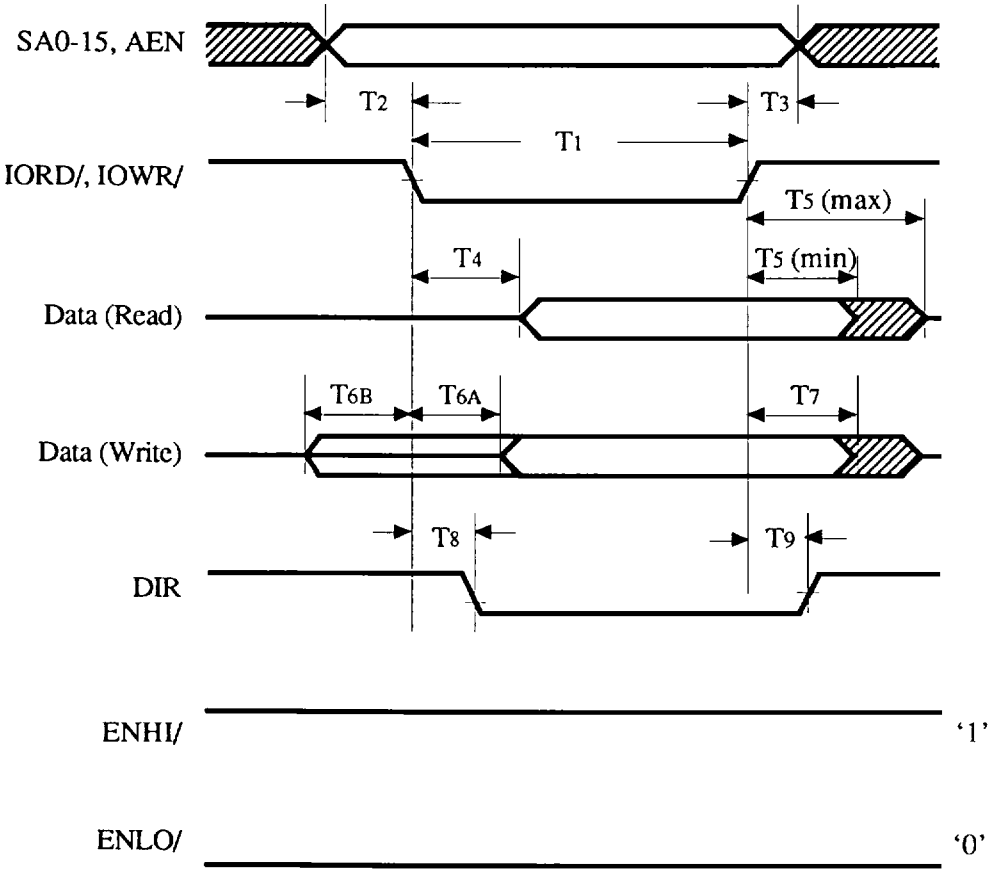


PC Video VGA Input Timing

TIMING CHARACTERISTICS - ISA BUS I/O TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{1A}	IORD/, IOWR/ Pulse Width, Reg FF Bit 2 = '0'	Note 1	2Tp + 20ns	–	–	nS
T_{1B}	IORD/, IOWR/ Pulse Width, Reg FF Bit 2 = '1'	Note 1	175	–	–	nS
T_2	Address setup to IORD, IOWR/		90	–	–	nS
T_3	Address hold from IORD, IOWR/		0	–	–	nS
T_4	I/O Read Data Delay from IORD/		–	–	50	nS
T_5	I/O Read Data hold from IORD/		0	–	30	nS
T_{6A}	I/O Write Data setup to IOWR/ Reg FF Bit 2='0'	Note 1	2Tp	–	–	nS
T_{6B}	I/O Write Data setup to IOWR/ Reg FF Bit 2='1'	Note 1	22	–	–	nS
T_7	I/O Write Data hold from IOWR/		0	–	–	nS
T_8	IORD/ falling to DIR valid		–	–	10	nS
T_9	IORD/ rising to DIR invalid		–	–	10	nS

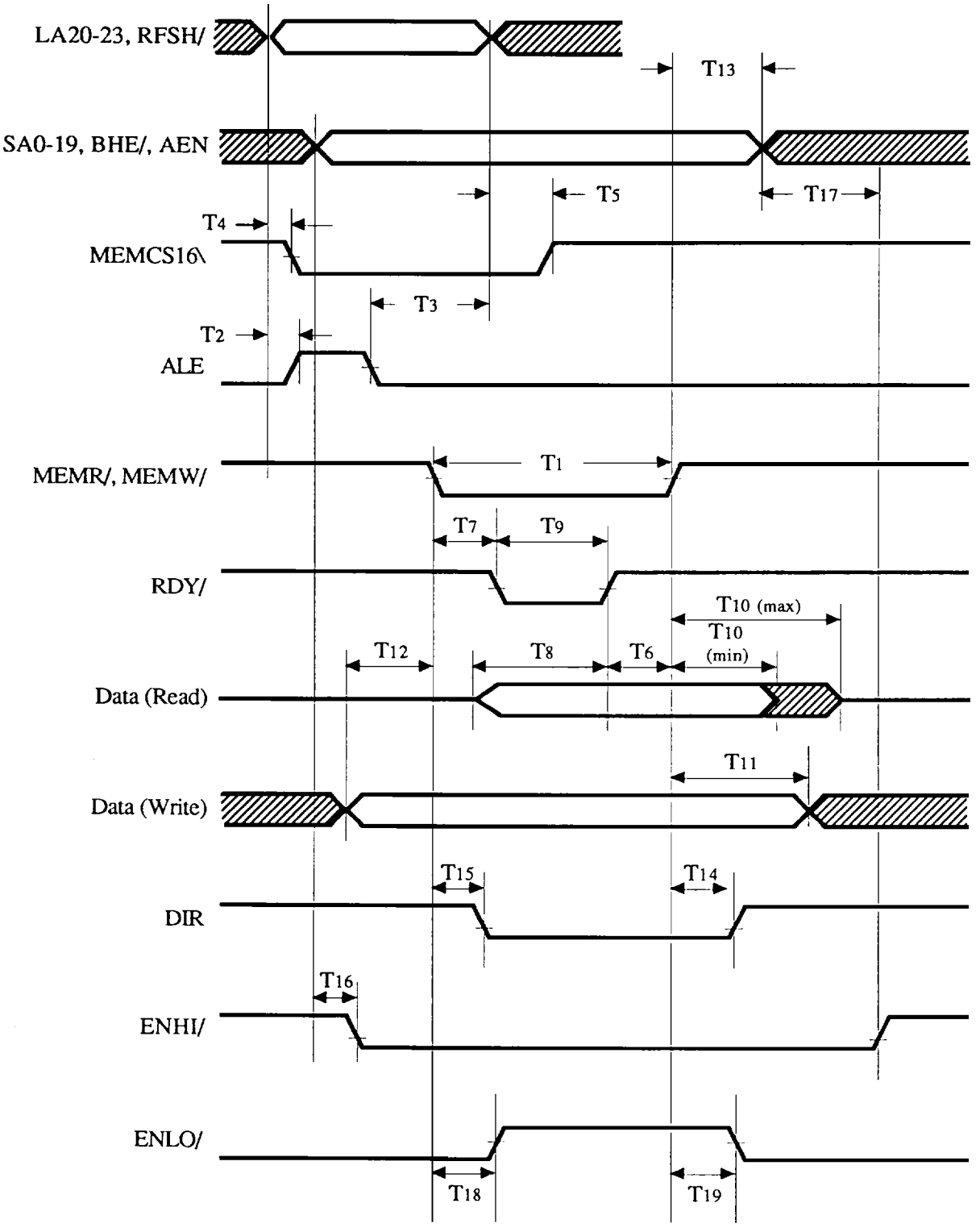
Note 1: See Register FF description



ISA Bus I/O Cycle Timing

AC TIMING CHARACTERISTICS - ISA BUS TIMING

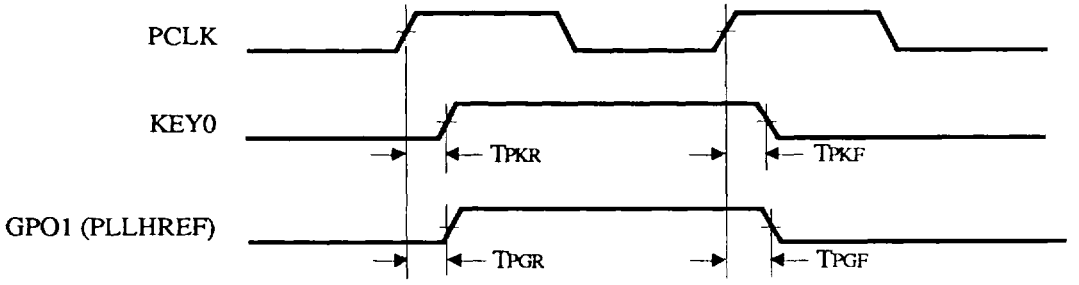
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_1	MEMR/, MEMW/ Pulse Width		175	–	–	nS
T_2	Address setup to ALE		20	–	–	nS
T_3	Address hold from ALE		0	–	–	nS
T_6	MEMR/, MEMW/ hold from RDY (Memory)		0	–	–	nS
T_{10}	Memory Read Data Hold from MEMR/		10	–	35	nS
T_{11}	Memory Write Data Hold from MEMR/		0	–	–	nS
T_7	MEMR/, MEMW/ to RDY Low Delay		-	–	25	nS
T_8	Memory Read Data setup to RDY		25	–	–	nS
T_9	RDY width		8 T_X	–	24 T_X	nS
T_4	LA valid to MEMCS16 Low Delay		–	–	20	nS
T_5	LA invalid to MEMCS16 High Delay		–	–	20	nS
T_{12}	Memory Write Data Setup to MEMW/		-40	–	–	nS
T_{13}	SA Hold from MEmr/, MEMW/		20	–	–	nS
T_{14}	MEMR/ falling to DIR valid		–	–	10	nS
T_{15}	MEMR/ rising to DIR invalid		–	–	10	nS
T_{16}	BHE falling to ENHI/ valid		–	–	10	nS
T_{17}	BHE rising to ENHI/ invalid		–	–	10	nS
T_{18}	MEMR/, MEMW/ to ENLO/ valid		–	–	10	nS
T_{19}	MEMR/, MEMW/ to ENLO/ invalid		–	–	10	nS



ISA Bus Timing

AC TIMING CHARACTERISTICS - VGA PIXEL CLOCK TO KEYO TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{PKR}	PCLK to KEYO Rising Delay		–	–	13	nS
T_{PKF}	PCLK to KEYO Falling Delay		–	–	17	nS
T_{PGR}	PCLK to GPO1 (PLLHREF) Rising Delay		–	–	10	nS
T_{PGF}	PCLK to GPO1 (PLLHREF) Falling Delay		–	–	9	nS

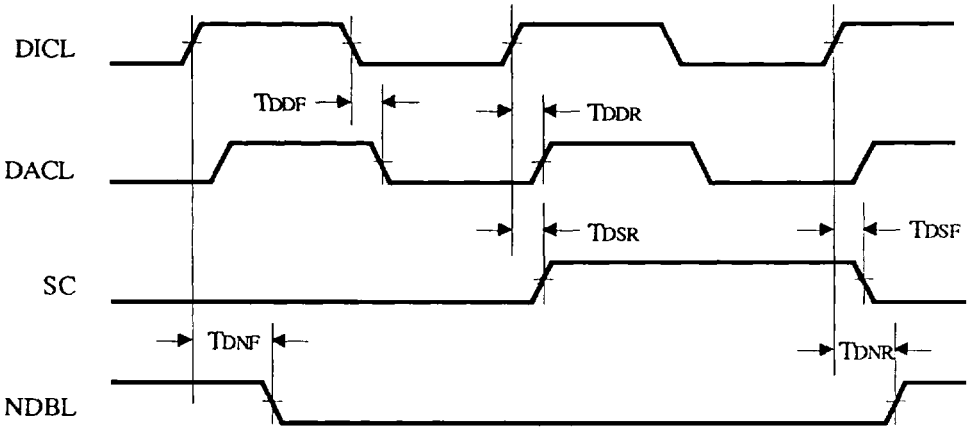


VGA Pixel KEYO (Analog Mux Control Timing)

AC TIMING CHARACTERISTICS - DISPLAY CLOCK TO DAC CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{DDR}	DICL to DACL Rising Delay		–	–	12	nS
T_{DDF}	DICL to DACL Falling Delay		–	–	12	nS
T_{DSR}	DICL to SC Rising Delay		–	–	14	nS
T_{DSF}	DICL to SC Falling Delay		–	–	14	nS
T_{DNR}	DICL to NDBL Rising		–	–	25	nS
T_{DNF}	DICL to NDBL Falling		–	–	25	nS

Note: All max values will increase by 2nS if horizontal zoom is enabled.



DISPLAY Clock to DAC Clock, DAC Blank and VRAM Shift Clock Timing

AC TIMING CHARACTERISTICS - MEMORY CLOCK TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_X	PCX2 (Note 1)	Note 1	–	T_P / 2	–	nS

Note 1: The 2 x Video Pixel Clock (PCX2) is used for memory timing. PCX2 is equal to twice the pixel input clock (XCLK). This clock is also used to generate timing for the random access port. DICL is used to generate the Shift Clock (SC).

PC Video AC TIMING CHARACTERISTICS - VRAM ACCESS REQUIREMENTS

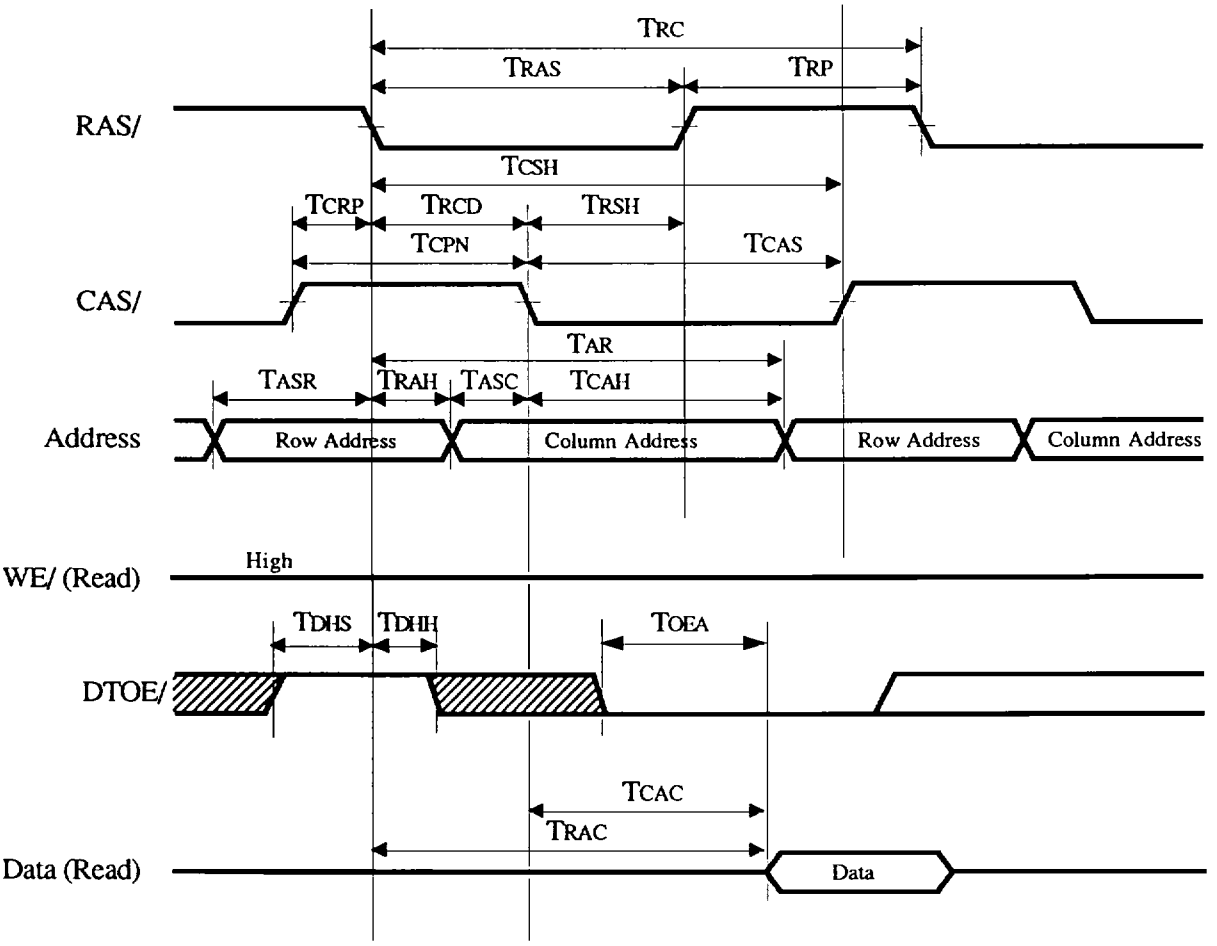
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RAC}	Data Access Time from RAS/		–	–	4 T_X	nS
T_{CAC}	Data Access Time from CAS/		–	–	T_X	nS

TIMING CHARACTERISTICS - VRAM TIMING

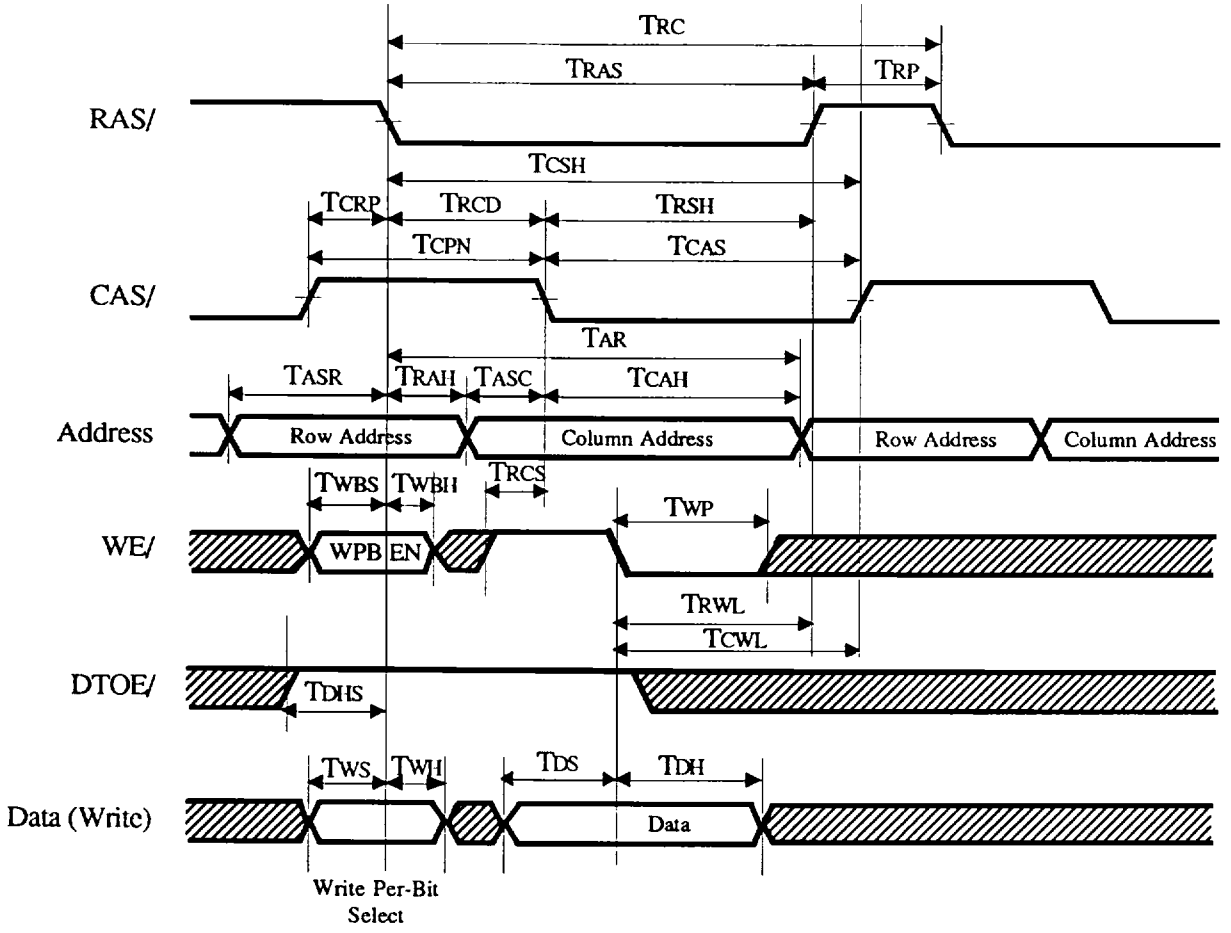
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RC}	Random read or write cycle time		$7T_X$	–	–	nS
T_{PC}	Fast-page cycle time		$4T_X$	–	–	nS
T_{RP}	RAS/ precharge		$3T_X$	–	–	nS
T_{RAS}	RAS/ pulse width		$4T_X$	–	–	nS
T_{RASP}	Fast-page RAS/ pulse width		$4T_X$	–	–	nS
T_{RSH}	RAS/ hold from CAS/		$2T_X$	–	–	nS
T_{CPN}	CAS/ precharge		$4T_X$	–	–	nS
T_{CP}	Fast-page CAS/ precharge time		$1T_X$	–	–	nS
T_{CAS}	CAS/ pulse width		$3T_X$	–	–	nS
T_{CAS1}	CAS/ pulse width (Fast Page Cycle)		$3T_X$	–	–	nS
T_{CAS2}	CAS/ pulse width (Fast Page Cycle)		$3T_X$	–	–	nS
T_{CSH}	CAS/ hold from RAS/		$5T_X$	–	–	nS
T_{RCD}	RAS/ to CAS/ delay		$1T_X$	–	–	nS
T_{CRP}	CAS/ high to RAS/ low precharge		$3T_X$	–	–	nS
T_{ASR}	Row Address setup time		$2T_X$	–	–	nS
T_{RAH}	Row Address hold time		$1T_X$	–	–	nS
T_{ASC}	Column Address setup to CAS/		$1T_X$	–	–	nS
T_{CAH}	Column Address hold time		$2T_X$	–	–	nS
T_{RAD}	RAS/ to Column Address delay time		$1T_X$	–	–	nS
T_{RAL}	Column Address to RAS/ lead time		$3T_X$	–	–	nS
T_{RCS}	Read command setup time		$5T_X$	–	–	nS
T_{WP1}	Write command pulse width(Fast Page Cycle)		$2T_X$	–	–	nS

AC TIMING CHARACTERISTICS - VRAM TIMING (Continued)

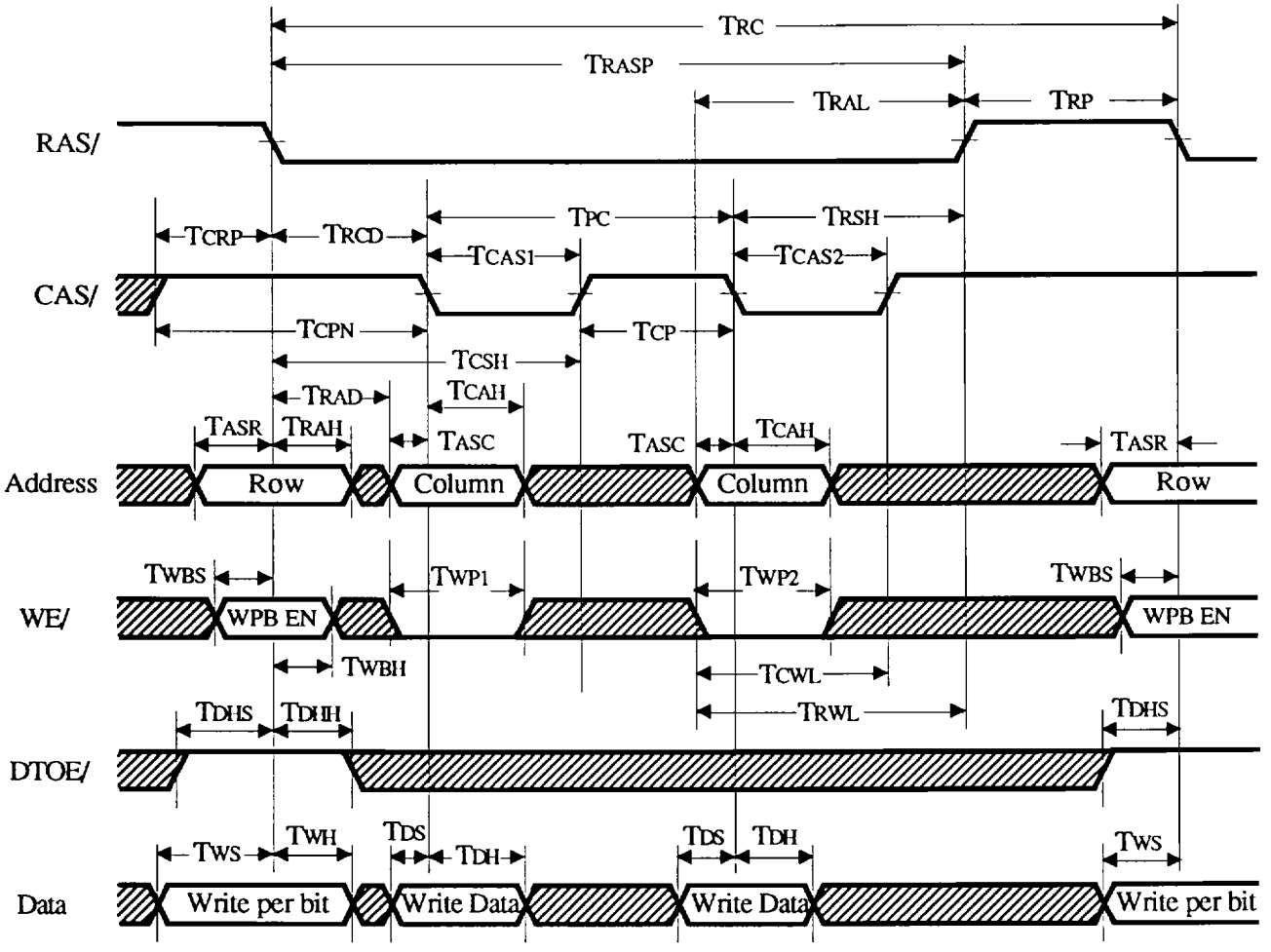
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{WP2}	Write command pulse width(Fast Page Cycle)		2 T_X	–	–	nS
T_{WP}	Write command pulse width		3 T_X	–	–	nS
T_{RWL}	Write command to RAS/ lead time		2 T_X	–	–	nS
T_{CWL}	Write command to CAS/ lead time		2 T_X	–	–	nS
T_{DS}	Data-in setup time		0.5 T_X	–	–	nS
T_{DH}	Data-in hold time		1 T_X	–	–	nS
T_{RPC}	RAS/ high to CAS/ low precharge time		5T_X	–	–	nS
T_{DLS}	DT/ low setup time		1 T_X	–	–	nS
T_{RDH}	DT/ low hold time after RAS/ low		3 T_X	–	–	nS
T_{CDH}	DT/ low hold time after CAS/ low		1 T_X	–	–	nS
T_{DHS}	DT/ high setup time		1 T_X	–	–	nS
T_{DHH}	DT/ high hold time		1 T_X	–	–	nS
T_{DTR}	DT/ high to RAS/ high delay		0	–	–	nS
T_{DTC}	DT/ high to CAS/ high delay		1 T_X	–	–	nS
T_{WBS}	Write-per-bit setup time		0.5 T_X	–	–	nS
T_{WBH}	Write-per-bit hold time		1 T_X	–	–	nS
T_{WS}	Write bit selection setup time		0.5 T_X	–	–	nS
T_{WH}	Write bit selection hold time		1 T_X	–	–	nS
T_{DTH}	DT/ high hold time after RAS/ high		2 T_X	–	–	nS



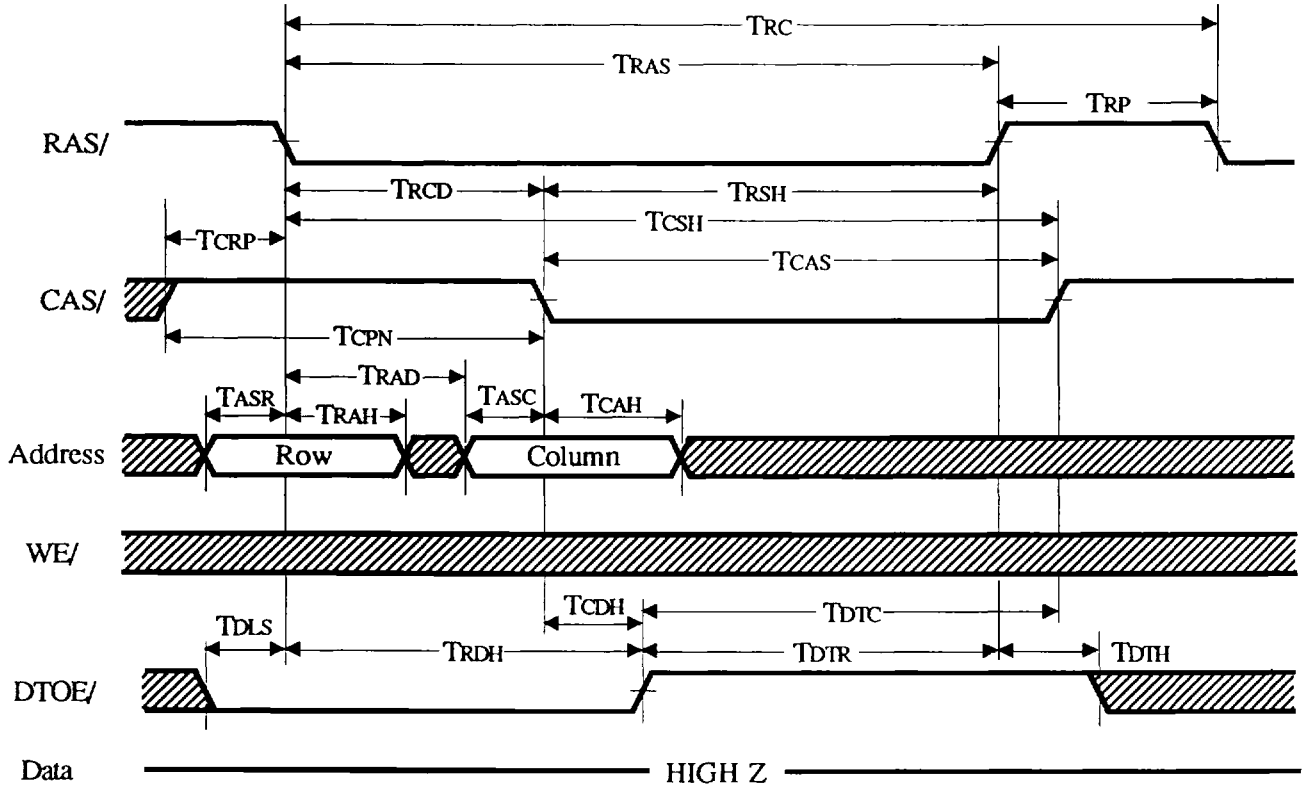
VRAM Random Read Cycle Timing



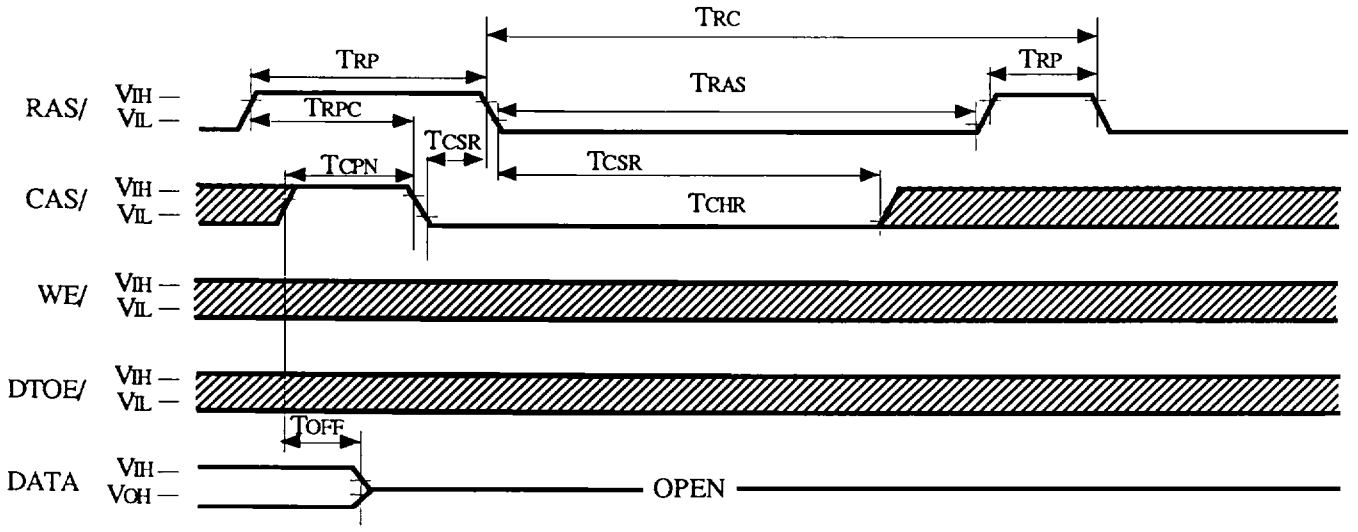
VRAM Random Write Cycle Timing



VRAM Fast-page Write Cycle Timing



VRAM Data Transfer Cycle Timing



VRAM Refresh Cycle Timing